R8051 Microcontroller

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Features

- Supports Virtex™, Virtex™-E and Spartan®-II devices
- Reduced instruction cycle time: up to 12 times faster than Legacy 8051
- 8-bit Control Unit
- 8-bit Arithmetic-Logic Unit
- 32-bit Input/Output ports
- Two 16-bit Timer/Counters
- Serial Peripheral interfaces in full duplex mode
- Two priority Interrupt Controllers
- Internal Data Memory interface can address up to 256 bytes of Read/Write Data Memory Space
- External Memory interface can address up to 64K bytes of External Program Memory Space and up to 64K bytes of External Data Memory Space
- Special Function Registers interface

AllianceCORE™ Facts

Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core Specification, Instruction set details, Tests set details
Design File Formats	.ngo, EDIF Netlist, VHDL or Verilog Source RTL available at additional cost
Constraints File	R8051.ucf
Verification	VHDL or Verilog testbench
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	Example design, assembler programs
Additional Items	Simulation and synthesis scripts
Simulation Tool Used	
1076-Compliant VHDL Simulator, Verilog Simulator	
Support	
Support provided by CAST, Inc.	

Applications

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Table 2: Core Implementation Data

Supported Family	Device Tested	CLB Slices[1]	Clock IOBs[2]	IOBs[2]	Performance (MHz)	Xilinx Tools	Special Features
Spartan-II	2S150-6	1299	1	159	34	3.2i	None
Virtex	V200-6	1299	1	159	33	3.2i	None
Virtex-E	V200E-8	1299	1	159	42	3.2i	None

Notes:
1. Optimized for speed
2. Assuming all core I/Os are routed off-chip

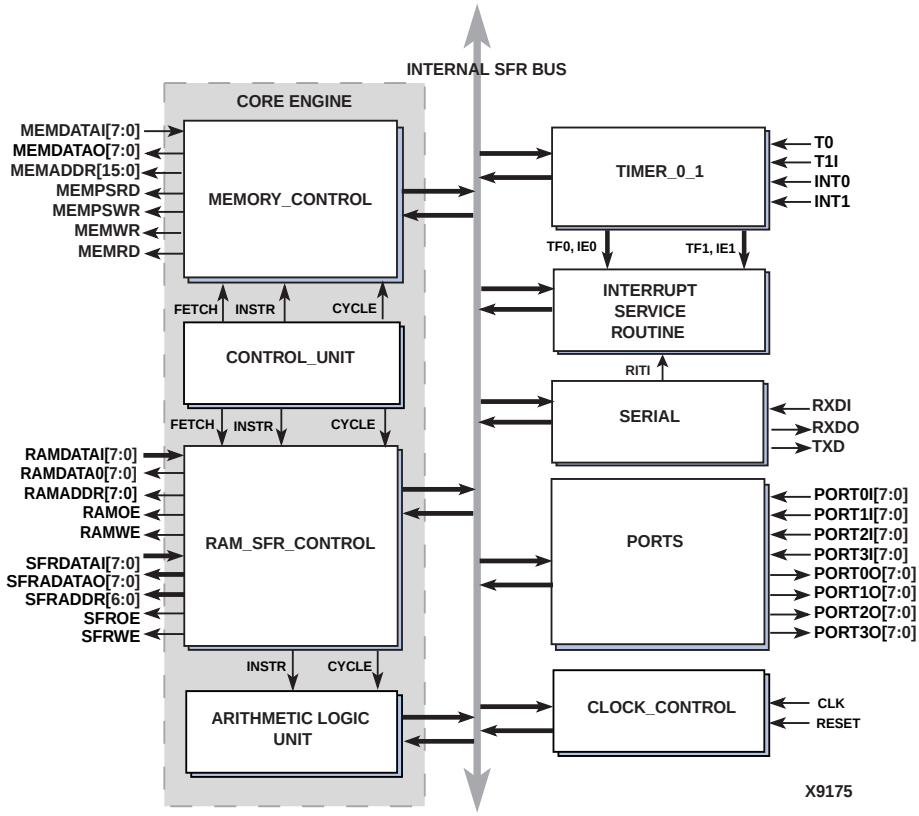

Table 1: R8051 Microcontroller Block Diagram

General Description

The R8051 is a core of a Fast Single-Chip 8-bit Microcontroller and is derived from the 80C51 microcontroller. The R8051 is a fully functional 8-bit Embedded Controller that executes all ASM51 instructions and has the same instruction set as the 80C31. The R8051 serves software and hardware interrupts, provides an interface for serial communications, and a timer system.

The R8051 is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with positive-edge clocking, no internal tri-states and a synchronous reset; therefore scan insertion is straightforward.

Functional Description

The R8051 core is partitioned into modules as shown in figure 1 and described below. A netlist version is provided for the core.

Core Engine

The R8051 engine allows to fetch instruction from program memory and to execute using RAM or SFR. The R8051 Core Engine is composed of four components:

- Memory control unit
- Control unit
- RAM and SFR control unit
- Arithmetic-logic unit

Memory Control Unit

- Can address up to 64K bytes of External Program Memory Space
- Can address up to 64K bytes of External Data Memory Space

Control Unit

The Control Unit performs intstruction fetch and execution from the Memory Control Unit and the RAM_SFR Control Unit.

RAM and SFR Control Unit

- Can address up to 256 bytes of Read/Write Data Memory Space
- Serves the Interface for off-core Special Function Registers

The Arithmetic Logic Unit Performs

- 8 bit arithmetic operations
- 8 bit logical operations
- Boolean manipulations
- 8 x 8 bit multiplication
- 8 / 8 bit division

Timer 0 and 1

Timers 0 and 1 are nearly identical. Timers 0 and 1 both have four modes. They are:

- 13-bit Timer/counter,
- 16-bit Timer/counter,
- 8-bit timer/counter with auto reload,
- two 8-bit timers.

The later mode is available to Timer 0 only. Each timer can also serve as a counter of external pulses (1 to 0 transition) on the corresponding T0 or T1 pin. One other option is to gate the timer/counter using an external control signal. This allows the timer to measure the pulse width of external signals.

Interrupt Service Routine

The R8051 core improves the three-priority interrupt system. There are 14 interrupt sources. Each source has an independent priority bit, flag, interrupt vector, and enable. In addition, interrupts can be globally enabled or disabled.

Serial

The R8051 core provides interface for serial communication. The serial port is capable of both synchronous and asynchronous modes. In synchronous mode, the microcontroller generates the clock and operates in a half-duplex mode. In asynchronous mode, full duplex operation is available. Receive data is buffered in a holding register. This allows the serial to receive an incoming word before software has read the previous value.

The port provides four operating modes. These offer different communication protocols and baud rates:

- Synchronous mode, fixed baud rate
- 8-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- 9-bit UART mode, variable baud rate

Ports

The R8051 provides four I/O ports. Port 0 – Port 3 are an 8-bit bi-directional I/O ports with separated inputs and outputs.

The alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051.

Clock_Control

This unit generates the internal synchronous reset signal. It also contains registers for selecting the clock for the timers and for programming the length of the external data memory access.

Performance

The architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most of the 1-byte instructions are performed in a single cycle. The R8051 uses 1 clock per cycle. This leads to performance improvement of rate 8.0 (in terms of MIPS) with respect to the Intel device working with the same clock frequency.

The original Intel 80C51 had a 12-clock architecture. A machine cycle needed 12 clocks and most instructions were either one or two machine cycles. Thus except for the MUL and DIV instructions, the 80C51 used either 12 or 24 clocks for each instruction. Furthermore, each cycle in the 8051 used two memory fetches. In many cases the second fetch was dummy and extra clocks were wasted.

The table below shows the speed advantage of the R8051 over the standard 8051. A speed advantage of 12 means that the R8051 performs the same instruction twelve times faster than the 8051. The average of speed advantage is 8.0. However, the real speed improvement seen in any system will depend on the instruction mix.

Table 3: Core Speed Average

Speed Advantage	Number of Instructions	Number of opcodes
24	1	1
12	27	83
9.6	2	2
8	16	38
6	44	89
4.8	1	2
4	18	31
3	2	9
Average: 8.0	Sum: 111	Sum: 255

Pinout

The pinout of the R8051 core is not fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in Figure 1 and described in Table 3.

Table 4: Core Signal Pinout

Signal	Direction	Description
Ports		
Port0I[7:0] Port0O[7:0]	Input Output	Port 0 Input Bus Port 0 Output Bus
Port1I[7:0] Port1O[7:0]	Input Output	Port 1 Input Bus Port 1 Output Bus
Port2I[7:0] Port2O[7:0]	Input Output	Port 2 Input Bus Port 2 Output Bus
Port3I[7:0] Port3O[7:0]	Input Output	Port 3 Input Bus Port 3 Output Bus
Clock Control		
CLK	Input	Clock Input
RESET	Input	Hardware reset input
Serial Communications Interface		
RXDI	Input	Serial 0 receive data
RXDO	Output	Serial 0 receive clock
TXD	Output	Serial 0 transmit data
Timer and Interrupt		
T0	Input	Timer 0 external input
T1	Input	Timer 1 external input
INT0	Input	External Interrupt 0
INT1	Input	External Interrupt I
Program Memory Interface		
MEMDATAI[7:0]	Input	Memory data input
MEMDATAO[7:0	Output	Memory data output
MEMADDR[15:0]	Output	Memory address
MEMPSWR	Output	Program store write enable
MEMPMSRD	Output	Program store read enable
MEMWR	Output	Data Memory write enable
MEMRD	Output	Data memory read enable

Table 4: Core Signal Pinout (cont.)

Signal	Direction	Description
Data Memory Interface		
RAMDATAI[7:0]	Input	Data bus input
RAMDATAO[7:0]	Output	Output
RAMADDR[7:0]	Output	Data file address
RAMWE	Output	Data file write enable
RAMOE	Input	Data bus input
External SFR Interface		
SFRDATAI[7:0]	Input	SFR data bus input
SFRDATAO[7:0]	Output	SFR data bus output
SFRADDR[6:0]	Output	SFR address
SFRWE	Output	SFR write enable
SFROE	Output	SFR output enable

R8051 Development Environment

The development environment for source code version includes:

- VHDL or Verilog source code for the R8051
- Synthesis support (Synopsys)
- A complete set of synthesis scripts
- Simulation support (Synopsys, MTI, Aldec)
- A set of scripts and macros
- Example CHIP_R8051 – 8051 compatible design
- This design uses the R8051 and illustrates how to build and connect memories and port modules
- Extensive HDL Test Bench that instantiates:
  - Example design CHIP_R8051
  - External RAM
  - External ROM
  - Clock generator
  - Process that compares your simulation results with the expected results
- A collection of 8051 assembler programs which are executed directly by the Test Bench
- A set of expected results
- Additional documentation
  - Architectural overview
  - Hardware description
  - User Guide
- Design support including consulting

Verification Methods

The R8051 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C51 chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from Xilinx AllianceCORE™ partner, CAST, Inc. Please contact CAST, Inc. for pricing and additional information.

The R8051 core is licensed from Evatronix S.A.

Related Information

- CMOS single-chip 8-bit microcontrollers, Phillips, 1996.
- Addendum to the MCS®51 Microcontroller Family, Intel, 1996.
- 8-bit Embedded Controllers, Intel, 1990

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