R14G-LP01 FOUR PORT RJ FORMAT OPTICAL TRANSCEIVER

5.0 Volt, PECL, 1300nM LED for Multimode Optical Fiber at up to 200MBaud

FEATURES

- Four RJ style optical transceivers in a single component
- Optimized for 62.5 or 50/125µ multimode optical fiber
- Compatible with solder and aqueous wash processes
- Enables reuse of exisitng RJ-45 UTP equipment cabinets
- Overall metal shield with enhanced grounding tabs
- Full compliance to the IEEE, ANSI and ATM requirements
- Duplex multimode LC receptacle at each port
- Differential PECL inputs and outputs
- Single +5.0 V power supply per port

ORDERING INFORMATION

Application	Description	Part Number
Fast Ethernet ESCON ATM	100Base-FX X3.296-1997 OC-3	R14G-LP01

APPLICATIONS

The R14G-LP01 multimode glass optical fiber transceivers provide low profile, cost effective solutions for high datarate multimode (up to 200 Megabaud, up to 2 Km) optical fiber data links with four duplex LC connector interfaces.

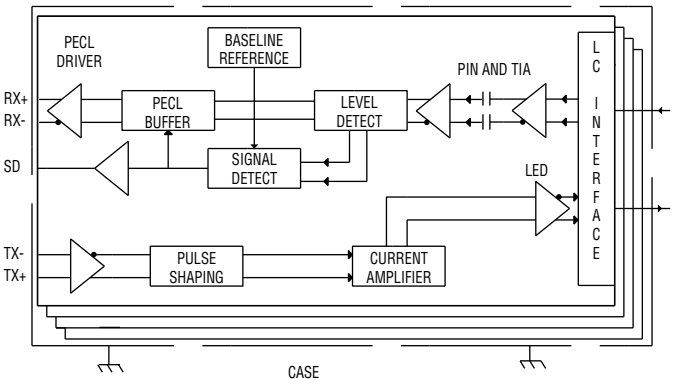
These transceivers are fully compliant with the IEEE, ATM and ANSI standards but can be used for any other data communications purpose within their operating parameters.

DESCRIPTION

The R14G-LP01 fiber optic transceivers consist of transmitter and receiver functions combined in a four port RJ Format “harmonica” module. The optical transmitters are high ouput 1300nM LED’s. The transmitter input lines are driven with differential PECL signals applied to the Transmit **(TX+ and TX-)** pins. These signals are internally converted to a suitable modulation current by a CMOS integrated circuit.

The optical receivers consist of PIN and Preamplifier assemblies and CMOS limiting post-amplifier integrated circuits. Outputs from the receivers consist of differential PECL data signals on the Receive **(RX+ and RX-)** pins and single ended PECL signal detect functions on the Signal Detect **(SD)** pins.

BLOCK DIAGRAM



METHODE ELECTRONICS, INC.

Methode Communication Modules

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Telephone: 321-308-4100 Fax: 321-308-0434
Web Page: www.methode.com

ABSOLUTE MAXIMUM RATINGS

Absolute maximum limits mean that no catastrophic damage will occur if the product is subjected to these ratings for short periods, provided each limiting parameter is in isolation and all other parameters have values within the performance specification. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time.

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Storage Temperature	T_S	-55		+100	° C
Lead Soldering Temperature	T_{SOLD}			+260	° C
Lead Soldering Time	t_{SOLD}			10	Seconds
Supply Voltage	V_{CC}	-0.5		6.0	V
Data Input Voltage	V_I	-0.5		V_{CC}	V
Differential Input Voltage (p-p)	V_D			2.0	V
Output Current	I_O			50	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temp. Limit - R14G-LP11	T_A	0		+70	° C
Supply Voltage	V_{CC}	4.75		5.25	V
Data Input Voltage - Low	V_{IL} - V_{CC}	-1.810		-1.475	V
Data Input Voltage - High	V_{IH} - V_{CC}	-1.165		-0.880	V
Data Output Load	R_L		50		Ohms
Differential Input Voltage (p-p)	V_D	0.800			V

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TRANSMITTERS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Baud Rate		10		200	MBaud
Optical Output Power	P_O	-19		-14	dBm
Optical Output Wavelength	λ_{OUT}	1270	1320	1380	nm
Extinction Ratio	ER		-47	-40	dB
Optical Rise Time (10%-90%)	t_R	0.6	1.5	3.0	nS
Optical Fall Time (10%-90%)	t_F	0.6	2.0	3.0	nS
Duty Cycle Distortion	t_{DCD}		<0.1	0.6	nS
Data Dependent Jitter	t_{DDJ}		<0.1	0.7	nS

RECEIVERS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Baud Rate		10		200	MBaud
Optical Wavelength	λ_{IN}	1270		1380	nm
Optical Sensitivity	P_I		-35	-32	dBm
Input Duty Cycle Distortion	t_{DCD}			1.0	nS
Input Data Dependent Jitter	t_{DDJ}			0.76	nS
Signal Detect Assert Time			<10	100	µS
Signal Detect Deassert Time			<10	350	µS

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REGULATORY COMPLIANCE

Requirement	Feature	Condition	Notes
MIL-STD-883-3015.7	ESD	Class II	2200V
IEC-801-2	ESD	Human Body Model	25KV
IEC-801-3	EMI	Immunity	>20dB
FCC	EMI	Class B	10V / M
EN 55022 (CISPR 22A)	EMI	Class B	>20dB
IEC-825 issue 1993-11	Eye Safety	Class 1	

c US

UL / CSA File Number: E209124

EN 60 950
EN 60 825-1
EN 60 825-2

TUV File Number: R2071012

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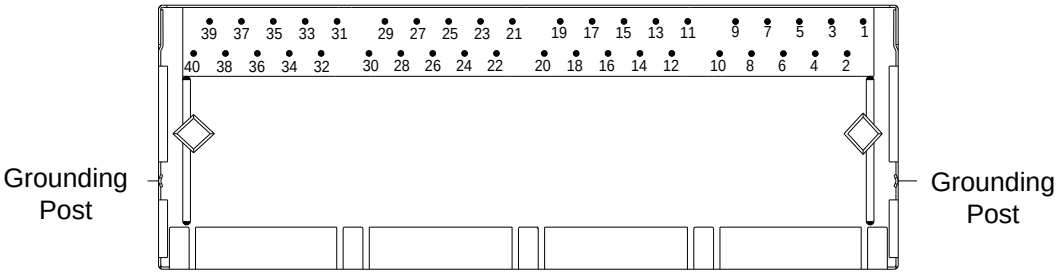
PIN NUMBER ASSIGNMENTS

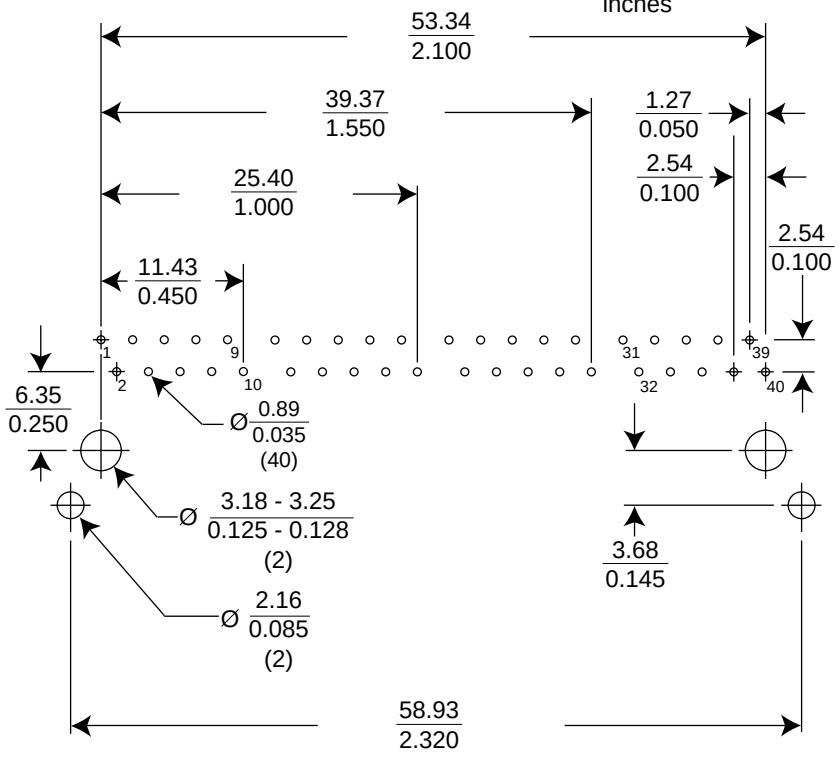
Bottom View of Component



RECOMMENDED PCB HOLE LAYOUT

PCB Component Side View

Dimensions Are Shown As: mm / inches



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PIN FUNCTIONS

Pin Number	Symbol	Description	Logic Family
GP	GP	Grounding Post *Connect to Chassis Ground*	N/A
1, 11, 21, 31	TD+	Transmitter DATA In	PECL
2, 12, 22, 32	VEETX	Transmitter Signal Ground	N/A
3, 13, 23, 33	TD–	Transmitter DATA In	PECL
4, 14, 24, 34	VCCTX	Transmitter Power Supply	N/A
5, 15, 25, 35	SD	Signal Detect *Normal Operation: Logic "1" Output* *Fault Condition: Logic "0" Output*	PECL
6, 16, 26, 36	N/C	No Connection	N/A
7, 17, 27, 37	RD–	Receiver DATA Out	PECL
8, 18, 28, 38	VCCRX	Receiver Power Supply	N/A
9, 19, 29, 39	RD+	Receiver DATA Out	PECL
10, 20, 30, 40	VEERX	Receiver Signal Ground	N/A

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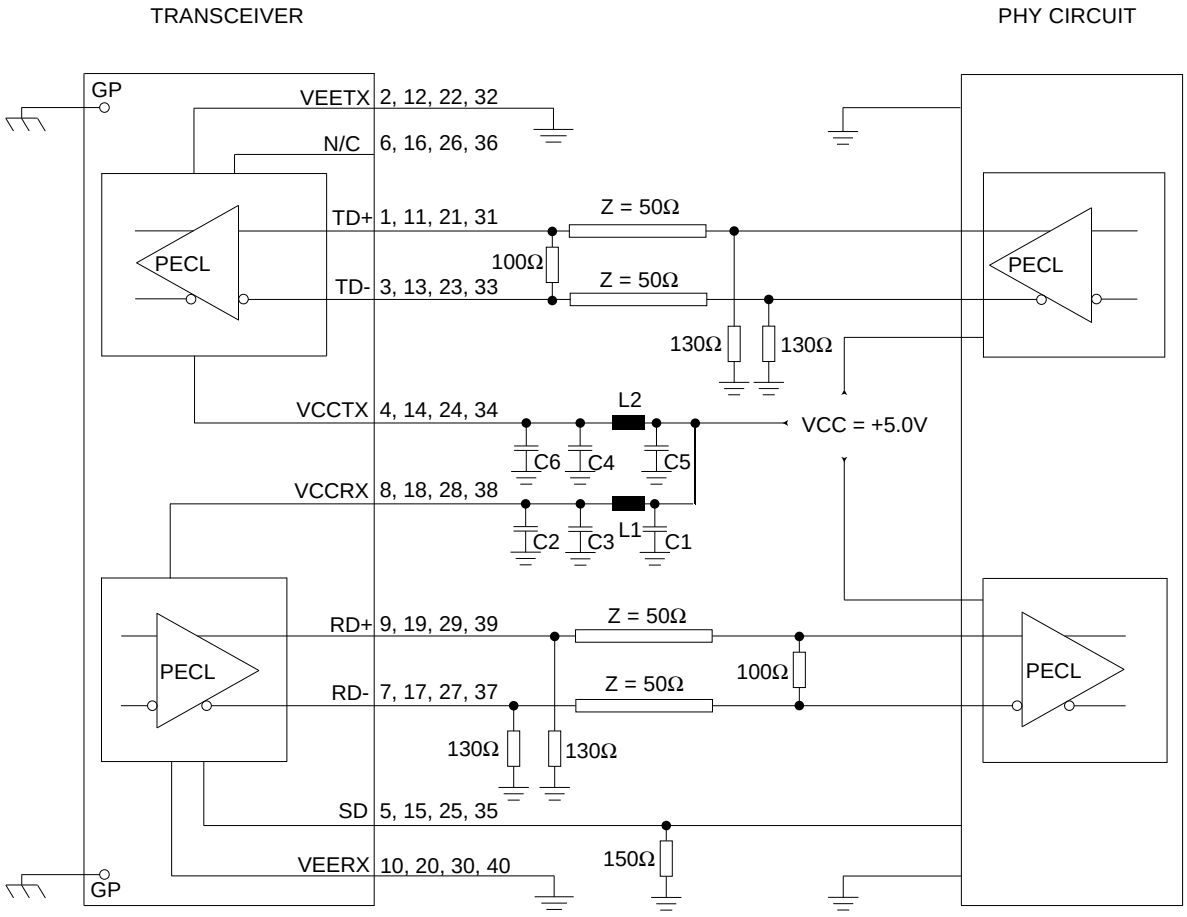
TRANSCEIVER APPLICATION SCHEMATIC
For Interface To +5.0V PECL Circuits



L1, L2 = 1mH to 4.7mH*
C1, C2, C6 = 10nF**
C3, C4, C5 = 4.7mF to 10mF**
* Or ferrite bead alternative
** MLC capacitors

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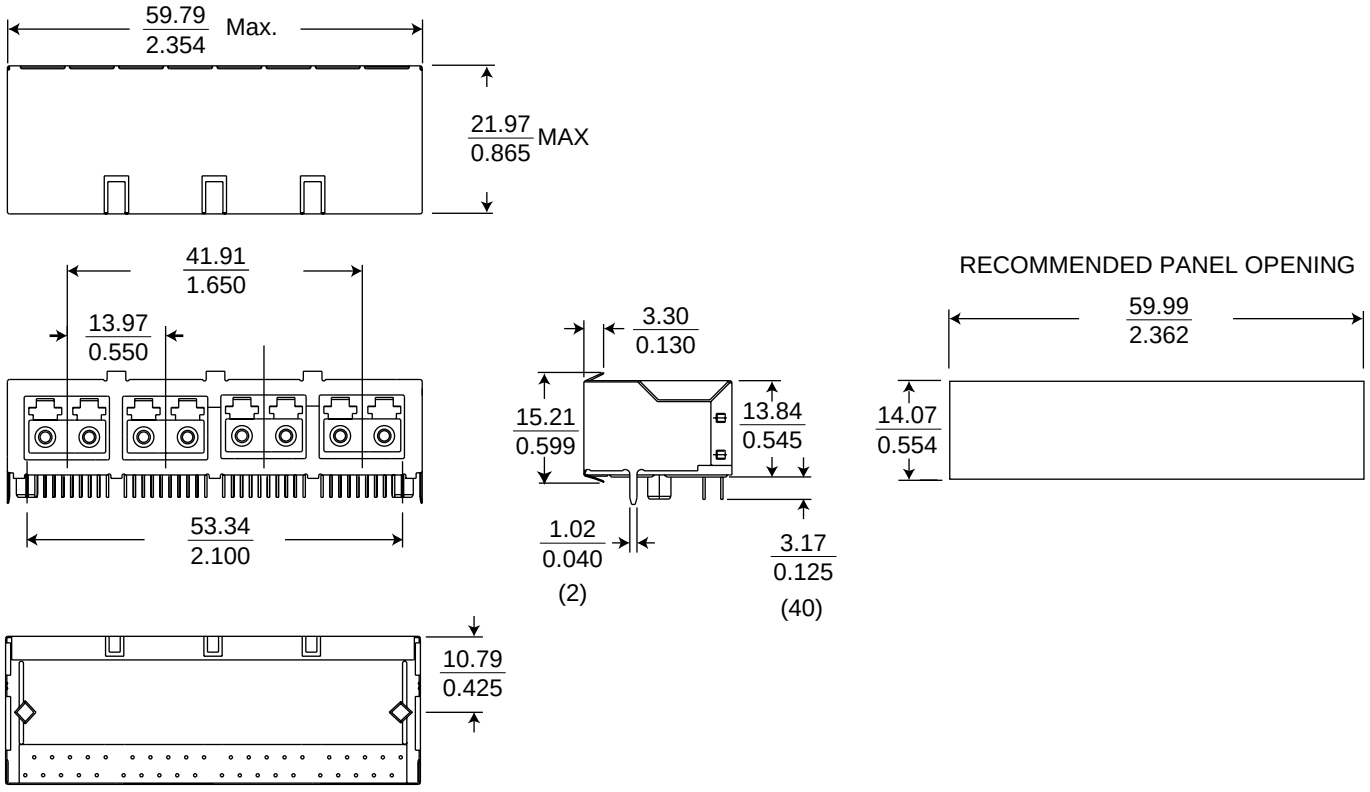
TRANSCEIVER OUTLINE DRAWING

Dimensions Shown As: mm / inches



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