BURR - BROWN®

PCM1726

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER 16 Bits, 96kHz Sampling

FEATURES

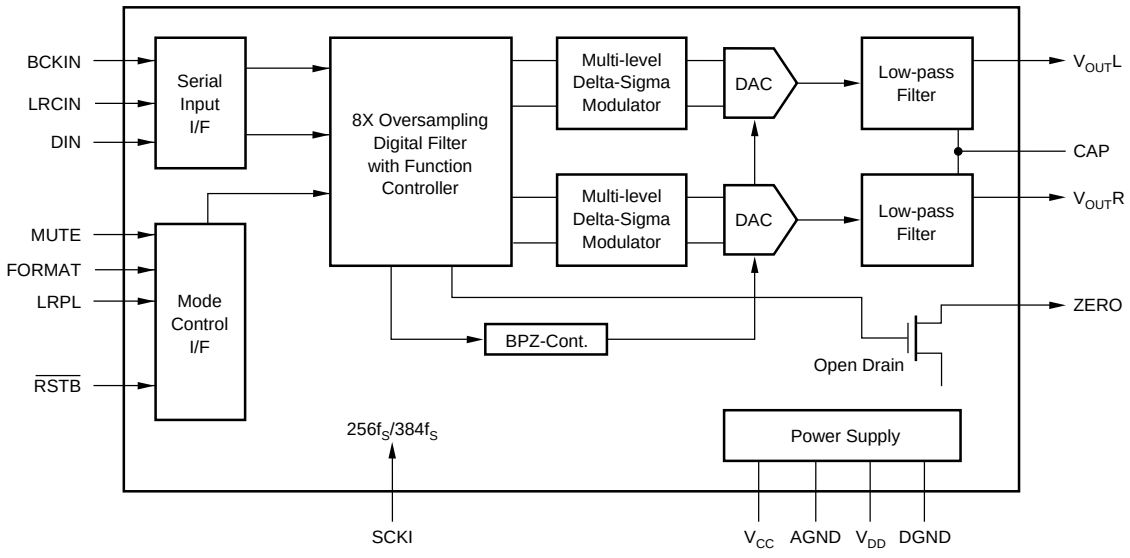
- **COMPLETE STEREO DAC: Includes Digital Filter and Output Amp**
- **DYNAMIC RANGE: 96dB**
- **MULTIPLE SAMPLING FREQUENCIES: 16kHz to 96kHz 8X Oversampling at All Sampling Frequencies**
- **SYSTEM CLOCK: $256f_S/384f_S$**
- **NORMAL OR I^2S DATA INPUT FORMATS**
- **SOFT MUTE**

DESCRIPTION

The PCM1726 is a complete low cost stereo audio digital-to-analog converter (DAC), operating off of a $256f_S$ or $384f_S$ system clock. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1726 accepts 16-bit input data in either normal or I^2S formats.

The digital filter performs an 8X interpolation function and includes soft mute. The PCM1726 can accept standard digital audio sampling frequencies as well as one-half and double sampling frequencies.

The PCM1726 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.



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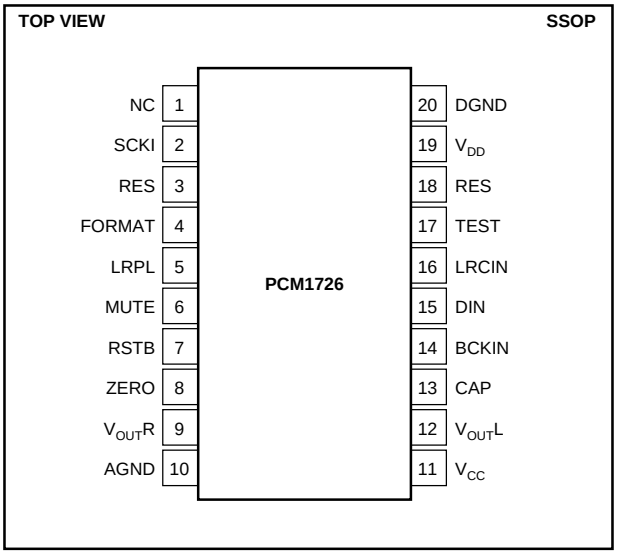
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 16-bit input data, SYSCLK = 384f_S, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1726 MIN	PCM1726 TYP	PCM1726 MAX	UNITS
RESOLUTION				16	Bits
DATA FORMAT					
Audio Data Format			Standard / I^2S		
Data Bit Length			16		
Sampling Frequency (f_S)		16		96	kHz
Internal System Clock Frequency			256f_S/384f_S		
DIGITAL INPUT/OUTPUT LOGIC LEVEL			TTL		
DYNAMIC PERFORMANCE(1)					
THD+N at f_S (0dB)	f_S = 44.1kHz		–90	–80	dB
	f_S = 96kHz		–88		dB
THD+N at –60dB	f_S = 44.1kHz		–34		dB
	f_S = 96kHz		–31		dB
Dynamic Range	f_S = 44.1kHz	90	96		dB
	f_S = 96kHz		93		dB
Signal-to-Noise Ratio(2)	f_S = 44.1kHz	92	100		dB
	f_S = 96kHz		97		dB
Channel Separation	f_S = 44.1kHz	90	97		dB
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	V_{OUT} = V_{CC}/2 at BPZ		±30		mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		0.62 x V_{CC}		Vp-p
Center Voltage			V_{CC}/2		VDC
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Passband				0.445	f_S
Stopband		0.555			f_S
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			11.125/f_S		sec
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}	4.5	5	5.5	VDC
Supply Current: I_{CC} + I_{DD}	V_{CC} = V_{DD} = 5V, f_S = 44.1kHz		18	25	mA
	V_{CC} = V_{DD} = 5V, f_S = 96kHz		25	35	mA
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (2) SNR is tested with Infinite Zero Detection off.

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1726E	20-Pin SSOP	334-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Power Dissipation	300mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

PIN ASSIGNMENTS

PIN	NAME	TYPE	FUNCTION
1	NC	—	No Connection.
2	SCKI	IN	System Clock Input: 256f_S or 384f_S.
3	RES	—	Reserved for Factory Use. Do not connect.
4(1)	FORMAT	IN	Input Data Format Control.
5(1)	LRPL	IN	Left/Right Polarity Control.
6(1)	MUTE	IN	Soft Mute Control.
7(1)	RSTB	IN	Reset Input. When this pin is low, the digital filters and modulators are held in reset.
8	ZERO	OUT	Zero Data Flag. This pin is low when the data is continuously zero for more than 65,535 cycles of BCKIN.
9	V_{OUT}R	OUT	Right Channel Analog Output.
10	AGND	PWR	Analog Ground.
11	V_{CC}	PWR	Analog Power Supply (+5V).
12	V_{OUT}L	OUT	Left Channel Analog Output.
13	CAP	—	Common Pin for Analog Output Amplifiers.
14(1)	BCKIN	IN	Bit Clock for Clocking in the Audio Data.
15(1)	DIN	IN	Serial Audio Data Input.
16(1)	LRCIN	IN	Left/Right Word Clock. Frequency is equal to f_S.
17	TEST	—	Must be Tied to Ground.
18	RES	—	Do Not Connect.
19	V_{DD}	PWR	Digital Power Supply (+5V). Recommended connection is to the analog power supply.
20	DGND	PWR	Digital Ground. Recommended connection is to the digital ground plane.

NOTE: (1) These pins include internal pull-up resistors.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

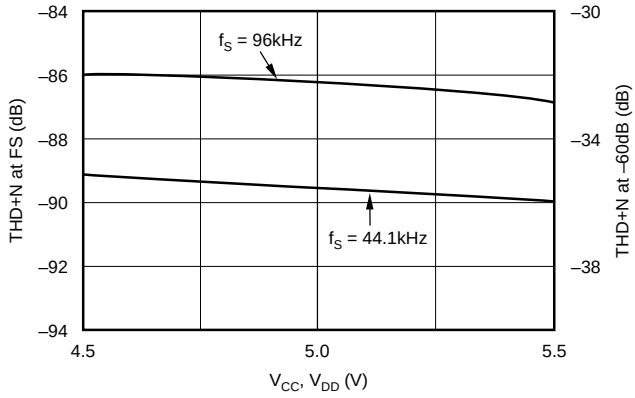
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL PERFORMANCE CURVES

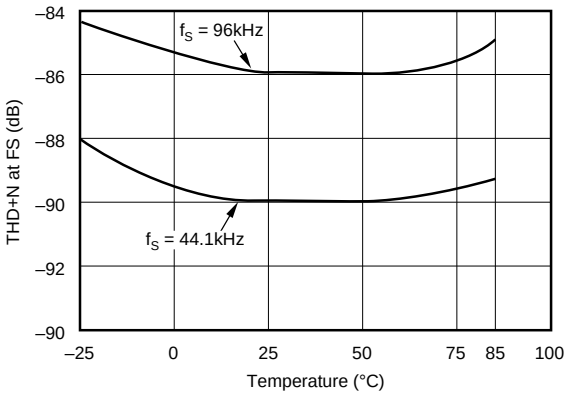
DYNAMIC PERFORMANCE

At T_A = +25°C, V_{CC} = V_{DD} = +5V, f_S = 44.1kHz, 16-bit input data, unless otherwise noted. Measurement bandwidth is 20kHz.

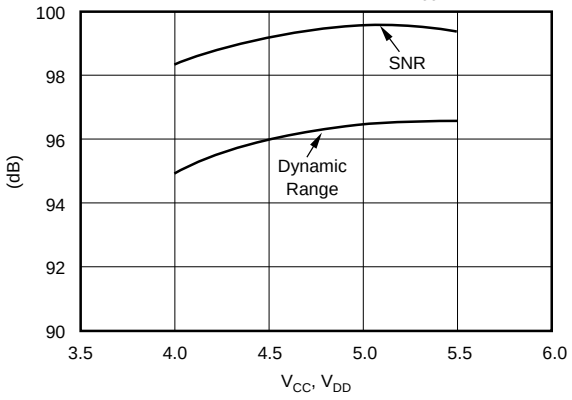
THD+N vs V_{CC}, V_{DD}



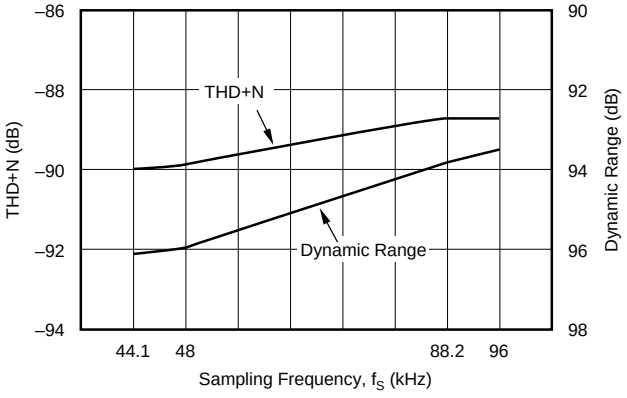
THD+N vs TEMPERATURE



DYNAMIC RANGE and SNR vs V_{CC}, V_{DD}



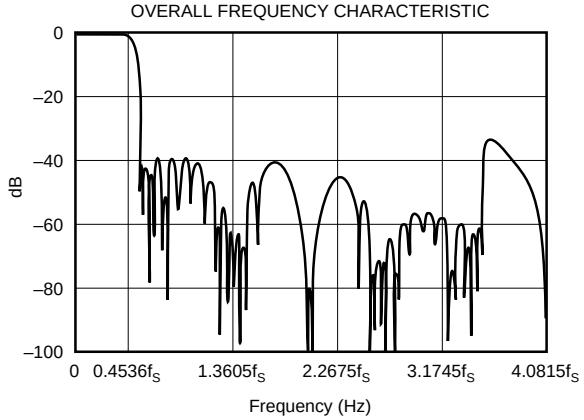
THD+N and DYNAMIC RANGE vs f_S



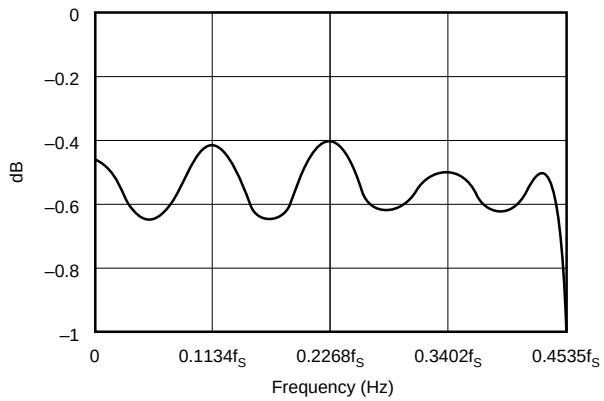
DIGITAL FILTER

At T_A = +25°C, V_{CC} = V_{DD} = +5V, f_S = 44.1kHz, f_{SYS} = 384f_S, and 16-bit input data, unless otherwise noted.

OVERALL FREQUENCY CHARACTERISTIC



PASSBAND RIPPLE CHARACTERISTIC



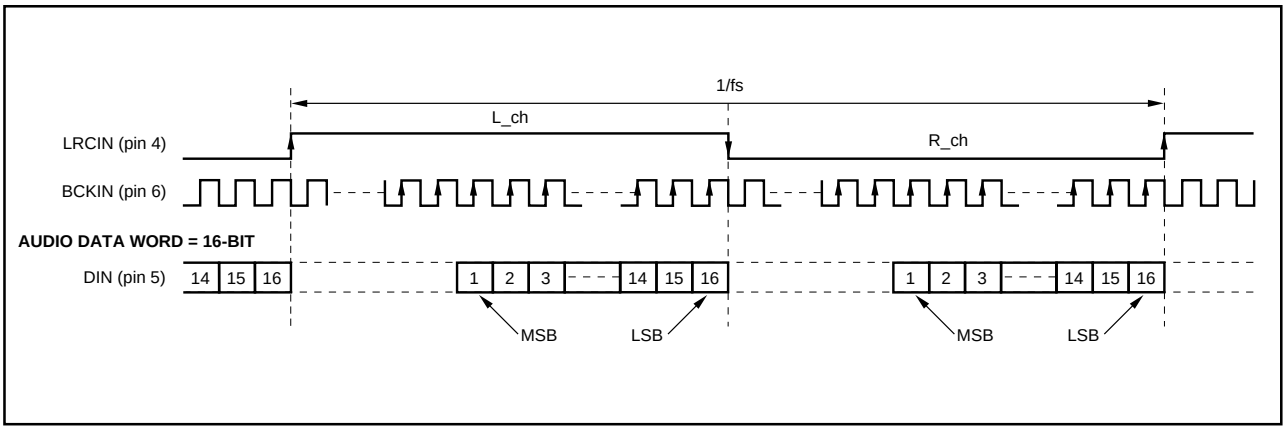


FIGURE 1. “Normal” Data Input Timing.

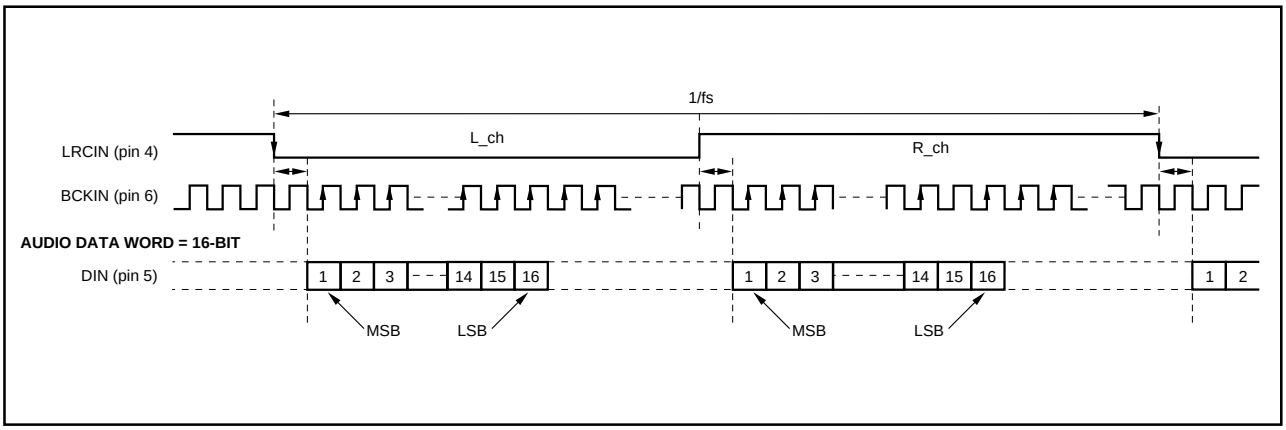
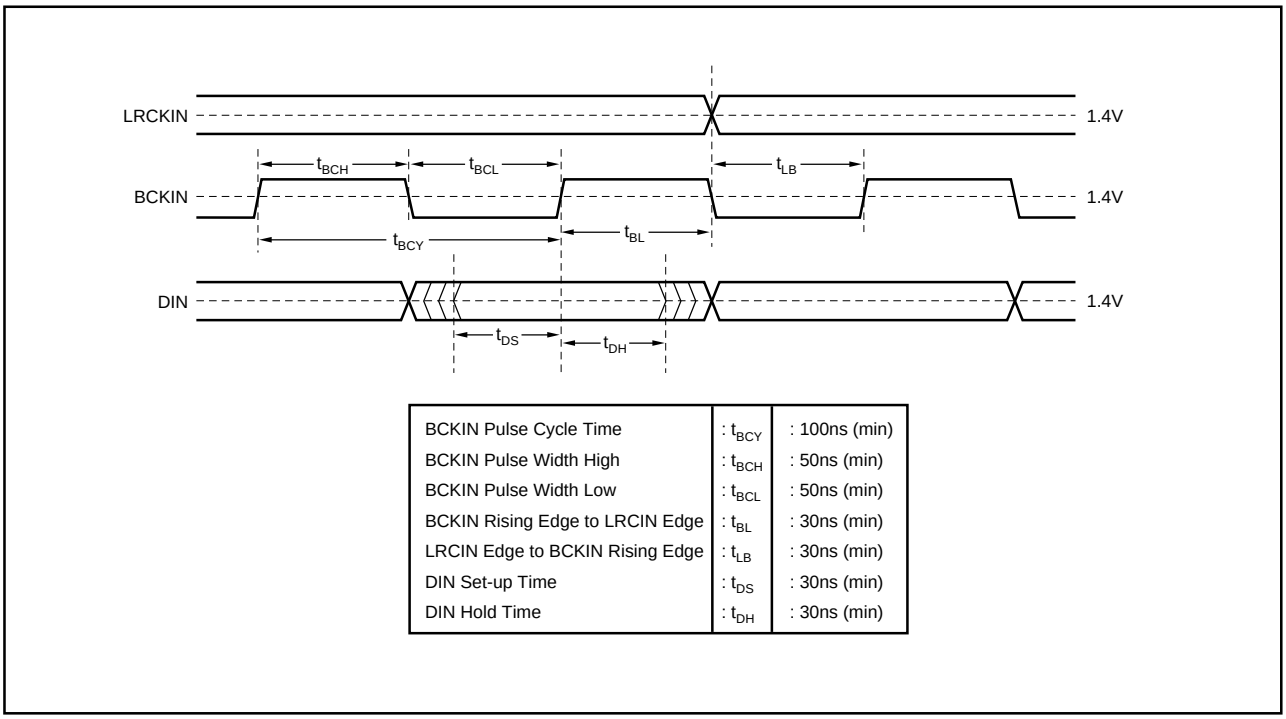


FIGURE 2. “I²S” Data Input Timing.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width High	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width Low	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 3. Audio Data Input Timing.

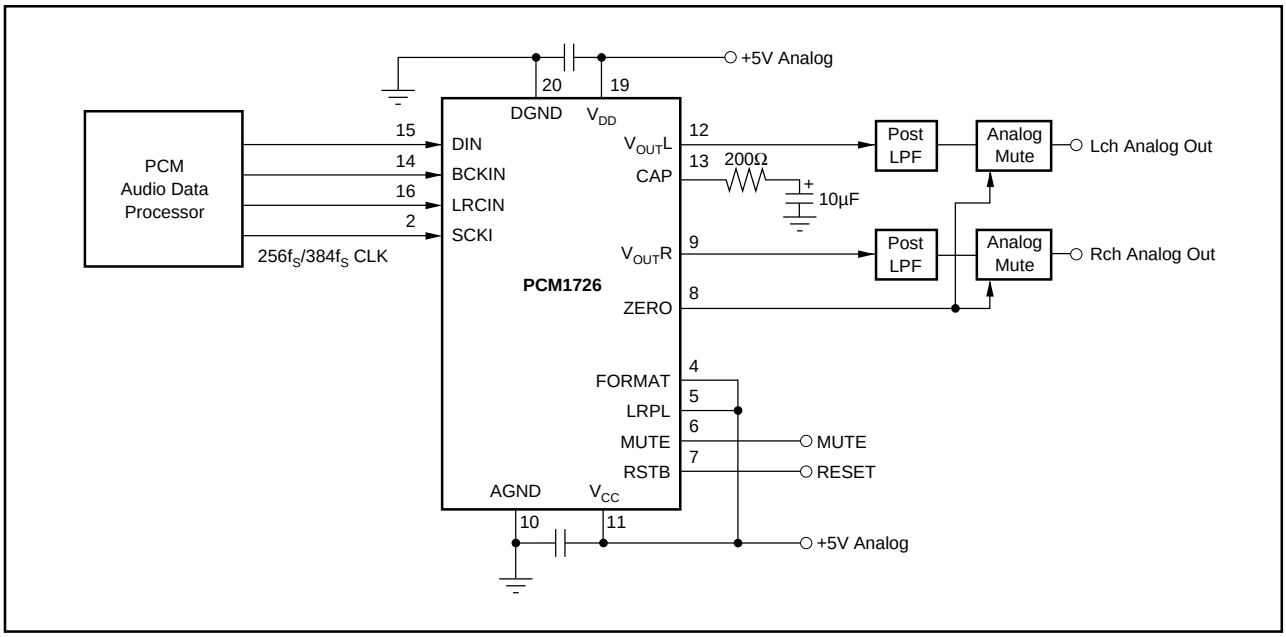


FIGURE 4. Typical Connection Diagram For I²S Data Format.

TYPICAL CONNECTION DIAGRAM

Figure 4 illustrates the typical connection diagram for PCM1726 used in a stand-alone application.

SYSTEM CLOCK

The system clock for PCM1726 must be either 256f_S or 384f_S, where f_S is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz or 48kHz. The system clock is used to operate the digital filter and the noise shaper. The system clock input (SCKI) is at pin 2.

PCM1726 has a system clock detection circuit which automatically detects the frequency, either 256f_S or 384f_S. The system clock should be synchronized with LRCIN (pin 16), but PCM1726 can compensate for phase differences. If the phase difference between LRCIN and system clock is greater than ±6 bit clocks (BCKIN), the synchronization is performed automatically. The analog outputs are forced to a bipolar zero state (V_{CC}/2) during the synchronization function. Table I shows the typical system clock frequency inputs for the PCM1726.

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHz)	
	256f_S	384f_S
32kHz	8.192	12.288
44.1kHz	11.2896	16.9340
48kHz	12.288	18.432

TABLE I. System Clock Frequencies vs Sampling Rate.

INPUT DATA FORMAT

PCM1726 can accept input data in either normal (MSB-first, right-justified) or I²S formats. When pin 4 (FORMAT) is LOW, normal data format is selected; a HIGH on pin 4 selects I²S format.

FORMAT	
0	Normal Format (MSB-first, right-justified)
1	I²S Format (Philips serial data protocol)

TABLE II. Input Format Selection.

SOFT MUTE

The outputs of the PCM1726 can be muted by taking pin 6 (MUTE) to a LOW state. This pin has an internal pull-up resistor and may be left open for non-muted operation of the DAC.

MUTE	
0	Soft Mute ON
1	Soft Mute OFF

TABLE III. Soft Mute Enable.

WORD POLARITY

The polarity of the input data word (LRCIN) may be controlled by pin 5 (LRPL). A LOW on pin 5 interprets the HIGH portion on LRCIN as left-channel data, and the LOW portion of LRCIN as right-channel data. Taking pin 5 HIGH reverses the polarity.

LRPL	LRCIN VALUE
0	Left-Channel is HIGH; Right-Channel is LOW
1	Left-Channel is LOW; Right-Channel is HIGH

TABLE IV. Left/Right Polarity Selection.

RESET

PCM1726 has an internal power-on reset circuit, as well as an external forced reset (RSTB, pin 7). The internal power-on reset initializes (resets) when the supply voltage V_{DD} > 4.0V (typ). External forced reset occurs when RSTB = LOW and the outputs of the DAC are at $V_{CC}/2$. The power-on reset has an initialization period equal to 1024 system clock periods after V_{DD} > 4.0V and RSTB = HIGH. During the initialization period, the outputs of the DAC are invalid, and the analog outputs are forced to $V_{CC}/2$. Figures 5 and 6 illustrate the power-on reset and reset-pin reset timing.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1726:

$$T_D = 11.125 \times 1/f_S$$

For f_S = 44.1kHz, T_D = 11.125/44.1kHz = 251.4µs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1726 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

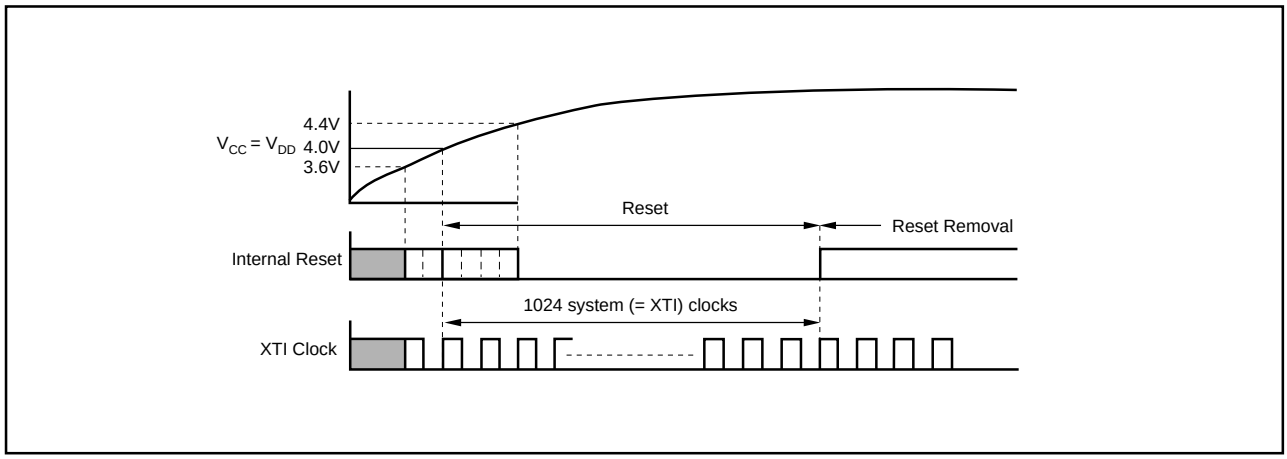


FIGURE 5. Internal Power-On Reset Timing.

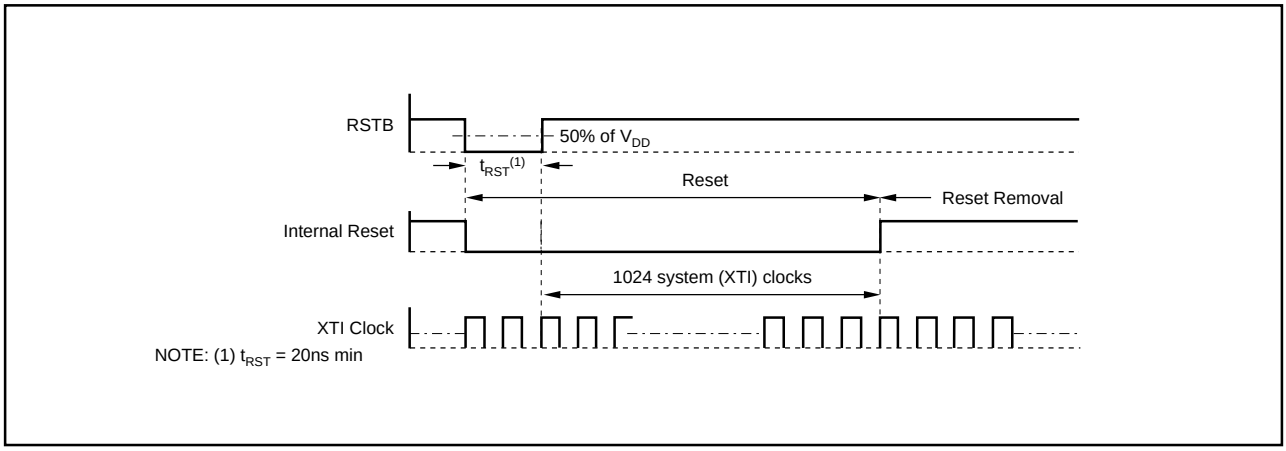


FIGURE 6. External Forced Reset Timing.

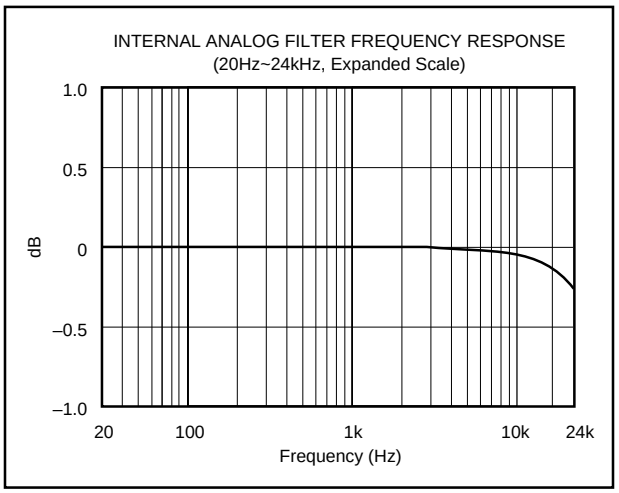


FIGURE 7. Low Pass Filter Frequency Response.

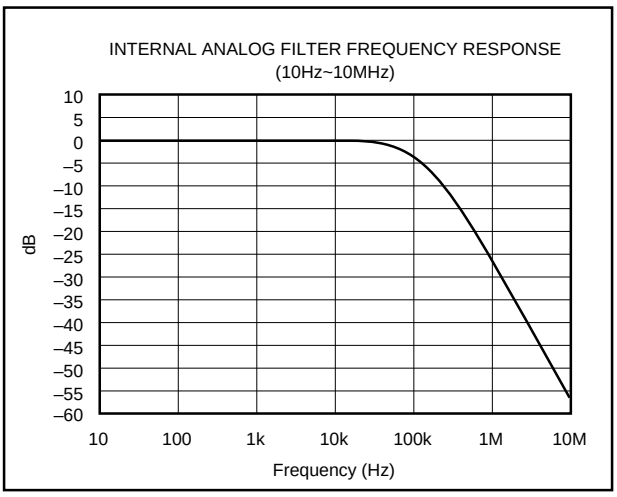


FIGURE 8. Low Pass Filter Wideband Frequency Response.

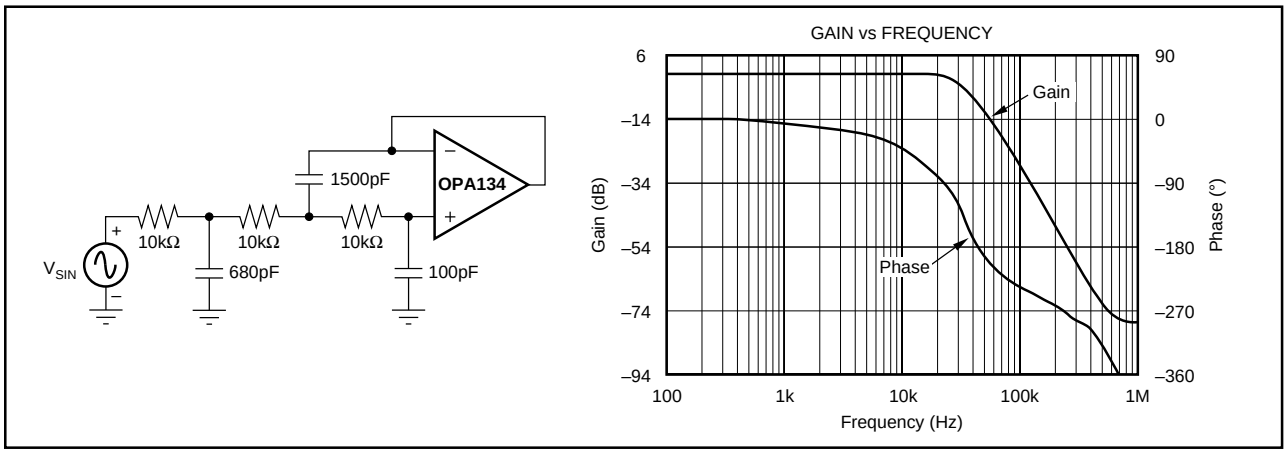


FIGURE 9. 3rd-Order LPF.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 7. The higher frequency rolloff of the filter is shown in Figure 8. If the user's application has the PCM1726 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 9. For some applications, a passive RC filter or 2nd-order filter may be adequate.

POWER SUPPLY CONNECTIONS

PCM1726 has two power supply connections: digital (V_{DD}) and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.6V.

An application circuit to avoid a latch-up condition is shown in Figure 10.

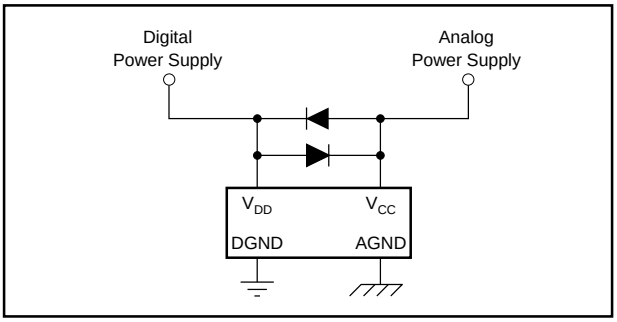


FIGURE 10. Latch-up Prevention Circuit.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. It is also recommended to include a 0.1µF ceramic capacitor in parallel with the 10µF tantalum bypass capacitor.

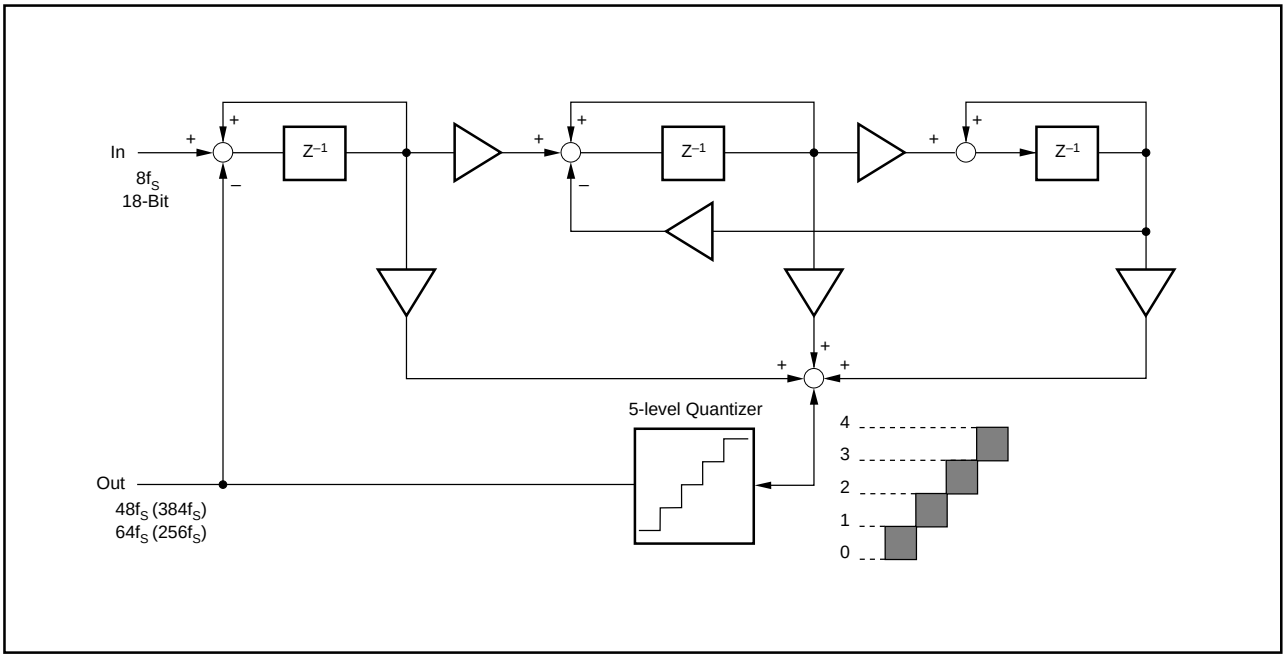
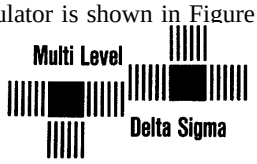


FIGURE 11. 5-Level ΔΣ Modulator Block Diagram.

THEORY OF OPERATION

The delta-sigma section of PCM1726 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 11. This 5-level delta-sigma modulator has the advantage of stability and clock jitter over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $48f_S$ for a $384f_S$ system clock, and $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 12.



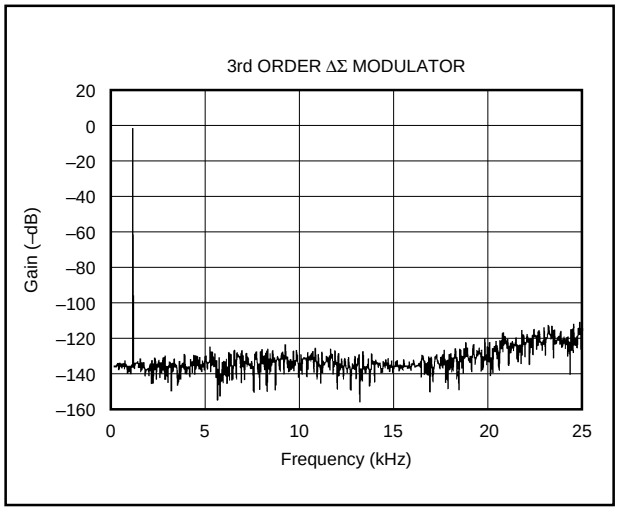


FIGURE 12. Quantization Noise Spectrum.