Intel® Pentium® 4 Processor in the 423-pin Package at 1.30 GHz, 1.40 GHz, and 1.50 GHz

Datasheet

Product Features

- Available at 1.30, 1.40, and 1.50 GHz
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel® NetBurst™ micro-architecture
- System bus frequency at 400 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advance Dynamic Execution
  - —Very deep out-of-order execution
  - —Enhanced branch prediction
- Level 1 Execution Trace Cache stores 12K micro-ops and removes decoder latency from main execution loops
- 8KB Level 1 data cache
- 256 KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 144 new Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 8-way cache associativity provides improved cache hit rate on reads/store operations.

The Intel® Pentium® 4 processor is designed for high-performance desktops and entry level workstations. It is binary compatible with previous Intel Architecture processors. The Pentium 4 processor provides great performance for applications running on advanced operating systems such as Windows* 98, Windows ME, Windows 2000 and UNIX*. This is achieved by the Intel® NetBurst™ micro-architecture which brings a new level of performance for system buyers. The Pentium 4 processor extends the power of the Pentium III processor with performance headroom for advanced audio and video internet capabilities. Systems based on Pentium 4 processors also include the latest features to simplify system management and lower the total cost of ownership for large and small business environments. The Pentium 4 processor offers great performance for today's and tomorrow's applications.

Order Number: 249198-002
January 2001

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1.0 Introduction

The Intel® Pentium® 4 Processor in the 423-pin Package socket with Intel® NetBurst™ micro-architechture is based on a new 32-bit micro-architecture that operates at significantly higher clock speeds and delivers performance levels that are significantly higher than previous generations of IA-32 processors. While based on the Intel® NetBurst™ micro-architecture, it still maintains the tradition of compatibility with IA-32 software. The Intel NetBurst micro-architecture features include hyper pipelined technology, a rapid execution engine, a 400 MHz system bus, and an execution trace cache. The hyper pipelined technology doubles the pipeline depth in the Pentium 4 processor, allowing the processor to reach much higher core frequencies. The rapid execution engine allows the two integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 400 MHz system bus is a quad-pumped bus running off a 100 MHz system clock making 3.2 GB/sec data transfer rates possible. The execution trace cache is a level 1 cache that stores approximately 12k decoded micro-operations, which removes the decoder from the main execution path, thereby increasing performance.

Improved features within the Intel NetBurst micro-architecture include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 256kB, on-die level 2 cache with increased bandwidth over previous micro-architectures. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management.

The Streaming SIMD Extensions 2 enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques, such as ray tracing.

The Pentium 4 processor supports uni-processor configurations only. As a result of this integration, the return to Pin Grid Array (PGA) style processor packaging is possible. The same manageability features which are included in Intel® Pentium® III processors are included on Pentium 4 processors with the addition of Thermal Monitor. The Thermal Monitor allows systems to be designed for anticipated processor thermals as opposed to worst case with no performance degradation expected. Power management capabilities such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep have also been retained for power management capabilities.

New heat sinks, heat sink retention mechanisms, and sockets are required for the Pentium 4 processor in the 423-pin package. The socket for the Pentium 4 processor in the 423-pin package is called the 423-Pin Socket in this and other documentation. Through-hole ZIF technology will be used for the 423-Pin Socket. Reference heat sink and retention mechanism designs have been developed with manufacturability as a high priority. Hence, mechanical assembly can be completed from the top of the motherboard and should not require any special tooling.

The Pentium 4 processor in the 423-pin package uses a new scalable system bus protocol referred to as the “system bus” in this document. The Pentium 4 processor system bus utilizes a split-transaction, deferred reply protocol similar to that of the P6 processor family system bus, but is not compatible with the P6 processor family system bus. The system bus uses Source-Synchronous Transfer (SST) of address and data to improve performance. Whereas the P6 processor family transfers data once per bus clock, the Pentium 4 processor transfers data four times per bus clock

(4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a ‘double-clocked’ or 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 3.2 Gbytes/second (3200Mbytes/sec). Finally, the system bus also introduces transactions that are used to deliver interrupts.

Signals on the system bus use Assisted GTL+ (AGTL+) level voltages which are fully described in the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide*.

1.1 Terminology

A ‘#’ symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the ‘#’ symbol implies that the signal is inverted. For example, D[3:0] = ‘HLHL’ refers to a hex ‘A’, and D[3:0]# = ‘LHLH’ also refers to a hex ‘A’ (H= High logic level, L= Low logic level).

“System bus” refers to the interface between the processor and system core logic (a.k.a. the chipset components). The system bus is a interface to the processor, memory, and I/O. For this document, “system bus” is used as the generic term for the Pentium 4 processor bus.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- Intel® Pentium® 4 Processor in the 423-pin Package—The entire product including processor core, integrated heat spreader, and interposer.
- Pentium 4 processor—Throughout this document “Pentium 4 processor” refers to the Intel® Pentium® 4 Processor in the 423-pin Package.
- **Interposer** —The structure on which the processor core package and I/O pins are mounted.
- **Processor core** —The processor’s execution engine. All AC timings and signal integrity specifications are to the silicon of the processor core.
- **Integrated heat spreader** —The surface used to make contact between a heatsink or other thermal solution and the processor. Abbreviated as IHS.
- **423-Pin Socket** —The connector which mates the Pentium 4 processor to the system board.
- **Retention mechanism** —The support structure that is mounted on the system board to provide added support and retention for heatsinks.
- **OLGA (Organic Land Grid Array) Package** —Microprocessor packaging using “flip chip” design, where the processor is attached to the substrate face-down for better signal integrity, more efficient heat removal and lower inductance.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1. References

Document	Order Number[1]
Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide	
AP-485, *Intel Processor Identification and the CPUID Instruction*	Order Number 241618
Intel® Pentium® 4 Processor Thermal Design Guidelines	
Intel® Pentium® 4 Processor EMI Guidelines	
Voltage Regulator Module (VRM) 9.0 DC-DC Converter Design Guidelines	
423-Pin Socket (PGA423) Design Guidelines	
Intel Architecture Software Developer's Manual	Order Number 243193
Volume I: Basic Architecture	Order Number 243190
Volume II: Instruction Set Reference	Order Number 243191
Volume III: System Programming Guide	Order Number 243192
Intel® Pentium® 4 Processor I/O Buffer Models[2]	
Intel® Pentium® 4 Processor Overshoot Checker Tool[2]	

Note:

1. Contact your Intel representative for the latest revision of the documents without order numbers.
2. The I/O Buffer Models are in IBIS format.

2.0 Electrical Specifications

2.1 System Bus and GTLREF

Most system bus signals of the Intel® Pentium® 4 Processor in the 423-pin Package system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signalling technology. As with the Intel P6 family of microprocessors, this signalling technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Unlike the P6 processor family, the termination voltage level for the Pentium 4 processor AGTL+ signals is V_{CC}, the operating voltage of the processor core. P6 family processors utilize a fixed 1.5V termination voltage known as V_{TT}. Because of the speed improvements to data and address busses, signal integrity and platform design methods become more critical than with previous processor families. Design guidelines for the Pentium 4 processor system bus are detailed in the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide*.

The AGTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board (See Table 13 for GTLREF specifications). Termination resistors are provided on the processor silicon and are terminated to its core voltage (V_{CC}). Intel chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most AGTL+ signals.

Some AGTL+ signals do not include on-die termination and must be terminated on the system board. See Table 4 for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system. Contact your Intel Field Representative to obtain the buffer models, *Intel® Pentium® 4 Processor I/O Buffer Models.*

2.2 Power and Ground Pins

For clean on-chip power distribution, Pentium 4 processors have 111 V_{CC} (power) and 112 V_{SS} (ground) inputs. All power pins must be connected to V_{CC}, while all V_{SS} pins must be connected to a system ground plane.The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 5. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and design guidelines, refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide.*

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator (or VRM pins) to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, must be provided by the voltage regulator solution (VRM). For more details on this topic, refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide*.

2.3.2 System Bus AGTL+ Decoupling

Pentium 4 processors integrate signal termination on the die as well as incorporate high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation. For more information, refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide*.

2.3.3 System Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the system bus interface speed as well as the core frequency of the processor. As in previous generation processors, the Pentium 4 processor core frequency is a multiple of the BCLK[1:0] frequency. The Pentium 4 processor bus ratio multiplier is set at its default ratio at manufacturing. No jumpers or user intervention is necessary, the processor will automatically run at the speed indicated on the package.

Unlike previous processors, the Pentium 4 processor uses a differential clocking implementation. For more information on Pentium 4 processor clocking, refer to the *CK00 Clock Synthesizer/Driver Design Guidelines.*

2.4 Voltage Identification

The VID specification for Pentium 4 processors is different from that of previous generations and is supported by the *VRM 9.0 DC-DC Convertor Design Guidelines*. The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in Table 5 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

Pentium 4 processors use five voltage identification pins, VID[4:0], to support automatic selection of power supply voltages. Table 2 specifies the voltage level corresponding to the state of VID[4:0]. A ‘1’ in this table refers to an open pin and a ‘0’ refers to low voltage level. The definition provided in Table 2 is not related in any way to previous processors or VRMs. If the processor socket is empty (VID[4:0] = 11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the *VRM 9.0 DC/DC Converter Design Guidelines* for more details.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2. Voltage Identification Definition

Processor Pins					
VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

2.4.1 Phase Lock Loop (PLL) Power and Filter

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Pentium 4 processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}. A typical filter topology is shown in Figure 1.

The AC low-pass requirements, with input at V_{CC} and output measured across the capacitor (C_A or C_{IO} in Figure 1), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2. For recommendations on implementing the filter refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide*.

Figure 1. Typical $V_{CCIOPLL}$, V_{CCA} and V_{SSA} Power Distribution

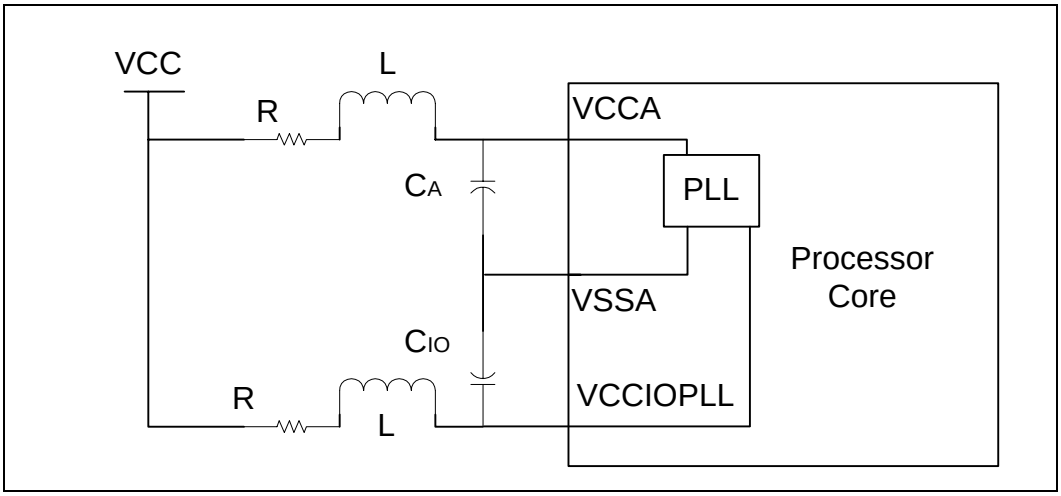
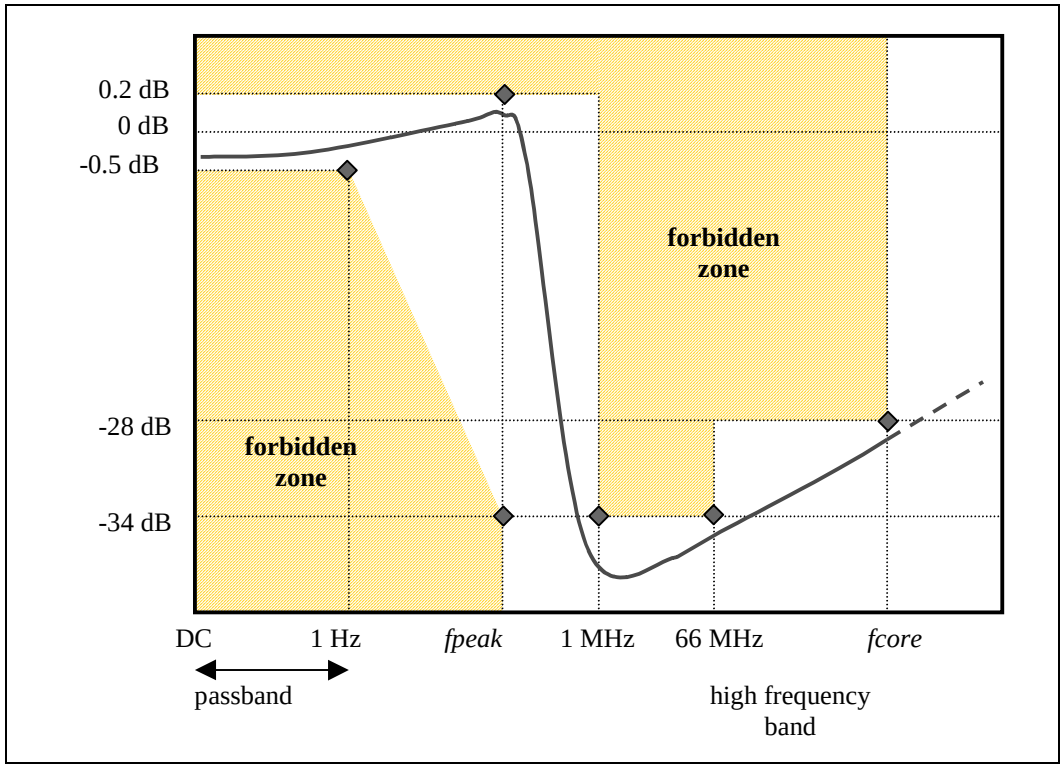


Figure 2. Phase Lock Loop (PLL) Filter Requirements



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. fpeak, if existent, should be less than 0.05 MHz.

2.5 Reserved, Unused Pins, and TESTHI[10:0]

All RESERVED pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Pentium 4 processors. See Chapter 5.0 for a pin listing of the processor and the location of all RESERVED pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. In a system level design, on-die termination has been included on the Pentium 4 processor to allow signals to be terminated within the processor silicon. Most unused AGTL+ inputs should be left as no connects, as AGTL+ termination is provided on the processor silicon. However, see Table 3 for details on AGTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value for the on-die termination resistors (R_{TT}). See Table 9.

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Therefore, the system board must properly terminate these signals. Signal termination for these signal types is discussed in the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide*. TAP signal termination requirements are also discussed in Section 9.1.4.

The TESTHI[10:0] pins must be connected to V_{CC} via a pull-up resistor. TESTHI[10:0] may be connected individually to V_{CC} via pull-up resistors between 1 kΩ and 10 kΩ value. Alternately, TESTHI[1:0] may be tied together and pulled up to V_{CC} with a single 1 kΩ - 4.7 kΩ resistor; TESTHI[7:2] may be tied together and pulled up to V_{CC} with a single 1 kΩ - 4.7 kΩ resistor; and TESTHI[10:8] may be tied together and pulled up to V_{CC} with a single 1 kΩ - 4.7 kΩ resistor. However, tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing.

2.6 System Bus Signal Groups

In order to simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependant upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 3 identifies which signals are common clock, source synchronous, and asynchronous.

Table 3. System Bus Pin Groups (Page 1 of 2)

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#[2], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#[2], BR0#[2], DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#[5]</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#[5]</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#

Table 3. System Bus Pin Groups (Page 2 of 2)

Signal Group	Type	Signals[1]
Asynchronous GTL+ Input[4]		A20M#, DBR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Asynchronous GTL+ Output[4]		FERR#, IERR#, THERMTRIP#, PROCHOT#
TAP Input[4]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[4]	Synchronous to TCK	DBR[3], TDO
System Bus Clock	Clock	BCLK[1:0], ITP_CLK[1:0][3]
Power/Other		V_{CC}, V_{CCA}, $V_{CCIOPLL}$, VID[4:0], V_{SS}, V_{SSA}, GTLREF[3:0], COMP[1:0], RESERVED, SKTOCC#, TESTHI[10:0], THERMDA, THERMDC, V_{CC_SENSE}, V_{SS_SENSE}

NOTE:
1. Refer to Section 5.2 for signal descriptions.
2. These AGTL+ signals do not have on-die termination and must be terminated on the system board.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
4. These signal groups are not terminated by the processor. They must be terminated on the system board.
5. The value of these pins during the active-to-inactive edge of RESET# determine processor configuration options. See Section 7.1 for details.

2.7 Asynchronous GTL+ Signals

Pentium 4 processors do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them. See Section 2.10 and Section 2.12 for the DC and AC specifications for the Asynchronous GTL+ signal groups. See section Section 7.2 for additional timing requirements for entering and leaving the low power states.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Pentium 4 processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required, with each driving a different voltage level. Refer to Chapter 9.0 for more detailed information.

2.9 Maximum Ratings

Table 4 lists the processor's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 4. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
V_{CC}	Any processor supply voltage with respect to V_{SS}	–0.5	2.1	V	1
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	-0.3	2.1	V	
$V_{inAsynch\_GTL+}$	Asynch GTL+ buffer DC input voltage with respect to V_{SS}	-0.3	2.1	V	
I_{VID}	Max VID pin current		5	mA	

NOTE:
1. This rating applies to any processor pin.

2.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core silicon and not the package pins unless noted otherwise. See Chapter 5.0 for the pin signal definitions and signal pin assignments. Most of the signals on the processor system bus are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 7.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 8.

Table 5 through Table 8 list the DC specifications for the Pentium 4 processor and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 5. Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CC}	V_{CC} for processor at 1.30 GHz 1.40 GHz 1.50 GHz	 1.565 1.560 1.555		 1.70 1.70 1.70	 V V	 2, 3, 4 2, 3, 4 2, 3, 4
V_{CC_MID}	V_{CC} for processor at maximum current		$(V_{CC\_MAX}+V_{CC\_MIN})/2$		V	4
I_{CC}	I_{CC} for processor 1.30 GHz 1.40 GHz 1.50 GHz			 38.1 40.6 43.0	 A A A	 4, 5 4, 5 4, 5
I_{SGNT} I_{SLP}	I_{CC} Stop-Grant, I_{CC} Sleep 1.30 GHz 1.40 GHz 1.50 GHz			 8.3 8.5 8.6	 A A A	6, 8
I_{DSLP}	I_{CC} Deep Sleep			6.6	A	8
I_{TCC}	I_{CC} TCC active			I_{CC}	A	7
I_{CC_PLL}	I_{CC} for PLL pins			30	mA	

NOTES:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or early empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.4 and Table 2 for more information.
3. The voltage specification requirements are measured across V_{CC_SENSE} and V_{SS_SENSE} pins at the socket with a 100MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. The processor should not be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MID} + 0.055*(1 - I_{CC}/I_{CC_MAX}) [V]. Moreover, V_{cc} should never exceed V_{CC_MAX} (VID). Failure to adhere to this specification can shorten the processor lifetime.
5. Maximum current is defined at V_{CC_MID}.
6. The current specified is also for AutoHALT State.
7. The maximum instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT# is the same as the maximum I_{CC} for the processor.
8. I_{CC} Stop-Grant, I_{CC} Sleep, and I_{CC} Deep Sleep are specified at V_{CC_MAX}.

Table 6. System Bus Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
V_L	Input Low Voltage		0		V	5	
V_H	Input High Voltage	0.660	0.710	0.850	V	5	
V_{CROSS}	Crossing Voltage	0.45*(V_H-V_L)	0.5*(V_H-V_L)	0.55*(V_H-V_L)	V	5	2, 3
V_{OV}	Overshoot	N/A	N/A	0.3	V	5	4
V_{US}	Undershoot	N/A	N/A	0.3	V	5	5
V_{RBM}	Ringback Margin	0.200			V	5	6
V_{TH}	Threshold Region	V_{CROSS} -0.100		V_{CROSS}+0.100	V	5	7

NOTES:.
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. The V_L and V_H used to calculate V_{CROSS} are the actual V_L and V_H seen by the processor.
4. Overshoot is defined as the absolute value of the maximum voltage allowed above the V_H level.
5. Undershoot is defined as the absolute value of the maximum voltage allowed below the V_{SS} level.
6. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
7. Threshold Region is defined as a region centered about the crossing voltage in which the differential receiver switches. It includes input threshold hysteresis.

Table 7. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	-0.150	GTLREF - 100mV	V	2, 6
V_{IH}	Input High Voltage	GTLREF + 100mV	V_{CC}	V	3, 4, 6
V_{OL}	Output Low Voltage	-0.150	V_{CC}* R_{ON_MAX} / (R_{ON_MAX}+.5 * Rtt_min)	V	6
V_{OH}	Output High Voltage	GTLREF + 100mV	V_{CC}	V	4, 6
I_{OL}	Output Low Current		V_{CC} / (0.5*Rtt_min + R_{ON_MIN})	mA	6
I_{LI}	Input Leakage Current		± 100	µA	
I_{LO}	Output Leakage Current		± 100	µA	
R_{ON}	Buffer On Resistance	5	11	Ω	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. Refer to processor I/O Buffer Models for I/V characteristics.
6. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.

Table 8. Asynchronous GTL+ and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	-0.150	V_{CC}/2 - 300mV	V	5
V_{IH}	Input High Voltage	V_{CC}/2 + 300mV	V_{CC}	V	4, 5
V_{OL}	Output Low Voltage	-0.150	0.400	V	2
V_{OH}	Output High Voltage		V_{CC}	V	3, 4, 5
I_{OL}	Output Low Current		28	mA	6
I_{LI}	Input Leakage Current		± 100	µA	
I_{LO}	Output Leakage Current		± 100	µA	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Parameter will be measured at 9mA (for use with system inputs).
3. All outputs are open-drain.
4. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
6. Rpu_min refers to the minimum resistance of the on board termination resistance.

2.11 AGTL+ System Bus Specifications

Routing topology recommendations may be found in the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide.* Termination resistors are not required for most AGTL+ signals, as these are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal's voltage with a reference voltage called GTLREF (known as V_{REF} in previous documentation).

Table 9 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on platform design see the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide.*

Table 9. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
GTLREF	Bus Reference Voltage	-2%	2/3 V_{CC}	+2%	V	2, 3, 6
R_{TT}	Termination Resistance	36	41	46	Ω	4
COMP[1:0]	COMP Resistance	42.77	43.2	45.45	Ω	5, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of V_{CC}.
3. GTLREF should be generated from V_{CC} by a voltage divider of 1% resistors or 1% matched resistors. Refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for implementation details.
4. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Refer to processor I/O buffer models for I/V characteristics.
5. COMP resistance must be provided on the system board with 1% resistors. See the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for implementation details.
6. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
7. A COMP Resistance of 43.2 +/- 1% is the preferred value.

2.12 System Bus AC Specifications

The processor System bus timings specified in this section are defined at the processor core silicon and are thus not measurable at the processor pins. See Chapter 5.0 for the Pentium 4 processor pin signal definitions.

Table 10 through Table 15 list the AC specifications associated with the processor system bus.

All AGTL+ timings are referenced to GTLREF for both '0' and '1' logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium 4 processor in IBIS format. AGTL+ layout guidelines are also available in the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guidelines*.

Care should be taken to read all notes associated with a particular timing parameter.

Table 10. System Bus Differential Clock Specifications

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
System Bus Frequency			100	MHz		
T1: BCLK[1:0] Period	10.0		10.2	ns	5	2
T2: BCLK[1:0] Period Stability			200	ps		3, 4
T3: BCLK[1:0] High Time	3.94	5	6.12	ns	5	
T4: BCLK[1:0] Low Time	3.94	5	6.12	ns	5	
T5: BCLK[1:0] Rise Time	175		700	ps	5	5
T6: BCLK[1:0] Fall Time	175		700	ps	5	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor core frequencies.
2. The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2).
3. For the clock jitter specification, refer to the *CK00 Clock Synthesizer/Driver Design Guidelines*.
4. In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
5. Slew rate is measured between the 35% and 65% points of the clock swing (V_L to V_H).

Table 11. System Bus Common Clock AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1,2,3]
T10: Common Clock Output Valid Delay	0.20	1.45	ns	6	4
T11: Common Clock Input Setup Time	0.65		ns	6	5
T12: Common Clock Input Hold Time	0.40		ns	6	5
T13: RESET# Pulse Width	1.00	10.00	ms	7	6, 7, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.
4. Valid delay timings for these signals are specified into the test circuit described in Figure 3 and with GTLREF at 2/3 V_{CC} ± 2%.
5. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.4 V/ ns to 4.0V/ns.
6. RESET# can be asserted asynchronously, but must be deasserted synchronously.
7. This should be measured after V_{CC} and BCLK[1:0] become stable.
8. Maximum specification applies only while PWRGOOD is asserted.

Table 12. System Bus Source Synch AC Specifications AGTL+ Signal Group (Page 1 of 2)

T# Parameter	Min	Typ	Max	Unit	Figure	Notes[1,2,3,4]
T20: Source Synchronous Data Output Valid Delay (first data/address only)	0.20		1.30	ns	8, 9	5
T21: T_{VBD}: Source Synchronous Data Output Valid Before Strobe	0.85			ns	9	5, 8
T22: T_{VAD}: Source Synchronous Data Output Valid After Strobe	0.85			ns	9	5, 8

Table 12. System Bus Source Synch AC Specifications AGTL+ Signal Group (Page 2 of 2)

T# Parameter	Min	Typ	Max	Unit	Figure	Notes[1,2,3,4]
T23: T_{VBA}: Source Synchronous Address Output Valid Before Strobe	1.88			ns	8	5, 8
T24: T_{VAA}: Source Synchronous Address Output Valid After Strobe	1.88			ns	8	5, 9
T25: T_{SUSS}: Source Synchronous Input Setup Time to Strobe	0.21			ns	8, 9	6
T26: T_{HSS}: Source Synchronous Input Hold Time to Strobe	0.21			ns	8, 9	6
T27: T_{SUCC}: Source Synchronous Input Setup Time to BCLK[1:0]	0.65			ns	8, 9	7
T28: T_{FASS}: First Address Strobe to Second Address Strobe		1/2		BCLK	8	10
T29: T_{FDSS}: First Data Strobe to Subsequent Strobes		n/4		BCLK	9	11, 12
T30: Data Strobe ‘n’ (DSTBN#) Output Valid Delay	8.80		10.20	ns	9	13
T31: Address Strobe Output Valid Delay	2.27		4.23	ns	8	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. Not 100% tested. Specified by design characterization.
3. All source synchronous AC timings are referenced to their associated strobe at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor core.
4. Unless otherwise noted these specifications apply to both data and address timings.
5. Valid delay timings for these signals are specified into the test circuit described in Figure 3 and with GTLREF at 2/3 V_{CC} ± 2%.
6. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.3 V/ns to 4.0V/ns.
7. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
8. This specification represents the minimum time the data or address will be valid before its strobe. Refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for more information on the definitions and use of these specifications.
9. This specification represents the minimum time the data or address will be valid after its strobe. Refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for more information on the definitions and use of these specifications.
10. The rising edge of ADSTB# must come approximately 1/2 BCLK period (5 ns) after the falling edge of ADSTB#.
11. For this timing parameter, n = 1, 2, and 3 for the second, third, and last data strobes respectively.
12. The second data strobe (falling edge of DSTBn#) must come approximately 1/4 BCLK period (2.5 ns) after the first falling edge of DSTBp#. The third data strobe (falling edge of DSTBp#) must come approximately 2/4 BCLK period (5 ns) after the first falling edge of DSTBp#. The last data strobe (falling edge of DSTBn#) must come approximately 3/4 BCLK period (7.5 ns) after the first falling edge of DSTBp#.
13. This specification applies only to DSTBN[3:0]# and is measured to the second falling edge of the strobe.

Table 13. Asynchronous GTL+ Signals AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1,2,3,6]
T35: Asynch GTL+ Input Pulse Width, except PWRGOOD	2		BCLKs		
T36: PWRGOOD to RESET# de-assertion time	1	10	ms	10	

Table 13. Asynchronous GTL+ Signals AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1,2,3,6]
T37: PWRGOOD Inactive Pulse Width	10		BCLKs	10	4
T38: PROCHOT# pulse width	500		us	11	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All AC timings for the Asynch GTL+ signals are referenced to the BCLK0 rising edge at Crossing Voltage. All Asynch GTL+ signal timings are referenced at GTLREF.
3. These signals may be driven asynchronously.
4. Refer to the PWRGOOD definition for more details regarding the behavior of this signal.
5. Length of assertion for PROCHOT# does not equal internal clock modulation time. Time is allocated after the assertion and before the deassertion of PROCHOT# for the processor to complete current instruction execution.
6. See section Section 7.2 for additional timing requirements for entering and leaving the low power states.

Table 14. System Bus AC Specifications (Reset Conditions)

T# Parameter	Min	Max	Unit	Figure	Notes
T45: Reset Configuration Signals (A[31:3]#, BR0#, INIT#, SMI#) Setup Time	4		BCLKs	7	1
T46: Reset Configuration Signals (A[31:3]#, BR0#, INIT#, SMI#) Hold Time	2	20	BCLKs	7	2

NOTES:
1. Before the deassertion of RESET#.
2. After clock that deasserts RESET#.
3. After the assertion of RESET#.

Table 15. TAP Signals AC Specifications

Parameter	Min	Max	Unit	Figure	Notes[1,2,3]
T55: TCK Period	60.0	1000	ns	4	
T56: TCK Rise Time		9.5	ns	4	4
T57: TCK Fall Time		9.5	ns	4	4
T58: TMS Rise Time		8.5	ns	4	4
T59: TMS Fall Time		8.5	ns	4	4
T60: TMS Clock to Output Delay	-5	-2	ns		5
T61: TDI Setup Time	0		ns		5, 8
T62: TDI Hold Time		3	ns		5, 8
T63: TDO Clock to Output Delay	0.5	3.5	ns		6
T64: TRST# Assert Time	2		TCK	11	7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the TAP signals are referenced to the TCK signal at GTLREF at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced at GTLREF at the processor pins.
4. Rise and fall times are measured from the 20% to 80% points of the signal swing.
5. Referenced to the falling edge of TCK.
6. Referenced to the rising edge of FBO (TCK) at the debug port connector.
7. TRST# is synchronized to TCK and is asserted for 5 TCK periods while TMS is asserted.
8. Specification for a minimum swing defined between TAP V_{IL_MAX} to V_{IH_MIN}. This assumes a minimum edge rate of 0.5V/ns.

2.13 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 10 through Table 15.

Note: For Figure 4 through Figure 11, the following apply:

1. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.

2. All source synchronous AC timings for AGTL+ signals are referenced to their associated strobe (address or data) at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor silicon.

3. All AC timings for AGTL+ strobe signals are referenced to BCLK[1:0] at V_{CROSS}. All AGTL+ strobe signal timings are referenced at GTLREF at the processor silicon.

4. All AC timings for the TAP signals are referenced to the TCK signal at GTLREF at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced at the processor pins.

The circuit used to test the AC specifications is shown in Figure 3.

Figure 3. AC Test Circuit

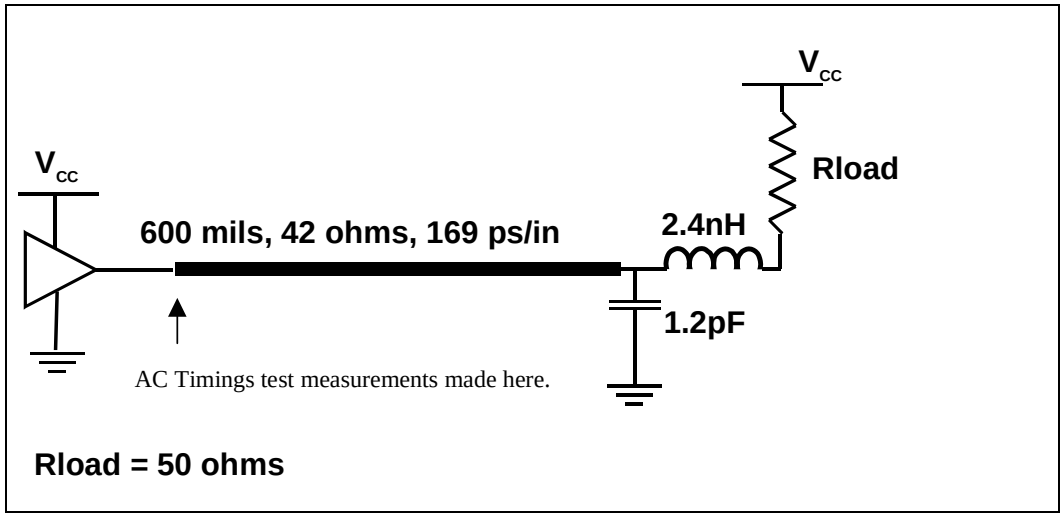
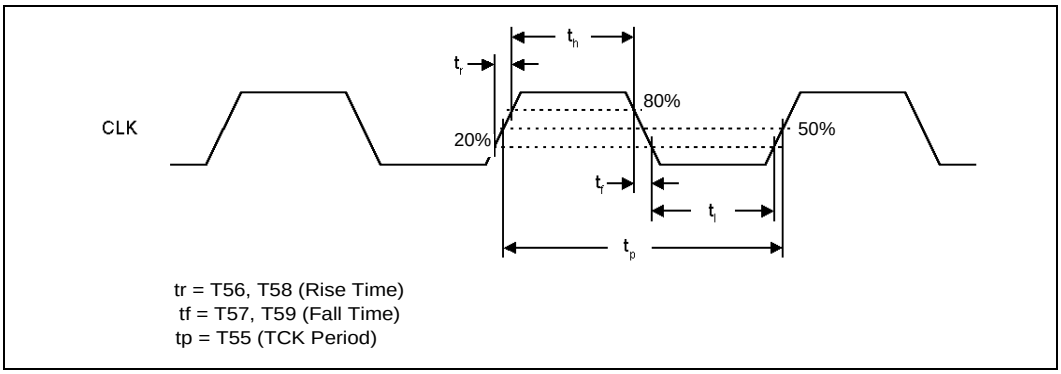
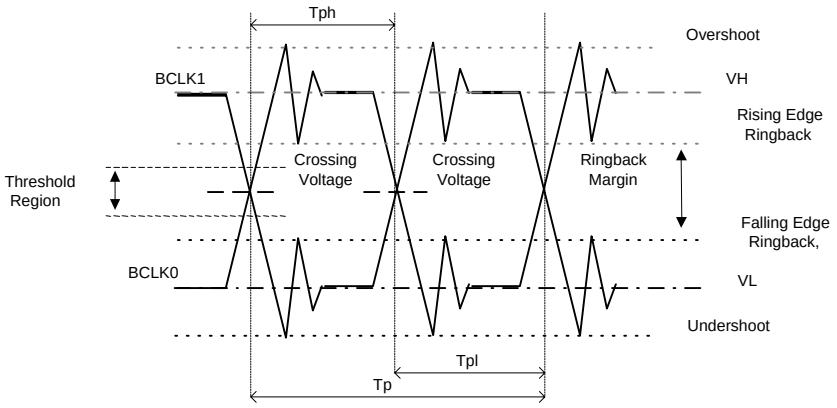


Figure 4. TCK Clock Waveform



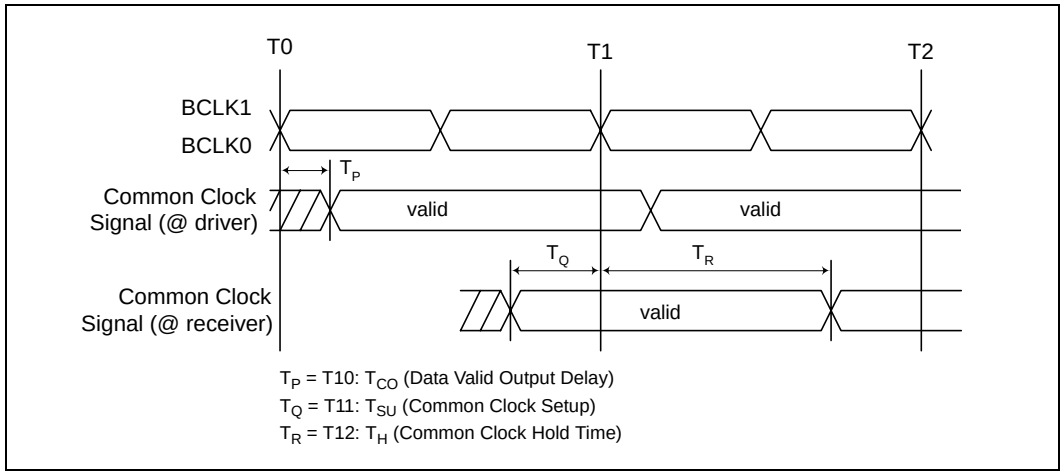
tr = T56, T58 (Rise Time)
tf = T57, T59 (Fall Time)
tp = T55 (TCK Period)

Figure 5. Differential Clock Waveform



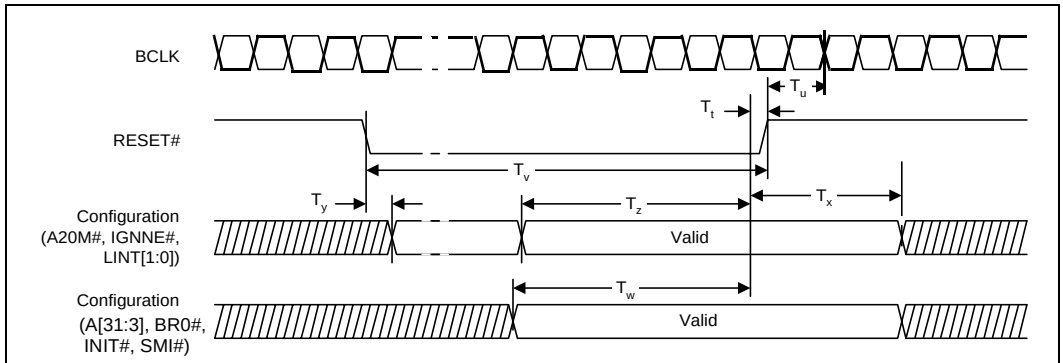
Tp = T1 (BCLK[1:0] period)
T2 = BCLK[1:0] Period stability (not shown)
Tph =T3 (BCLK[1:0] pulse high time)
Tpl = T4 (BCLK[1:0] pulse low time)
T5 = BCLK[1:0] rise time through the threshold region (not shown)
T6 = BCLK[1:0] fall time through the threshold region (not shown)

Figure 6. System Bus Common Clock Valid Delay Timings



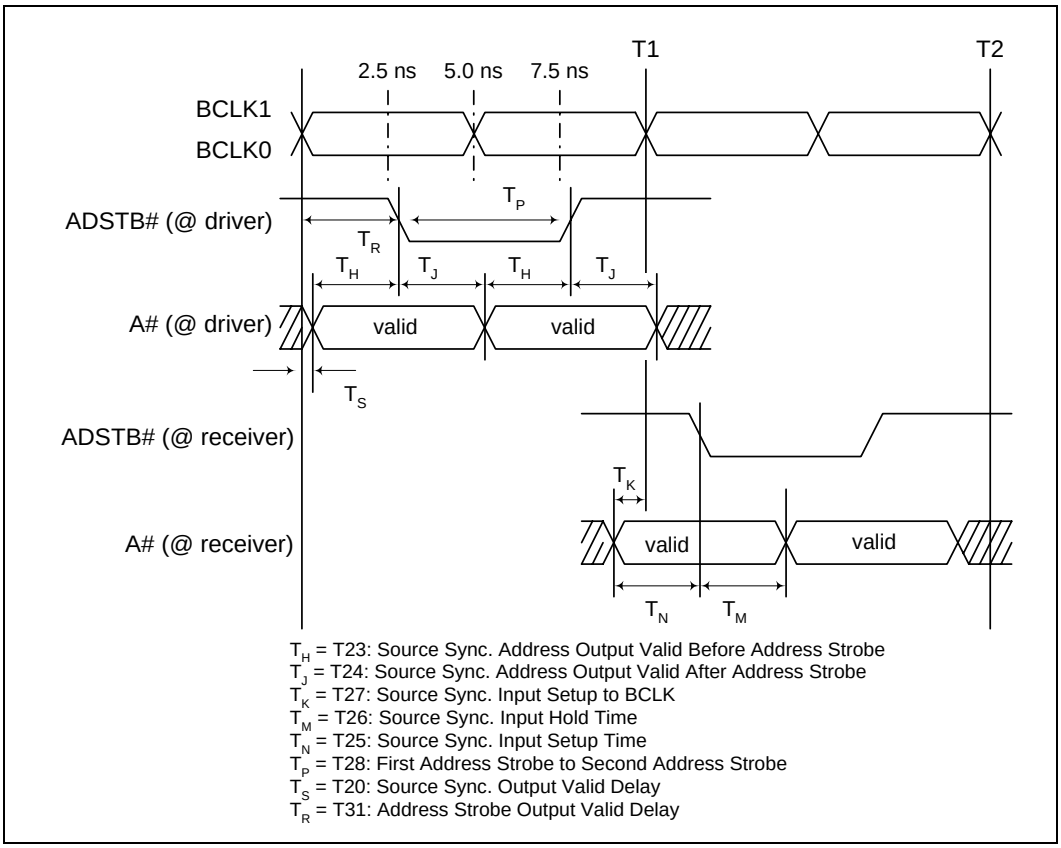
T_P = T10: T_{CO} (Data Valid Output Delay)
T_Q = T11: T_{SU} (Common Clock Setup)
T_R = T12: T_H (Common Clock Hold Time)

Figure 7. System Bus Reset and Configuration Timings



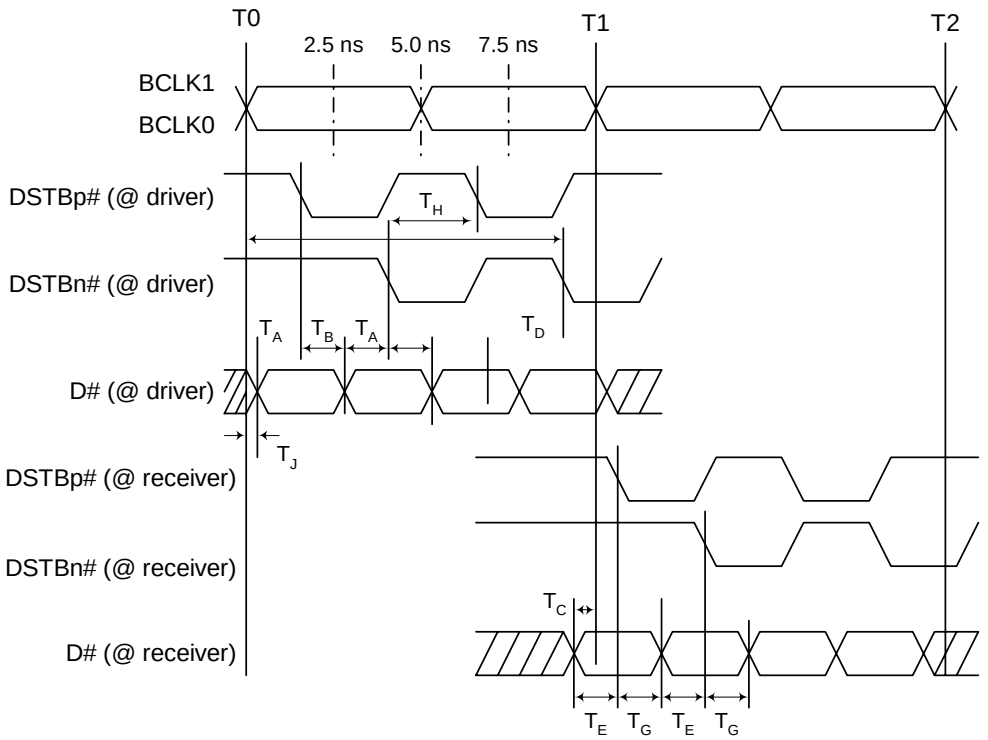
T_V = T13 (RESET# Pulse Width)
T_W = T45 (Reset Configuration Signals Setup Time)
T_X = T46 (Reset Configuration Signals Hold Time)

Figure 8. Source Synchronous 2X (Address) Timings



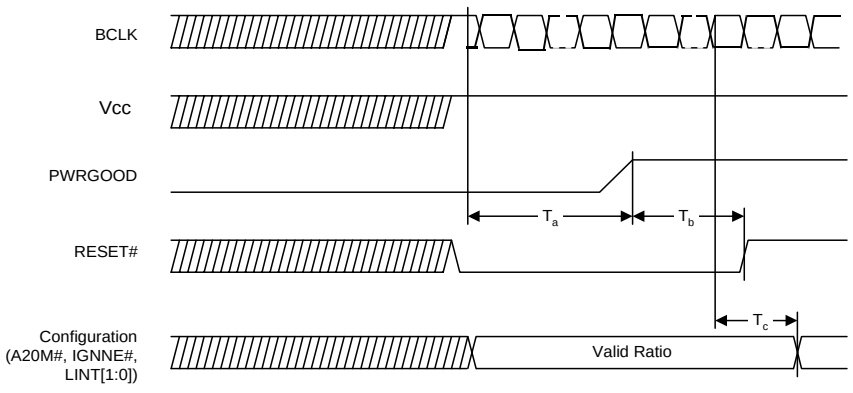
T_H = T23: Source Sync. Address Output Valid Before Address Strobe
T_J = T24: Source Sync. Address Output Valid After Address Strobe
T_K = T27: Source Sync. Input Setup to BCLK
T_M = T26: Source Sync. Input Hold Time
T_N = T25: Source Sync. Input Setup Time
T_P = T28: First Address Strobe to Second Address Strobe
T_S = T20: Source Sync. Output Valid Delay
T_R = T31: Address Strobe Output Valid Delay

Figure 9. Source Synchronous 4X Timings



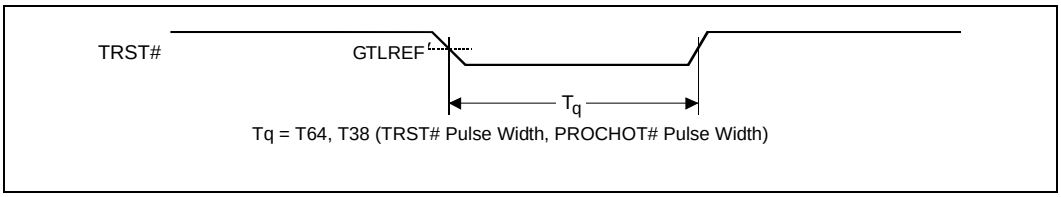
T_A = T21: Source Sync. Data Output Valid Delay Before Data Strobe
T_B = T22: Source Sync. Data Output Valid Delay After Data Strobe
T_C = T27: Source Sync. Setup Time to BCLK
T_D = T30: Source Sync. Data Strobe 'N' (DSTBN#) Output Valid Delay
T_E = T25: Source Sync. Input Setup Time
T_G = T26: Source Sync. Input Hold Time
T_H = T29: First Data Strobe to Subsequent Strobes
T_J = T20: Source Sync. Data Output Valid Delay

Figure 10. Power-On Reset and Configuration Timings



Ta = T37 (PWRGOOD Inactive Pulse Width)
Tb = T36 (PWRGOOD to RESET# de-assertion time)
Tc = T46 (Reset Configuration Signals Hold Time)

Figure 11. Test Reset Timings



3.0 System Bus Signal Quality Specifications

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines or cause incorrect latching of data. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, overshoot and undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation, and all specifications are at the processor silicon and cannot be measured at the processor pins. The *Intel® Pentium® 4 Processor Overshoot Checker Tool* is to be utilized to determine pass/fail signal quality conditions found through simulation analysis with the *Intel® Pentium® 4 Processor I/O Buffer Models (IBIS format).* This tool takes into account the specifications contained in this section.

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. The same is true for all system bus AC timing specifications in Section 2.12. Therefore, proper simulation of the Pentium 4 processor system bus is the only means to verify proper timing and signal quality metrics, and Intel highly recommends simulation during system design and measurement during system analysis.

3.1 BCLK Signal Quality Specifications and Measurement Guidelines

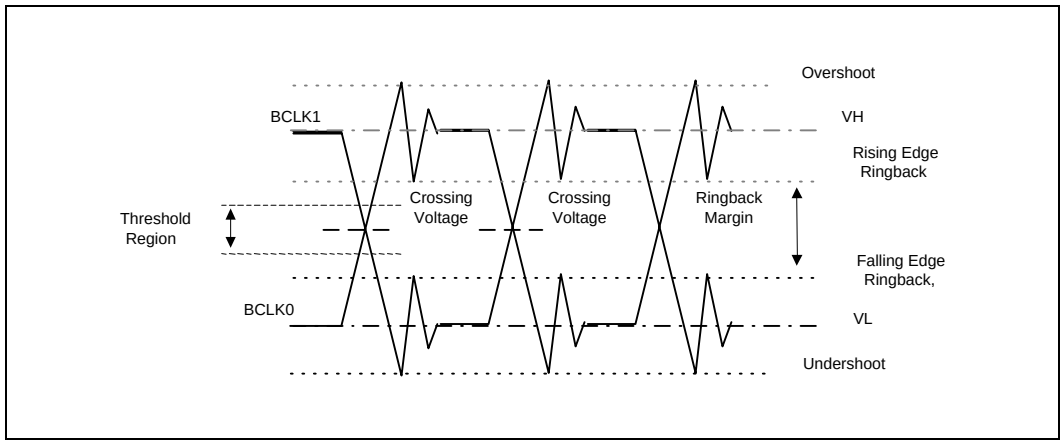
Table 16 describes the signal quality specifications for the processor system bus clock (BCLK) signals. Figure 12 describes the signal quality waveform for the system bus clock at the processor silicon. Specifications are measured at the processor silicon, not the 423-pin Socket pins.

Table 16. BCLK Signal Quality Specifications

Parameter	Min	Max	Unit	Figure	Notes[1]
BCLK[1:0] Overshoot	N/A	0.30	V	12	
BCLK[1:0] Undershoot	N/A	0.30	V	12	
BCLK[1:0] Ringback Margin	0.20	N/A	V	12	
BCLK[1:0] Threshold Region	N/A	0.10	V	12	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium 4 processor frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 12. BCLK[1:0] Signal Integrity Waveform



3.2 System Bus Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide*.

Table 17 provides the signal quality specifications for all processor signals for use in simulating signal quality at the processor silicon. Signal quality measurements cannot be made at the processor pins.

The Pentium 4 processor maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 18 through Table 21. Figure 13 shows the system bus ringback tolerance for low-to-high transitions and Figure 14 shows ringback tolerance for high-to-low transitions.

Table 17. Ringback Specifications for AGTL+, Asynchronous GTL+, and TAP Signal Groups

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
All Signals	0 → 1	GTLREF + 0.100	V	13	1,2,3,4,5,6,7
All Signals	1 → 0	GTLREF - 0.100	V	14	1,2,3,4,5,6,7

NOTES:
1. All signal integrity specifications are measured at the processor silicon.
2. Unless otherwise noted, all specifications in this table apply to all Pentium 4 processor frequencies.
3. Specifications are for the edge rate of 0.3 - 4.0V/ns.
4. All values specified by design characterization.
5. Please see Section 3.3 for maximum allowable overshoot.
6. Ringback between GTLREF + 100 mV and GTLREF - 100 mV is not supported.
7. Intel recommends simulations not exceed a ringback value of GTLREF +/- 200 mV to allow margin for other sources of system noise.

Figure 13. Low-to-High System Bus Receiver Ringback Tolerance

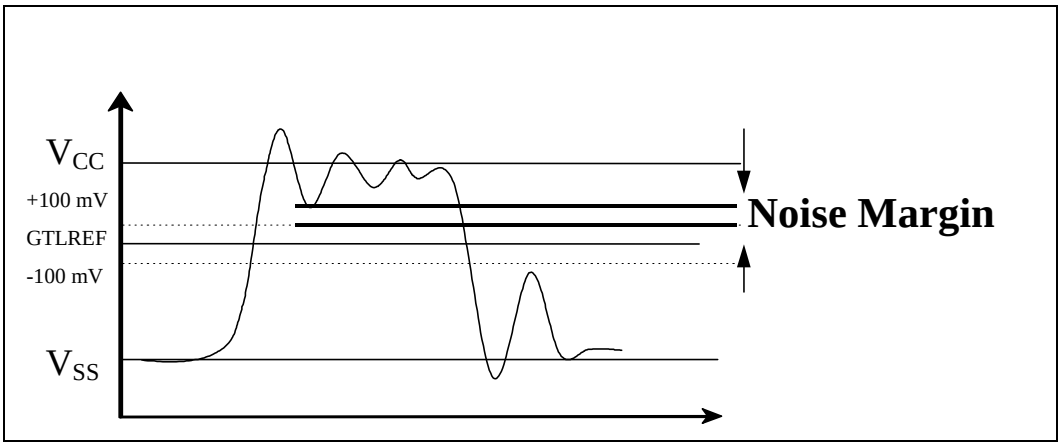
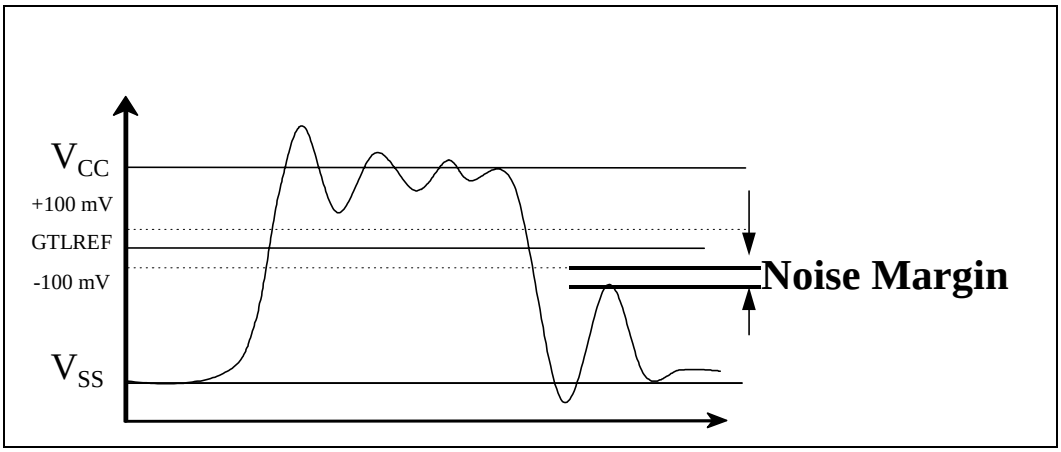


Figure 14. High-to-Low System Bus Receiver Ringback Tolerance



3.3 System Bus Signal Quality Specifications and Measurement Guidelines

3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below V_{SS}. The overshoot/undershoot specifications limit transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction, and the activity factor (AF) of the incident waveform. Permanent damage to the processor is the likely result of excessive overshoot/undershoot.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly modelled. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modelled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the Pentium 4 processor system bus, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

3.3.2 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the Pentium 4 processor both overshoot and undershoot are referenced to V_{SS}. It is important to note that overshoot and undershoot conditions are separate and their impacts must be determined independently.

Overshoot/undershoot magnitude levels must observe the absolute maximum specifications listed in Table 18 through Table 21. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations. Provided that the magnitude of the overshoot/undershoot is within the absolute maximum specifications (2.3V for overshoot and -0.65V for undershoot), the pulse magnitude, duration and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.3.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note 1: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

3.3.4 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

For source synchronous signals (address, data, and associated strobes), the activity factor is in reference to the strobe edge, since the highest frequency of assertion of any source synchronous signal is every active edge of its associated strobe. An AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every strobe cycle.

The specifications provided in Table 18 through Table 21 show the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just

meets the pulse duration for a specific magnitude where the AF < 1, means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note 1: Activity factor for common clock AGTL+ signals is referenced to BCLK[1:0] frequency.

Note 2: Activity factor for source synchronous (2x) signals is referenced to ADSTB[1:0]#.

Note 3: Activity factor for source synchronous (4x) signals is referenced to DSTBP[3:0]# and DSTBN[3:0]#.

3.3.5 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the Pentium 4 processor is not a simple single value. Instead, many factors are needed to determine the over/undershoot specification. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the *signal group* that the particular signal falls into. For AGTL+ signals operating in the 4x source synchronous domain, use Table 18. For AGTL+ signals operating in the 2x source synchronous domain, use Table 19. If the signal is an AGTL+ signal operating in the common clock domain, use Table 20. Finally, all other signals reside in the 33MHz domain (asynchronous GTL+, TAP, etc.) and are referenced in Table 21.
2. Determine the *magnitude* of the overshoot or the undershoot (relative to V_{SS}).
3. Determine the *activity factor* (how often does this overshoot occur?).
4. Next, from the appropriate specification table, determine the *maximum pulse duration* (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

3.3.6 Determining if a System Meets the Over/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below. Results from simulation may also be evaluated by utilizing the *Intel® Pentium® 4 Processor Overshoot Checker Tool* through the use of time-voltage data files.

1. Ensure no signal ever exceeds V_{CC} or -0.25V OR
2. If only one overshoot/undershoot event occurs, ensure it meets the over/undershoot specifications in the following tables OR
3. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of

these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

The following notes apply to Table 18 through Table 21.

NOTES:
1. Absolute Maximum Overshoot magnitude of 2.3V must never be exceeded.
2. Absolute Maximum Overshoot is measured relative to V_{SS}, Pulse Duration of overshoot is measured relative to V_{CC}.
3. Absolute Maximum Undershoot and Pulse Duration of undershoot is measured relative to V_{SS}.
4. Ringback below V_{CC} can not be subtracted from overshoots/undershoots.
5. Lesser undershoot does not allocate longer or larger overshoot.
6. OEM's are strongly encouraged to follow Intel provided layout guidelines.
7. All values specified by design characterization.

Table 18. Source Synchronous (400MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2,3]
2.30	-0.65	0.07	0.65	5.00	
2.25	-0.60	0.12	1.22	5.00	
2.20	-0.55	0.23	2.25	5.00	
2.15	-0.50	0.42	4.15	5.00	
2.10	-0.45	0.74	5.00	5.00	
2.05	-0.40	1.38	5.00	5.00	
2.00	-0.35	2.50	5.00	5.00	
1.95	-0.30	4.50	5.00	5.00	
1.90	-0.25	5.00	5.00	5.00	
1.85	-0.20	5.00	5.00	5.00	
1.80	-0.15	5.00	5.00	5.00	
1.75	-0.10	5.00	5.00	5.00	

NOTES:
1. These specifications are specified at the processor silicon.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 19. Source Synchronous (200MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2,3]
2.30	-0.65	0.13	1.30	10.0	
2.25	-0.60	0.24	2.44	10.0	
2.20	-0.55	0.45	4.50	10.0	
2.15	-0.50	0.83	8.30	10.0	
2.10	-0.45	1.48	10.0	10.0	
2.05	-0.40	2.76	10.0	10.0	
2.00	-0.35	5.00	10.0	10.0	
1.95	-0.30	5.00	10.0	10.0	
1.90	-0.25	10.0	10.0	10.0	
1.85	-0.20	10.0	10.0	10.0	
1.80	-0.15	10.0	10.0	10.0	
1.75	-0.10	10.0	10.0	10.0	

NOTES:
1. These specifications are specified at the processor silicon.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 20. Common Clock (100MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2,3]
2.30	-0.65	0.26	2.60	20.0	
2.25	-0.60	0.49	4.88	20.0	
2.20	-0.55	0.90	9.00	20.0	
2.15	-0.50	1.66	16.60	20.0	
2.10	-0.45	2.96	20.0	20.0	
2.05	-0.40	5.52	20.0	20.0	
2.00	-0.35	10.0	20.0	20.0	
1.95	-0.30	18.0	20.0	20.0	
1.90	-0.25	20.0	20.0	20.0	
1.85	-0.20	20.0	20.0	20.0	
1.80	-0.15	20.0	20.0	20.0	
1.75	-0.10	20.0	20.0	20.0	

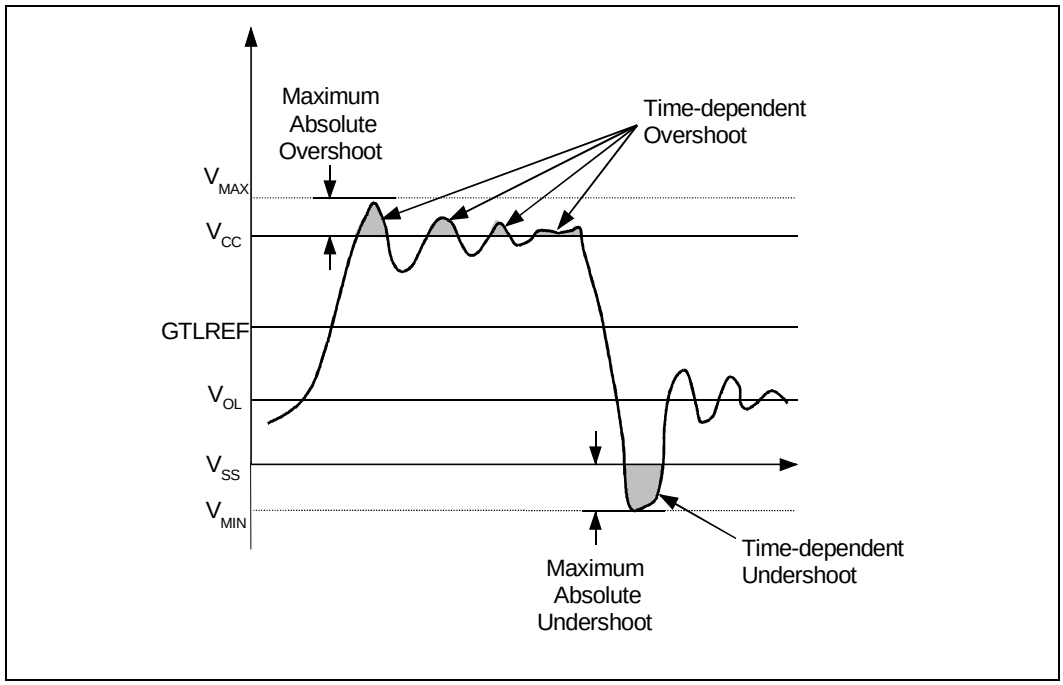
NOTES:
1. These specifications are specified at the processor silicon.
2. BCLK period is 10 ns.
3. AF is referenced to BCLK[1:0].

Table 21. Asynchronous GTL+ and TAP Signal Groups Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2]
2.30	-0.65	0.78	7.80	60.0	
2.25	-0.60	1.46	14.64	60.0	
2.20	-0.55	2.70	27.0	60.0	
2.15	-0.50	4.98	49.8	60.0	
2.10	-0.45	8.88	60.0	60.0	
2.05	-0.40	16.56	60.0	60.0	
2.00	-0.35	30.0	60.0	60.0	
1.95	-0.30	54.0	60.0	60.0	
1.90	-0.25	60.0	60.0	60.0	
1.85	-0.20	60.0	60.0	60.0	
1.80	-0.15	60.0	60.0	60.0	
1.75	-0.10	60.0	60.0	60.0	

NOTES:
1. These specifications are specified at the processor silicon.
2. This table assumes a 33MHz time domain.

Figure 15. Maximum Acceptable Overshoot/Undershoot Waveform



4.0 Package Mechanical Specifications

The Intel® Pentium® 4 Processor in the 423-pin Package uses Pin Grid Array (PGA) package technology. Components of the package include an integrated heat spreader, processor silicon, silicon mounting substrate or Organic Land Grid Array (OLGA), and an interposer which is the pincarrier. Mechanical specifications for the processor are given in this section. See Section 1.1 for a terminology listing. The processor socket which accepts the Pentium 4 processor in the 423-pin package is referred to as a 423-Pin Socket. See the *423-Pin Socket (PGA423) Design Guidelines* for further details on the 423-Pin Socket.

Note: The drawing below is not to scale and is for reference only. The socket and system board are supplied as a reference only.

Figure 16. Exploded View of Processor Components on a System Board

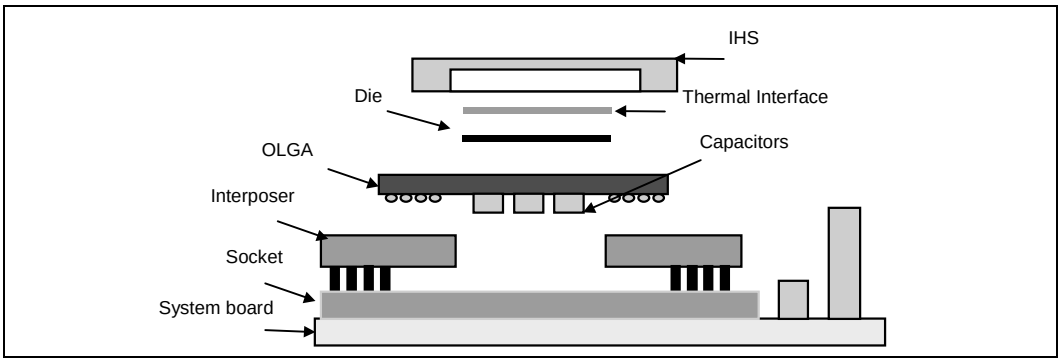


Figure 17. Processor Package

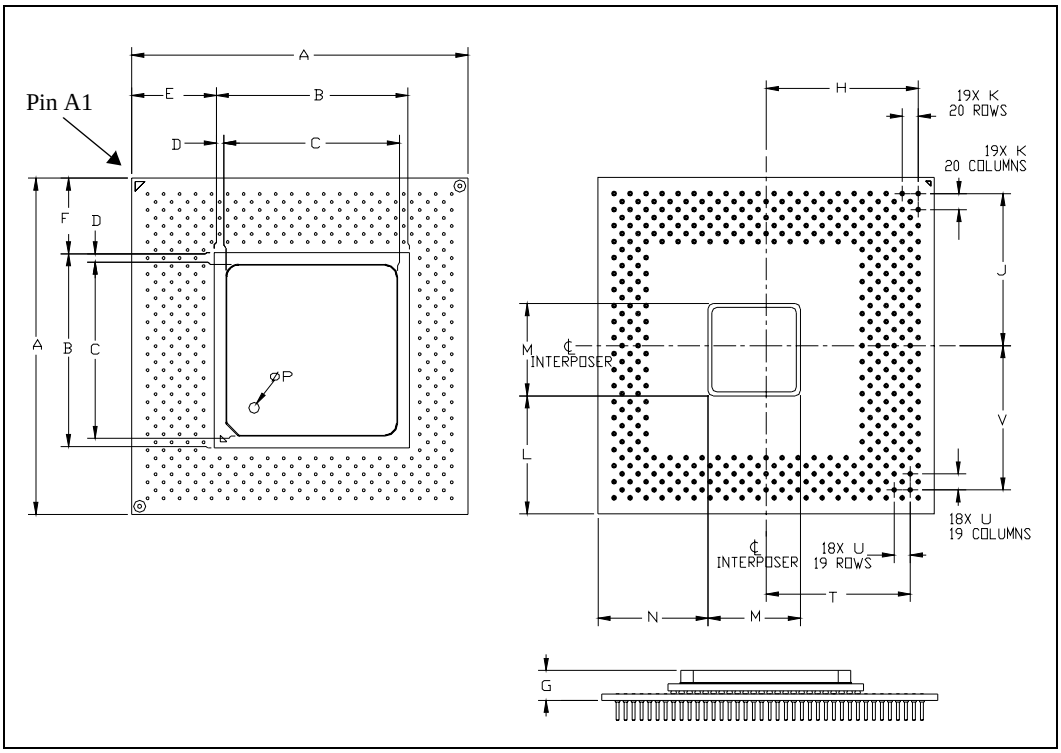


Table 22. Description Table for Processor Dimensions

Code Letter	Min	Typ	Max	Notes[1]
A	2.094	2.100	2.106	
B	1.217	1.220	1.224	
C	1.059	1.063	1.067	2
D	0.054	0.079	0.104	
E	0.509	0.515	0.521	
F	0.057	0.465	0.471	
G	0.167	0.192	0.217	
H	0.941	0.950	0.959	
J	0.941	0.950	0.959	
K		0.100		
L	0.727	0.737	0.747	
M	0.571	0.576	0.581	
N	0.677	0.687	0.697	
P	0.055	0.067	0.079	3
T	0.891	0.900	0.909	
U		0.100		
V	0.891	0.900	0.909	

NOTES:
1. All dimensions in inches unless otherwise noted.
2. Nickel plated copper.
3. Diameter

Figure 18 details the keep in specification for pin-side components. Pentium 4 processors may contain pin side capacitors mounted to the processor OLGA package. The capacitors will be exposed within the opening of the interposer cavity.

Figure 20 details the flatness and tilt specifications for the IHS. Tilt is measured with the reference datum set to the bottom of the processor interposer.

Figure 18. Processor Cross-Section and Keep-in

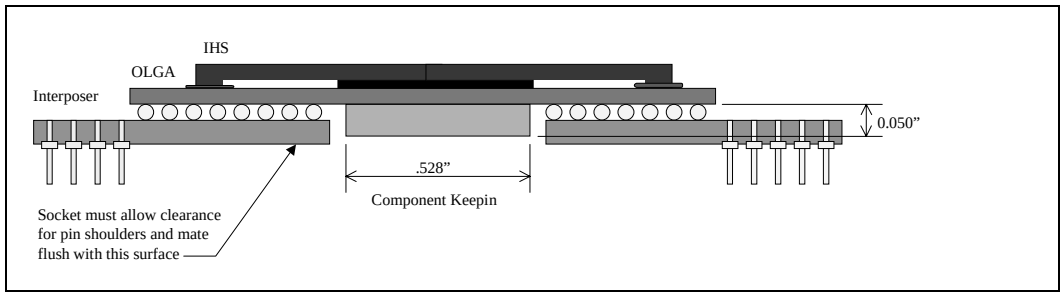


Figure 19. Processor Pin Detail

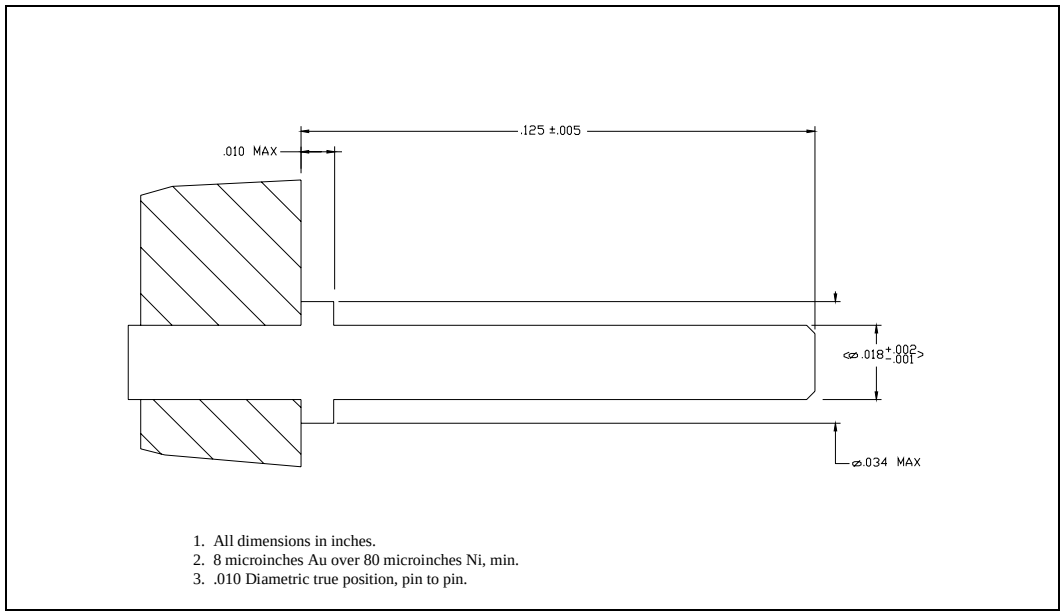
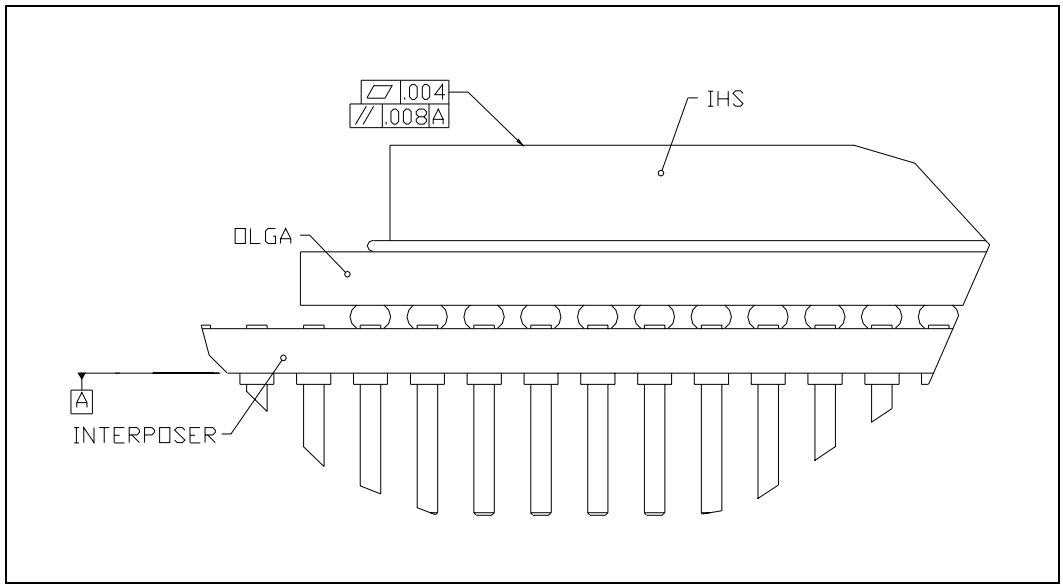


Figure 20. IHS Flatness Specification



4.1 Package Load Specifications

Table 23 provides dynamic and static load specifications for the Pentium 4 processor in the 423-pin package IHS. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solutions

must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heat sink-to-processor thermal interface. It is not recommended to use any portion of the processor interposer as a mechanical reference or load bearing surface for thermal solutions.

Table 23. Package Dynamic and Static Load Specifications

Parameter	Max	Unit	Notes
Static	25	lbf	1, 2, 3
Dynamic	100	lbf	1, 3, 4

NOTES:
1. This specification applies to a uniform load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. These parameters are based on design characterization and not tested.
4. Dynamic load specifications are defined assuming a maximum duration of 11ms.

4.2 Processor Insertion Specifications

The Pentium 4 processor in the 423-pin package can be inserted and removed 30 times from a 423-pin socket meeting the *423-Pin Socket Design Guidelines* document. Note that this specification is based on design characterization and is not tested.

4.3 Processor Mass Specifications

Table 24 specifies the processor's mass. This includes all components which make up the entire processor product.

Table 24. Processor Mass

Processor	Mass (grams)
Pentium 4 processor, 31mm OLGA	23

4.4 Processor Materials

The Pentium 4 processor is assembled from several components. The basic material properties are described in Table 25.

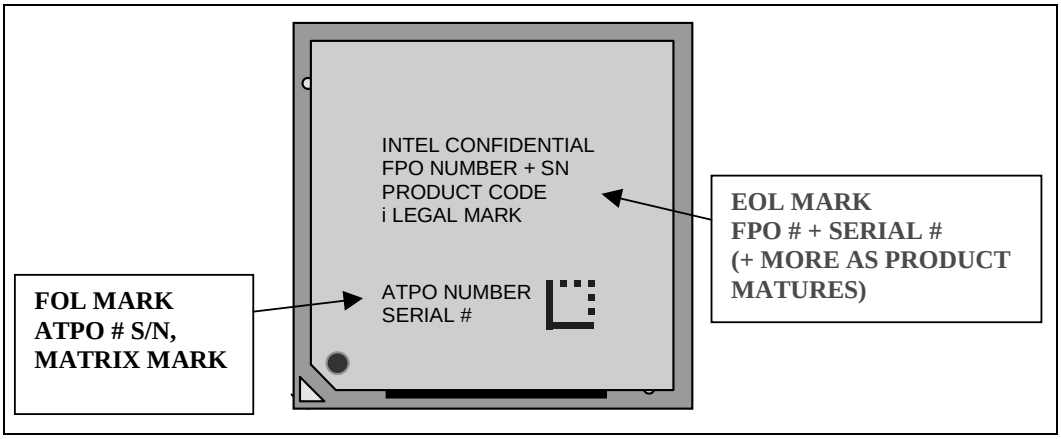
Table 25. Processor Material Properties

Component	Material	Notes
Integrated Heat Spreader	Nickel over copper	
Interposer	FR4	
Interposer pins	Gold over nickel	

4.5 Processor Markings

The following section details the processor top-side laser markings and is provided to aid in the identification of the Pentium 4 processor. Specific details regarding individual fields in the product markings will be provided in a future release of the EMTS.

Figure 21. Processor Markings

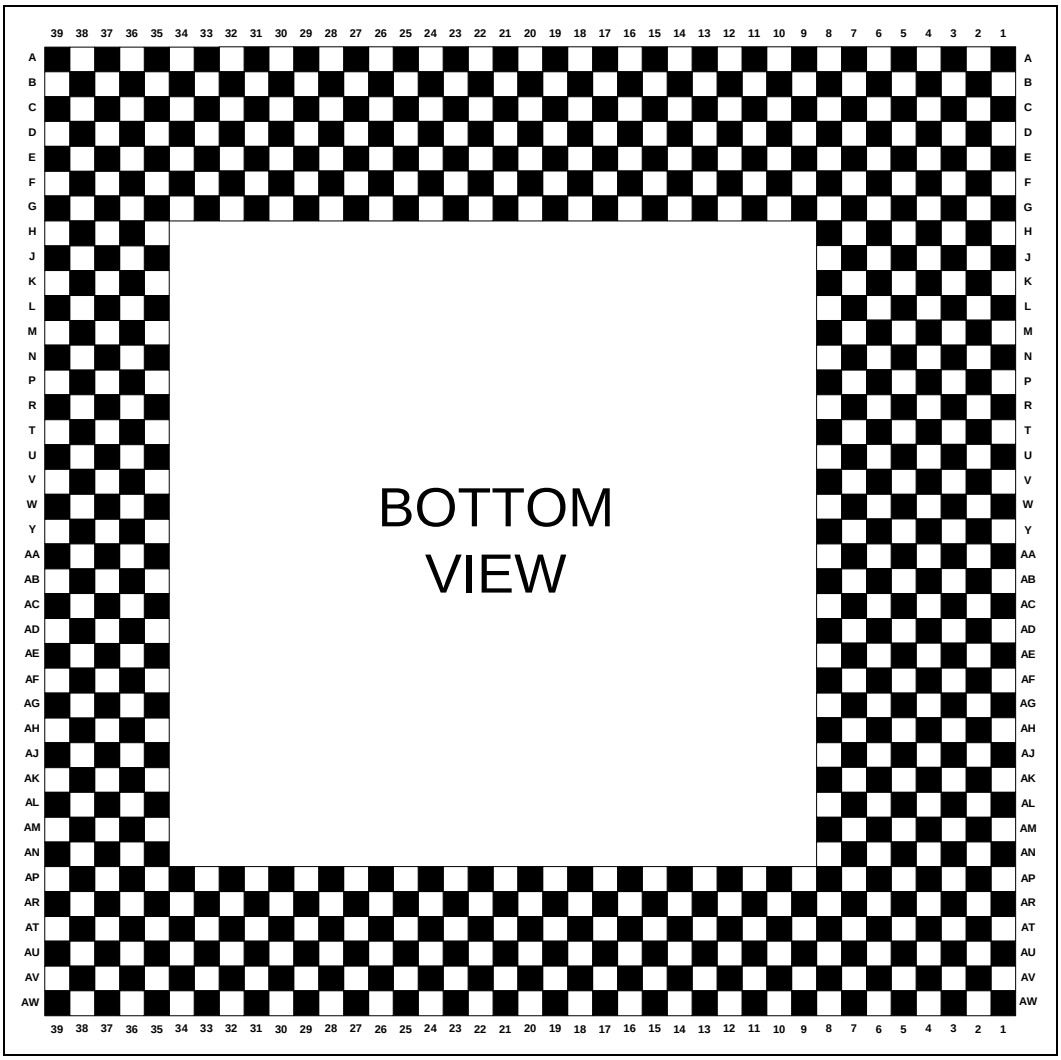


NOTES:
1. Character size for laser markings is: height 0.050", width 0.032".
2. All characters will be in upper case.

4.6 Processor Pin-Out Coordinates

Figure 22 details the coordinates of the 423 processor pins as viewed from the bottom of the package.

Figure 22. Processor Pinout Diagram - Bottom View



5.0 Pin Listing and Signal Definitions

5.1 Processor Pin Assignments

Section 5.1 contains the pinlist for the Intel® Pentium® 4 Processor in the 423-pin Package in Table 26 and Table 27. Table 26 is a listing of all processor pins ordered alphabetically by pin name. Table 27 is also a listing of all processor pins but ordered by pin number.

5.1.1 Pin Listing by Pin Name

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A3#	F30	Source Synch	Input/Output
A4#	C29	Source Synch	Input/Output
A5#	D30	Source Synch	Input/Output
A6#	C31	Source Synch	Input/Output
A7#	F28	Source Synch	Input/Output
A8#	D28	Source Synch	Input/Output
A9#	F26	Source Synch	Input/Output
A10#	C23	Source Synch	Input/Output
A11#	A31	Source Synch	Input/Output
A12#	C25	Source Synch	Input/Output
A13#	A25	Source Synch	Input/Output
A14#	A23	Source Synch	Input/Output
A15#	A27	Source Synch	Input/Output
A16#	D24	Source Synch	Input/Output
A17#	A29	Source Synch	Input/Output
A18#	C27	Source Synch	Input/Output
A19#	D26	Source Synch	Input/Output
A20#	A17	Source Synch	Input/Output
A21#	C17	Source Synch	Input/Output
A22#	A21	Source Synch	Input/Output
A23#	C19	Source Synch	Input/Output
A24#	F22	Source Synch	Input/Output
A25#	D22	Source Synch	Input/Output
A26#	A15	Source Synch	Input/Output
A27#	A13	Source Synch	Input/Output

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A28#	F20	Source Synch	Input/Output
A29#	C21	Source Synch	Input/Output
A30#	A19	Source Synch	Input/Output
A31#	C11	Source Synch	Input/Output
A32#	A9	Source Synch	Input/Output
A33#	A11	Source Synch	Input/Output
A34#	C15	Source Synch	Input/Output
A35#	D12	Source Synch	Input/Output
A20M#	T38	Asynch GTL+	Input
ADS#	F36	Common Clock	Input/Output
ADSTB0#	G25	Source Synch	Input/Output
ADSTB1#	G21	Source Synch	Input/Output
AP0#	F16	Common Clock	Input/Output
AP1#	D14	Common Clock	Input/Output
BCLK0	AR7	Bus Clock	Input
BCLK1	AP8	Bus Clock	Input
BINIT#	F18	Common Clock	Input/Output
BNR#	E35	Common Clock	Input/Output
BPM0#	F8	Common Clock	Input/Output
BPM1#	F12	Common Clock	Input/Output
BPM2#	F10	Common Clock	Input/Output
BPM3#	E7	Common Clock	Input/Output
BPM4#	C13	Common Clock	Input/Output
BPM5#	D6	Common Clock	Input/Output
BPRI#	L37	Common Clock	Input
BR0#	B36	Common Clock	Input/Output

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
COMP0	AU27	Power/Other	Input/Output
COMP1	F24	Power/Other	Input/Output
D0#	Y38	Source Synch	Input/Output
D1#	AD36	Source Synch	Input/Output
D2#	W37	Source Synch	Input/Output
D3#	AE37	Source Synch	Input/Output
D4#	AG39	Source Synch	Input/Output
D5#	AA35	Source Synch	Input/Output
D6#	V36	Source Synch	Input/Output
D7#	AF38	Source Synch	Input/Output
D8#	W39	Source Synch	Input/Output
D9#	AE39	Source Synch	Input/Output
D10#	AB36	Source Synch	Input/Output
D11#	AD38	Source Synch	Input/Output
D12#	AH36	Source Synch	Input/Output
D13#	AJ37	Source Synch	Input/Output
D14#	AC37	Source Synch	Input/Output
D15#	AA39	Source Synch	Input/Output
D16#	AT36	Source Synch	Input/Output
D17#	AK38	Source Synch	Input/Output
D18#	AP34	Source Synch	Input/Output
D19#	AW37	Source Synch	Input/Output
D20#	AM38	Source Synch	Input/Output
D21#	AU39	Source Synch	Input/Output
D22#	AP36	Source Synch	Input/Output
D23#	AN39	Source Synch	Input/Output
D24#	AK36	Source Synch	Input/Output
D25#	AR37	Source Synch	Input/Output
D26#	AT38	Source Synch	Input/Output
D27#	AN35	Source Synch	Input/Output
D28#	AU35	Source Synch	Input/Output
D29#	AW39	Source Synch	Input/Output
D30#	AT34	Source Synch	Input/Output
D31#	AL37	Source Synch	Input/Output
D32#	AW31	Source Synch	Input/Output
D33#	AT32	Source Synch	Input/Output
D34#	AU29	Source Synch	Input/Output
D35#	AP26	Source Synch	Input/Output
D36#	AU33	Source Synch	Input/Output

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D37#	AW29	Source Synch	Input/Output
D38#	AU31	Source Synch	Input/Output
D39#	AT30	Source Synch	Input/Output
D40#	AT28	Source Synch	Input/Output
D41#	AP24	Source Synch	Input/Output
D42#	AU25	Source Synch	Input/Output
D43#	AP28	Source Synch	Input/Output
D44#	AW25	Source Synch	Input/Output
D45#	AT24	Source Synch	Input/Output
D46#	AW23	Source Synch	Input/Output
D47#	AU23	Source Synch	Input/Output
D48#	AU19	Source Synch	Input/Output
D49#	AT20	Source Synch	Input/Output
D50#	AU21	Source Synch	Input/Output
D51#	AW21	Source Synch	Input/Output
D52#	AW19	Source Synch	Input/Output
D53#	AT18	Source Synch	Input/Output
D54#	AU17	Source Synch	Input/Output
D55#	AT16	Source Synch	Input/Output
D56#	AU15	Source Synch	Input/Output
D57#	AT14	Source Synch	Input/Output
D58#	AW13	Source Synch	Input/Output
D59#	AU13	Source Synch	Input/Output
D60#	AT12	Source Synch	Input/Output
D61#	AP14	Source Synch	Input/Output
D62#	AW17	Source Synch	Input/Output
D63#	AP12	Source Synch	Input/Output
DBI0#	AL39	Source Synch	Input/Output
DBI1#	AU37	Source Synch	Input/Output
DBI2#	AT22	Source Synch	Input/Output
DBI3#	AW15	Source Synch	Input/Output
DBR#	AV2	Asynch GTL+	Output
DBSY#	B34	Common Clock	Input/Output
DEFER#	J35	Common Clock	Input
DP0#	AW33	Common Clock	Input/Output
DP1#	AW35	Common Clock	Input/Output
DP2#	AW27	Common Clock	Input/Output
DP3#	AT26	Common Clock	Input/Output
DRDY#	G37	Common Clock	Input/Output

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
DSTBN0#	AG35	Source Synch	Input/Output
DSTBN1#	AP32	Source Synch	Input/Output
DSTBN2#	AP22	Source Synch	Input/Output
DSTBN3#	AP18	Source Synch	Input/Output
DSTBP0#	AJ35	Source Synch	Input/Output
DSTBP1#	AP30	Source Synch	Input/Output
DSTBP2#	AP20	Source Synch	Input/Output
DSTBP3#	AP16	Source Synch	Input/Output
FERR#	P38	Asynch GTL+	Output
GTLREF	AC35	Power/Other	Input
GTLREF	AP10	Power/Other	Input
GTLREF	F14	Power/Other	Input
GTLREF	T36	Power/Other	Input
HIT#	K36	Common Clock	Input/Output
HITM#	D36	Common Clock	Input/Output
IERR#	C7	Common Clock	Output
IGNNE#	M38	Asynch GTL+	Input
INIT#	D8	Asynch GTL+	Input
ITP_CLK0	AU1	TAP	Input
ITP_CLK1	AW1	TAP	Input
LINT0	H36	Asynch GTL+	Input
LINT1	W35	Asynch GTL+	Input
LOCK#	A33	Common Clock	Input/Output
MCERR#	D10	Common Clock	Input/Output
PROCHOT#	F38	Asynch GTL+	Output
PWRGOOD	AW9	Asynch GTL+	Input
REQ0#	C33	Source Synch	Input/Output
REQ1#	D32	Source Synch	Input/Output
REQ2#	F34	Source Synch	Input/Output
REQ3#	D34	Source Synch	Input/Output
REQ4#	F32	Source Synch	Input/Output
RESERVED	AT4		
RESET#	AW11	Common Clock	Input
RS0#	M36	Common Clock	Input
RS1#	N35	Common Clock	Input
RS2#	U35	Common Clock	Input
RSP#	C9	Common Clock	Input
SKTOCC#	A5	Power/Other	Output
SLP#	AW7	Asynch GTL+	Input

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
SMI#	K38	Asynch GTL+	Input
STPCLK#	C5	Asynch GTL+	Input
TCK	R37	TAP	Input
TDI	J39	TAP	Input
TDO	P36	TAP	Output
TESTHI0	A7	Power/Other	Input
TESTHI1	AT10	Power/Other	Input
TESTHI2	AT6	Power/Other	Input
TESTHI3	AT8	Power/Other	Input
TESTHI4	AU7	Power/Other	Input
TESTHI5	AU9	Power/Other	Input
TESTHI6	AU11	Power/Other	Input
TESTHI7	AW5	Power/Other	Input
TESTHI8	D16	Power/Other	Input
TESTHI9	D18	Power/Other	Input
TESTHI10	D20	Power/Other	Input
THERMDA	H38	Power/Other	
THERMDC	E39	Power/Other	
THERMTRIP#	U37	Asynch GTL+	Output
TMS	D38	TAP	Input
TRDY#	A35	Common Clock	Input
TRST#	R35	TAP	Input
VCC	A37	Power/Other	
VCC	A39	Power/Other	
VCC	AA1	Power/Other	
VCC	AA5	Power/Other	
VCC	AB38	Power/Other	
VCC	AB4	Power/Other	
VCC	AB8	Power/Other	
VCC	AC3	Power/Other	
VCC	AC7	Power/Other	
VCC	AD2	Power/Other	
VCC	AD6	Power/Other	
VCC	AE1	Power/Other	
VCC	AE35	Power/Other	
VCC	AE5	Power/Other	
VCC	AF4	Power/Other	
VCC	AF8	Power/Other	
VCC	AG3	Power/Other	

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AG37	Power/Other	
VCC	AG7	Power/Other	
VCC	AH2	Power/Other	
VCC	AH6	Power/Other	
VCC	AJ1	Power/Other	
VCC	AJ39	Power/Other	
VCC	AJ5	Power/Other	
VCC	AK4	Power/Other	
VCC	AK8	Power/Other	
VCC	AL3	Power/Other	
VCC	AL7	Power/Other	
VCC	AM2	Power/Other	
VCC	AM36	Power/Other	
VCC	AM6	Power/Other	
VCC	AN1	Power/Other	
VCC	AN5	Power/Other	
VCC	AP38	Power/Other	
VCC	AP4	Power/Other	
VCC	AR13	Power/Other	
VCC	AR17	Power/Other	
VCC	AR21	Power/Other	
VCC	AR25	Power/Other	
VCC	AR29	Power/Other	
VCC	AR3	Power/Other	
VCC	AR33	Power/Other	
VCC	AR9	Power/Other	
VCC	AT2	Power/Other	
VCC	AV10	Power/Other	
VCC	AV14	Power/Other	
VCC	AV18	Power/Other	
VCC	AV22	Power/Other	
VCC	AV26	Power/Other	
VCC	AV30	Power/Other	
VCC	AV34	Power/Other	
VCC	AV38	Power/Other	
VCC	AV6	Power/Other	
VCC	B10	Power/Other	
VCC	B14	Power/Other	
VCC	B18	Power/Other	

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	B22	Power/Other	
VCC	B26	Power/Other	
VCC	B30	Power/Other	
VCC	B6	Power/Other	
VCC	C3	Power/Other	
VCC	C37	Power/Other	
VCC	D2	Power/Other	
VCC	E1	Power/Other	
VCC	E13	Power/Other	
VCC	E17	Power/Other	
VCC	E21	Power/Other	
VCC	E25	Power/Other	
VCC	E29	Power/Other	
VCC	E33	Power/Other	
VCC	E5	Power/Other	
VCC	E9	Power/Other	
VCC	F4	Power/Other	
VCC	G13	Power/Other	
VCC	G19	Power/Other	
VCC	G29	Power/Other	
VCC	G3	Power/Other	
VCC	G33	Power/Other	
VCC	G39	Power/Other	
VCC	G7	Power/Other	
VCC	G9	Power/Other	
VCC	H2	Power/Other	
VCC	H6	Power/Other	
VCC	J1	Power/Other	
VCC	J37	Power/Other	
VCC	J5	Power/Other	
VCC	K4	Power/Other	
VCC	K8	Power/Other	
VCC	L3	Power/Other	
VCC	L35	Power/Other	
VCC	L7	Power/Other	
VCC	M2	Power/Other	
VCC	M6	Power/Other	
VCC	N1	Power/Other	
VCC	N5	Power/Other	

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	P4	Power/Other	
VCC	P8	Power/Other	
VCC	R3	Power/Other	
VCC	R7	Power/Other	
VCC	T2	Power/Other	
VCC	T6	Power/Other	
VCC	U1	Power/Other	
VCC	U39	Power/Other	
VCC	U5	Power/Other	
VCC	V4	Power/Other	
VCC	V8	Power/Other	
VCC	W3	Power/Other	
VCC	W7	Power/Other	
VCC	Y2	Power/Other	
VCC	Y36	Power/Other	
VCC	Y6	Power/Other	
VCC_SENSE	N39	Power/Other	Output
VCCA	AU5	Power/Other	
VCCIOPLL	AW3	Power/Other	
VID0	C1	Power/Other	Output
VID1	B2	Power/Other	Output
VID2	B4	Power/Other	Output
VID3	A3	Power/Other	Output
VID4	A1	Power/Other	Output
VSS	AA3	Power/Other	
VSS	AA37	Power/Other	
VSS	AA7	Power/Other	
VSS	AB2	Power/Other	
VSS	AB6	Power/Other	
VSS	AC1	Power/Other	
VSS	AC39	Power/Other	
VSS	AC5	Power/Other	
VSS	AD4	Power/Other	
VSS	AD8	Power/Other	
VSS	AE3	Power/Other	
VSS	AE7	Power/Other	
VSS	AF2	Power/Other	
VSS	AF36	Power/Other	
VSS	AF6	Power/Other	

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AG1	Power/Other	
VSS	AG5	Power/Other	
VSS	AH38	Power/Other	
VSS	AH4	Power/Other	
VSS	AH8	Power/Other	
VSS	AJ3	Power/Other	
VSS	AJ7	Power/Other	
VSS	AK2	Power/Other	
VSS	AK6	Power/Other	
VSS	AL1	Power/Other	
VSS	AL35	Power/Other	
VSS	AL5	Power/Other	
VSS	AM4	Power/Other	
VSS	AM8	Power/Other	
VSS	AN3	Power/Other	
VSS	AN37	Power/Other	
VSS	AN7	Power/Other	
VSS	AP2	Power/Other	
VSS	AP6	Power/Other	
VSS	AR1	Power/Other	
VSS	AR11	Power/Other	
VSS	AR15	Power/Other	
VSS	AR19	Power/Other	
VSS	AR23	Power/Other	
VSS	AR27	Power/Other	
VSS	AR31	Power/Other	
VSS	AR35	Power/Other	
VSS	AR39	Power/Other	
VSS	AR5	Power/Other	
VSS	AU3	Power/Other	
VSS	AV12	Power/Other	
VSS	AV16	Power/Other	
VSS	AV20	Power/Other	
VSS	AV24	Power/Other	
VSS	AV28	Power/Other	
VSS	AV32	Power/Other	
VSS	AV36	Power/Other	
VSS	AV8	Power/Other	
VSS	B12	Power/Other	

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	B16	Power/Other	
VSS	B20	Power/Other	
VSS	B24	Power/Other	
VSS	B28	Power/Other	
VSS	B32	Power/Other	
VSS	B38	Power/Other	
VSS	B8	Power/Other	
VSS	C35	Power/Other	
VSS	C39	Power/Other	
VSS	D4	Power/Other	
VSS	E11	Power/Other	
VSS	E15	Power/Other	
VSS	E19	Power/Other	
VSS	E23	Power/Other	
VSS	E27	Power/Other	
VSS	E3	Power/Other	
VSS	E31	Power/Other	
VSS	E37	Power/Other	
VSS	F2	Power/Other	
VSS	F6	Power/Other	
VSS	G1	Power/Other	
VSS	G11	Power/Other	
VSS	G15	Power/Other	
VSS	G17	Power/Other	
VSS	G23	Power/Other	
VSS	G27	Power/Other	
VSS	G31	Power/Other	
VSS	G35	Power/Other	
VSS	G5	Power/Other	
VSS	H4	Power/Other	
VSS	H8	Power/Other	
VSS	J3	Power/Other	
VSS	J7	Power/Other	
VSS	K2	Power/Other	
VSS	K6	Power/Other	
VSS	L1	Power/Other	
VSS	L39	Power/Other	
VSS	L5	Power/Other	
VSS	M4	Power/Other	

Table 26. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	M8	Power/Other	
VSS	N3	Power/Other	
VSS	N37	Power/Other	
VSS	N7	Power/Other	
VSS	P2	Power/Other	
VSS	P6	Power/Other	
VSS	R1	Power/Other	
VSS	R5	Power/Other	
VSS	T4	Power/Other	
VSS	T8	Power/Other	
VSS	U3	Power/Other	
VSS	U7	Power/Other	
VSS	V2	Power/Other	
VSS	V38	Power/Other	
VSS	V6	Power/Other	
VSS	W1	Power/Other	
VSS	W5	Power/Other	
VSS	Y4	Power/Other	
VSS	Y8	Power/Other	
VSS_SENSE	R39	Power/Other	Output
VSSA	AV4	Power/Other	

5.1.2 Pin Listing by Pin Number

Table 27 contains a listing of the Pentium 4 processor pins in order by pin number.

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A1	VID4	Power/Other	Output
A3	VID3	Power/Other	Output
A5	SKTOCC#	Power/Other	Output
A7	TESTHI0	Power/Other	Input
A9	A32#	Source Synch	Input/Output
A11	A33#	Source Synch	Input/Output
A13	A27#	Source Synch	Input/Output
A15	A26#	Source Synch	Input/Output
A17	A20#	Source Synch	Input/Output
A19	A30#	Source Synch	Input/Output
A21	A22#	Source Synch	Input/Output
A23	A14#	Source Synch	Input/Output
A25	A13#	Source Synch	Input/Output
A27	A15#	Source Synch	Input/Output
A29	A17#	Source Synch	Input/Output
A31	A11#	Source Synch	Input/Output
A33	LOCK#	Common Clock	Input/Output
A35	TRDY#	Common Clock	Input
A37	VCC	Power/Other	
A39	VCC	Power/Other	
B2	VID1	Power/Other	Output
B4	VID2	Power/Other	Output
B6	VCC	Power/Other	
B8	VSS	Power/Other	
B10	VCC	Power/Other	
B12	VSS	Power/Other	
B14	VCC	Power/Other	
B16	VSS	Power/Other	
B18	VCC	Power/Other	
B20	VSS	Power/Other	
B22	VCC	Power/Other	

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
B24	VSS	Power/Other	
B26	VCC	Power/Other	
B28	VSS	Power/Other	
B30	VCC	Power/Other	
B32	VSS	Power/Other	
B34	DBSY#	Common Clock	Input/Output
B36	BR0#	Common Clock	Input/Output
B38	VSS	Power/Other	
C1	VID0	Power/Other	Output
C3	VCC	Power/Other	
C5	STPCLK#	Asynch GTL+	Input
C7	IERR#	Common Clock	Output
C9	RSP#	Common Clock	Input
C11	A31#	Source Synch	Input/Output
C13	BPM4#	Common Clock	Input/Output
C15	A34#	Source Synch	Input/Output
C17	A21#	Source Synch	Input/Output
C19	A23#	Source Synch	Input/Output
C21	A29#	Source Synch	Input/Output
C23	A10#	Source Synch	Input/Output
C25	A12#	Source Synch	Input/Output
C27	A18#	Source Synch	Input/Output
C29	A4#	Source Synch	Input/Output
C31	A6#	Source Synch	Input/Output
C33	REQ0#	Source Synch	Input/Output
C35	VSS	Power/Other	
C37	VCC	Power/Other	
C39	VSS	Power/Other	
D2	VCC	Power/Other	
D4	VSS	Power/Other	
D6	BPM5#	Common Clock	Input/Output
D8	INIT#	Asynch GTL+	Input

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
D10	MCERR#	Common Clock	Input/Output
D12	A35#	Source Synch	Input/Output
D14	AP1#	Common Clock	Input/Output
D16	TESTHI8	Power/Other	Input
D18	TESTHI9	Power/Other	Input
D20	TESTHI10	Power/Other	Input
D22	A25#	Source Synch	Input/Output
D24	A16#	Source Synch	Input/Output
D26	A19#	Source Synch	Input/Output
D28	A8#	Source Synch	Input/Output
D30	A5#	Source Synch	Input/Output
D32	REQ1#	Source Synch	Input/Output
D34	REQ3#	Source Synch	Input/Output
D36	HITM#	Common Clock	Input/Output
D38	TMS	TAP	Input
E1	VCC	Power/Other	
E3	VSS	Power/Other	
E5	VCC	Power/Other	
E7	BPM3#	Common Clock	Input/Output
E9	VCC	Power/Other	
E11	VSS	Power/Other	
E13	VCC	Power/Other	
E15	VSS	Power/Other	
E17	VCC	Power/Other	
E19	VSS	Power/Other	
E21	VCC	Power/Other	
E23	VSS	Power/Other	
E25	VCC	Power/Other	
E27	VSS	Power/Other	
E29	VCC	Power/Other	
E31	VSS	Power/Other	
E33	VCC	Power/Other	
E35	BNR#	Common Clock	Input/Output
E37	VSS	Power/Other	
E39	THERMDC	Power/Other	
F2	VSS	Power/Other	
F4	VCC	Power/Other	
F6	VSS	Power/Other	
F8	BPM0#	Common Clock	Input/Output

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
F10	BPM2#	Common Clock	Input/Output
F12	BPM1#	Common Clock	Input/Output
F14	GTLREF	Power/Other	Input
F16	AP0#	Common Clock	Input/Output
F18	BINIT#	Common Clock	Input/Output
F20	A28#	Source Synch	Input/Output
F22	A24#	Source Synch	Input/Output
F24	COMP1	Power/Other	Input/Output
F26	A9#	Source Synch	Input/Output
F28	A7#	Source Synch	Input/Output
F30	A3#	Source Synch	Input/Output
F32	REQ4#	Source Synch	Input/Output
F34	REQ2#	Source Synch	Input/Output
F36	ADS#	Common Clock	Input/Output
F38	PROCHOT#	Asynch GTL+	Output
G1	VSS	Power/Other	
G3	VCC	Power/Other	
G5	VSS	Power/Other	
G7	VCC	Power/Other	
G9	VCC	Power/Other	
G11	VSS	Power/Other	
G13	VCC	Power/Other	
G15	VSS	Power/Other	
G17	VSS	Power/Other	
G19	VCC	Power/Other	
G21	ADSTB1#	Source Synch	Input/Output
G23	VSS	Power/Other	
G25	ADSTB0#	Source Synch	Input/Output
G27	VSS	Power/Other	
G29	VCC	Power/Other	
G31	VSS	Power/Other	
G33	VCC	Power/Other	
G35	VSS	Power/Other	
G37	DRDY#	Common Clock	Input/Output
G39	VCC	Power/Other	
H2	VCC	Power/Other	
H4	VSS	Power/Other	
H6	VCC	Power/Other	
H8	VSS	Power/Other	

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
H36	LINT0	Asynch GTL+	Input
H38	THERMDA	Power/Other	
J1	VCC	Power/Other	
J3	VSS	Power/Other	
J5	VCC	Power/Other	
J7	VSS	Power/Other	
J35	DEFER#	Common Clock	Input
J37	VCC	Power/Other	
J39	TDI	TAP	Input
K2	VSS	Power/Other	
K4	VCC	Power/Other	
K6	VSS	Power/Other	
K8	VCC	Power/Other	
K36	HIT#	Common Clock	Input/Output
K38	SMI#	Asynch GTL+	Input
L1	VSS	Power/Other	
L3	VCC	Power/Other	
L5	VSS	Power/Other	
L7	VCC	Power/Other	
L35	VCC	Power/Other	
L37	BPRI#	Common Clock	Input
L39	VSS	Power/Other	
M2	VCC	Power/Other	
M4	VSS	Power/Other	
M6	VCC	Power/Other	
M8	VSS	Power/Other	
M36	RS0#	Common Clock	Input
M38	IGNNE#	Asynch GTL+	Input
N1	VCC	Power/Other	
N3	VSS	Power/Other	
N5	VCC	Power/Other	
N7	VSS	Power/Other	
N35	RS1#	Common Clock	Input
N37	VSS	Power/Other	
N39	VCC_SENSE	Power/Other	Output
P2	VSS	Power/Other	
P4	VCC	Power/Other	
P6	VSS	Power/Other	
P8	VCC	Power/Other	

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
P36	TDO	TAP	Output
P38	FERR#	Asynch GTL+	Output
R1	VSS	Power/Other	
R3	VCC	Power/Other	
R5	VSS	Power/Other	
R7	VCC	Power/Other	
R35	TRST#	TAP	Input
R37	TCK	TAP	Input
R39	VSS_SENSE	Power/Other	Output
T2	VCC	Power/Other	
T4	VSS	Power/Other	
T6	VCC	Power/Other	
T8	VSS	Power/Other	
T36	GTLREF	Power/Other	Input
T38	A20M#	Asynch GTL+	Input
U1	VCC	Power/Other	
U3	VSS	Power/Other	
U5	VCC	Power/Other	
U7	VSS	Power/Other	
U35	RS2#	Common Clock	Input
U37	THERMTRIP#	Asynch GTL+	Output
U39	VCC	Power/Other	
V2	VSS	Power/Other	
V4	VCC	Power/Other	
V6	VSS	Power/Other	
V8	VCC	Power/Other	
V36	D6#	Source Synch	Input/Output
V38	VSS	Power/Other	
W1	VSS	Power/Other	
W3	VCC	Power/Other	
W5	VSS	Power/Other	
W7	VCC	Power/Other	
W35	LINT1	Asynch GTL+	Input
W37	D2#	Source Synch	Input/Output
W39	D8#	Source Synch	Input/Output
Y2	VCC	Power/Other	
Y4	VSS	Power/Other	
Y6	VCC	Power/Other	
Y8	VSS	Power/Other	

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
Y36	VCC	Power/Other	
Y38	D0#	Source Synch	Input/Output
AA1	VCC	Power/Other	
AA3	VSS	Power/Other	
AA5	VCC	Power/Other	
AA7	VSS	Power/Other	
AA35	D5#	Source Synch	Input/Output
AA37	VSS	Power/Other	
AA39	D15#	Source Synch	Input/Output
AB2	VSS	Power/Other	
AB4	VCC	Power/Other	
AB6	VSS	Power/Other	
AB8	VCC	Power/Other	
AB36	D10#	Source Synch	Input/Output
AB38	VCC	Power/Other	
AC1	VSS	Power/Other	
AC3	VCC	Power/Other	
AC5	VSS	Power/Other	
AC7	VCC	Power/Other	
AC35	GTLREF	Power/Other	Input
AC37	D14#	Source Synch	Input/Output
AC39	VSS	Power/Other	
AD2	VCC	Power/Other	
AD4	VSS	Power/Other	
AD6	VCC	Power/Other	
AD8	VSS	Power/Other	
AD36	D1#	Source Synch	Input/Output
AD38	D11#	Source Synch	Input/Output
AE1	VCC	Power/Other	
AE3	VSS	Power/Other	
AE5	VCC	Power/Other	
AE7	VSS	Power/Other	
AE35	VCC	Power/Other	
AE37	D3#	Source Synch	Input/Output
AE39	D9#	Source Synch	Input/Output
AF2	VSS	Power/Other	
AF4	VCC	Power/Other	
AF6	VSS	Power/Other	
AF8	VCC	Power/Other	

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AF36	VSS	Power/Other	
AF38	D7#	Source Synch	Input/Output
AG1	VSS	Power/Other	
AG3	VCC	Power/Other	
AG5	VSS	Power/Other	
AG7	VCC	Power/Other	
AG35	DSTBN0#	Source Synch	Input/Output
AG37	VCC	Power/Other	
AG39	D4#	Source Synch	Input/Output
AH2	VCC	Power/Other	
AH4	VSS	Power/Other	
AH6	VCC	Power/Other	
AH8	VSS	Power/Other	
AH36	D12#	Source Synch	Input/Output
AH38	VSS	Power/Other	
AJ1	VCC	Power/Other	
AJ3	VSS	Power/Other	
AJ5	VCC	Power/Other	
AJ7	VSS	Power/Other	
AJ35	DSTBP0#	Source Synch	Input/Output
AJ37	D13#	Source Synch	Input/Output
AJ39	VCC	Power/Other	
AK2	VSS	Power/Other	
AK4	VCC	Power/Other	
AK6	VSS	Power/Other	
AK8	VCC	Power/Other	
AK36	D24#	Source Synch	Input/Output
AK38	D17#	Source Synch	Input/Output
AL1	VSS	Power/Other	
AL3	VCC	Power/Other	
AL5	VSS	Power/Other	
AL7	VCC	Power/Other	
AL35	VSS	Power/Other	
AL37	D31#	Source Synch	Input/Output
AL39	DBI0#	Source Synch	Input/Output
AM2	VCC	Power/Other	
AM4	VSS	Power/Other	
AM6	VCC	Power/Other	
AM8	VSS	Power/Other	

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AM36	VCC	Power/Other	
AM38	D20#	Source Synch	Input/Output
AN1	VCC	Power/Other	
AN3	VSS	Power/Other	
AN5	VCC	Power/Other	
AN7	VSS	Power/Other	
AN35	D27#	Source Synch	Input/Output
AN37	VSS	Power/Other	
AN39	D23#	Source Synch	Input/Output
AP2	VSS	Power/Other	
AP4	VCC	Power/Other	
AP6	VSS	Power/Other	
AP8	BCLK1	System Bus Clk	Input
AP10	GTLREF	Power/Other	Input
AP12	D63#	Source Synch	Input/Output
AP14	D61#	Source Synch	Input/Output
AP16	DSTBP3#	Source Synch	Input/Output
AP18	DSTBN3#	Source Synch	Input/Output
AP20	DSTBP2#	Source Synch	Input/Output
AP22	DSTBN2#	Source Synch	Input/Output
AP24	D41#	Source Synch	Input/Output
AP26	D35#	Source Synch	Input/Output
AP28	D43#	Source Synch	Input/Output
AP30	DSTBP1#	Source Synch	Input/Output
AP32	DSTBN1#	Source Synch	Input/Output
AP34	D18#	Source Synch	Input/Output
AP36	D22#	Source Synch	Input/Output
AP38	VCC	Power/Other	
AR1	VSS	Power/Other	
AR3	VCC	Power/Other	
AR5	VSS	Power/Other	
AR7	BCLK0	Bus Clk	Input
AR9	VCC	Power/Other	
AR11	VSS	Power/Other	
AR13	VCC	Power/Other	
AR15	VSS	Power/Other	
AR17	VCC	Power/Other	
AR19	VSS	Power/Other	
AR21	VCC	Power/Other	

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AR23	VSS	Power/Other	
AR25	VCC	Power/Other	
AR27	VSS	Power/Other	
AR29	VCC	Power/Other	
AR31	VSS	Power/Other	
AR33	VCC	Power/Other	
AR35	VSS	Power/Other	
AR37	D25#	Source Synch	Input/Output
AR39	VSS	Power/Other	
AT2	VCC	Power/Other	
AT4	RESERVED		
AT6	TESTHI2	Power/Other	Input
AT8	TESTHI3	Power/Other	Input
AT10	TESTHI1	Power/Other	Input
AT12	D60#	Source Synch	Input/Output
AT14	D57#	Source Synch	Input/Output
AT16	D55#	Source Synch	Input/Output
AT18	D53#	Source Synch	Input/Output
AT20	D49#	Source Synch	Input/Output
AT22	DBI2#	Source Synch	Input/Output
AT24	D45#	Source Synch	Input/Output
AT26	DP3#	Common Clock	Input/Output
AT28	D40#	Source Synch	Input/Output
AT30	D39#	Source Synch	Input/Output
AT32	D33#	Source Synch	Input/Output
AT34	D30#	Source Synch	Input/Output
AT36	D16#	Source Synch	Input/Output
AT38	D26#	Source Synch	Input/Output
AU1	ITP_CLK0	TAP	Input
AU3	VSS	Power/Other	
AU5	VCCA	Power/Other	
AU7	TESTHI4	Power/Other	Input
AU9	TESTHI5	Power/Other	Input
AU11	TESTHI5	Power/Other	Input
AU13	D59#	Source Synch	Input/Output
AU15	D56#	Source Synch	Input/Output
AU17	D54#	Source Synch	Input/Output
AU19	D48#	Source Synch	Input/Output
AU21	D50#	Source Synch	Input/Output

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AU23	D47#	Source Synch	Input/Output
AU25	D42#	Source Synch	Input/Output
AU27	COMP0	Power/Other	Input/Output
AU29	D34#	Source Synch	Input/Output
AU31	D38#	Source Synch	Input/Output
AU33	D36#	Source Synch	Input/Output
AU35	D28#	Source Synch	Input/Output
AU37	DBI1#	Source Synch	Input/Output
AU39	D21#	Source Synch	Input/Output
AV2	DBR#	Asynch GTL+	Output
AV4	VSSA	Power/Other	
AV6	VCC	Power/Other	
AV8	VSS	Power/Other	
AV10	VCC	Power/Other	
AV12	VSS	Power/Other	
AV14	VCC	Power/Other	
AV16	VSS	Power/Other	
AV18	VCC	Power/Other	
AV20	VSS	Power/Other	
AV22	VCC	Power/Other	
AV24	VSS	Power/Other	
AV26	VCC	Power/Other	
AV28	VSS	Power/Other	
AV30	VCC	Power/Other	
AV32	VSS	Power/Other	
AV34	VCC	Power/Other	
AV36	VSS	Power/Other	
AV38	VCC	Power/Other	
AW1	ITP_CLK1	TAP	Input
AW3	VCCIOPLL	Power/Other	
AW5	TESTHI7	Power/Other	Input
AW7	SLP#	Asynch GTL+	Input
AW9	PWRGOOD	Asynch GTL+	Input
AW11	RESET#	Common Clock	Input
AW13	D58#	Source Synch	Input/Output
AW15	DBI3#	Source Synch	Input/Output
AW17	D62#	Source Synch	Input/Output
AW19	D52#	Source Synch	Input/Output
AW21	D51#	Source Synch	Input/Output

Table 27. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AW23	D46#	Source Synch	Input/Output
AW25	D44#	Source Synch	Input/Output
AW27	DP2#	Common Clock	Input/Output
AW29	D37#	Source Synch	Input/Output
AW31	D32#	Source Synch	Input/Output
AW33	DP0#	Common Clock	Input/Output
AW35	DP1#	Common Clock	Input/Output
AW37	D19#	Source Synch	Input/Output
AW39	D29#	Source Synch	Input/Output

5.2 Alphabetical Signals Reference

Table 28. Signal Description (Page 1 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A[35:3]#</td><td>Input/ Output</td><td>A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Pentium 4 processor in the 423-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#.
On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 7.1 for more details.</td></tr>
<tr><td>A20M#</td><td>Input</td><td>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/ write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.
A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>ADS#</td><td>Input/ Output</td><td>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td></tr>
<tr><td>ADSTB[1:0]#</td><td>Input/ Output</td><td>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB0#</td></tr>
<tr><td>A[35:17]#</td><td>ADSTB1#</td></tr>
</table></td></tr>
<tr><td>AP[1:0]#</td><td>Input/ Output</td><td>AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processor system bus agents. The following table defines the coverage model of these signals.
<table>
<tr><th>Request Signals</th><th>subphase 1</th><th>subphase 2</th></tr>
<tr><td>A[35:24]#</td><td>AP0#</td><td>AP1#</td></tr>
<tr><td>A[23:3]#</td><td>AP1#</td><td>AP0#</td></tr>
<tr><td>REQ[4:0]#</td><td>AP1#</td><td>AP0#</td></tr>
</table></td></tr>
<tr><td>BCLK[1:0]</td><td>Input</td><td>The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.</td></tr>
</table>

Table 28. Signal Description (Page 2 of 8)

Name	Type	Description
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Pentium 4 processor system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Please refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for more detailed information. **These signals do not have on-die termination and must be terminated on the system board.**
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. **This signal does not have on-die termination and must be terminated.**
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to Table 9 in Chapter 2.0.

Table 28. Signal Description (Page 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#.
Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN#/ DSTBP#</th><th>DBI#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBI[3:0]#</td><td>Input/ Output</td><td>DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DBI[3:0] Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DBI3#</td><td>D[63:48]#</td></tr>
<tr><td>DBI2#</td><td>D[47:32]#</td></tr>
<tr><td>DBI1#</td><td>D[31:16]#</td></tr>
<tr><td>DBI0#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor system bus agents.</td></tr>
</table>

Table 28. Signal Description (Page 4 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DRDY#</td><td>Input/ Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr>
</table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr>
</table></td></tr>
<tr><td>FERR#</td><td>Output</td><td>FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.</td></tr>
<tr><td>GTLREF</td><td>Input</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CC}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide for more information.</td></tr>
<tr><td>HIT#

HITM#</td><td>Input/ Output

Input/ Output</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td></tr>
<tr><td>IERR#</td><td>Output</td><td>IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
This signal does not have on-die termination and must be terminated on the system board.</td></tr>
<tr><td>IGNNE#</td><td>Input</td><td>IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set.
IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
</table>

Table 28. Signal Description (Page 5 of 8)

Name	Type	Description
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum tested operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. See Section 7.3 for more details.

Table 28. Signal Description (Page 6 of 8)

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 10 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 13, and be followed by a 1 to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated on the system board.**
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.

Table 28. Signal Description (Page 7 of 8)

Name	Type	Description
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[10:0]	Input	TESTHI[10:0] must be connected to a V_{CC} power source through 1-10 kΩ resistors for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 7.3.1.
THERMDC	Other	Thermal Diode Cathode. See Section 7.3.1.
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 Ω pull-down resistor.
V_{CCA}	Input	V_{CCA} provides isolated power for the internal processor core PLL's. Refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for complete implementation details.
$V_{CCIOPLL}$	Input	$V_{CCIOPLL}$ provides isolated power for internal processor system bus PLL's. Follow the guidelines for V_{CCA}, and refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for complete implementation details.
$V_{CCSENSE}$	Output	$V_{CCSENSE}$ is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure power near the silicon with little noise.

Table 28. Signal Description (Page 8 of 8)

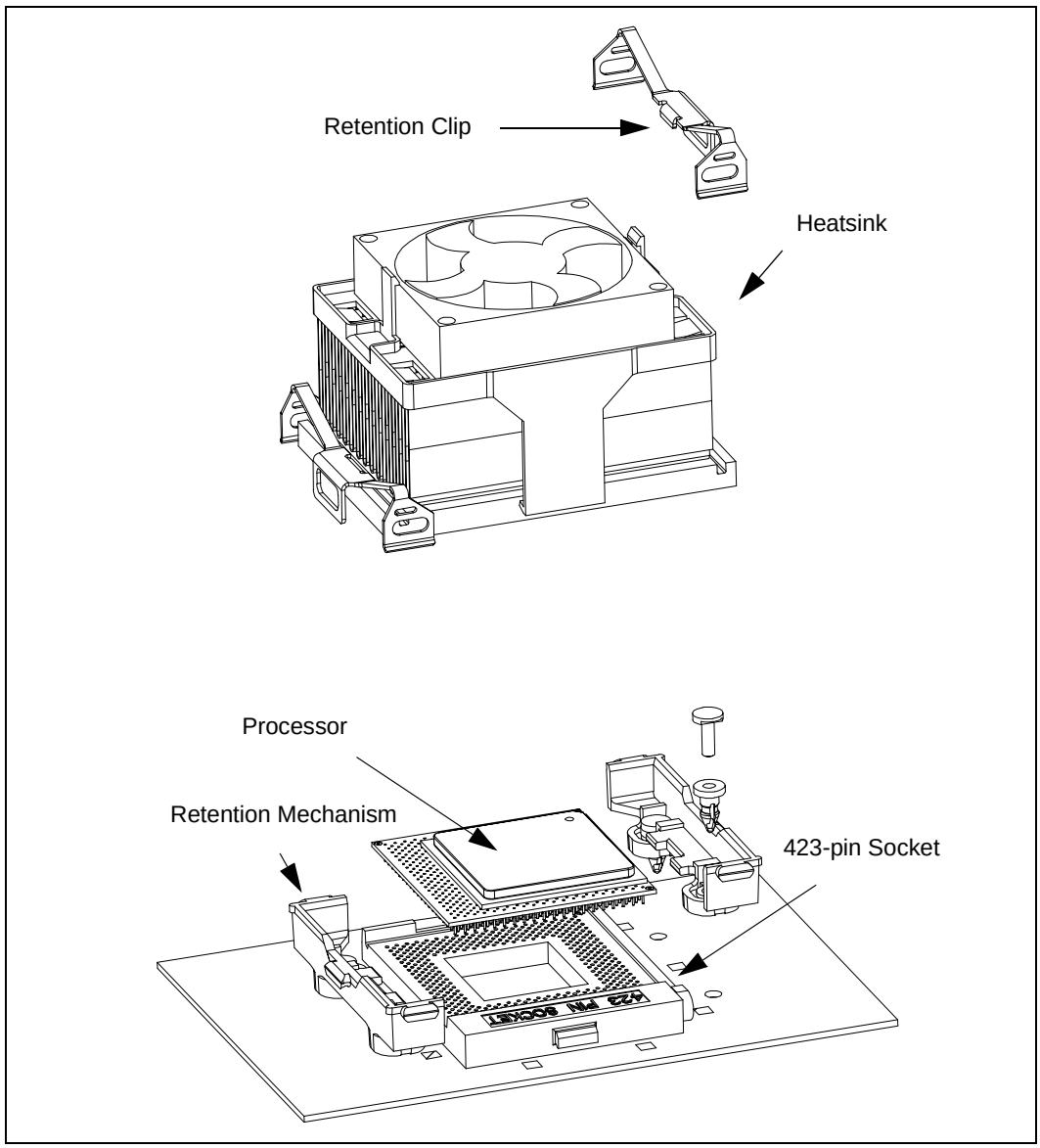
Name	Type	Description
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
V_{SSA}	Input	V_{SSA} is the isolated ground for internal PLL's.
$V_{SSSENSE}$	Output	$V_{SSSENSE}$ is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise

6.0 Thermal Specifications and Design Considerations

Intel® Pentium® 4 Processor in the 423-pin Package use an integrated thermal heat spreader for heatsink attachment which is intended to provide for multiple types of thermal solutions. This section will provide data necessary for development of a thermal solution. See Figure 23 for an exploded view of an example Pentium 4 processor thermal solution. This is for illustration purposes only. For further thermal solution design details, please refer to the *Intel® Pentium® 4 Processor Thermal Design Guidelines*.

Note: The processor is either shipped by itself or with a heatsink for boxed processors. See Chapter 8.0 for details on boxed processors.

Figure 23. Example Thermal Solution (Not to scale)



6.1 Thermal Specifications

Table 29 specifies the thermal design power dissipation envelope for Pentium 4 processors. Analysis indicates that real applications are unlikely to cause the processor to consume its maximum possible power consumption. Intel recommends that system thermal designs target the "Thermal Design Power" indicated in Table 29. The Thermal Monitor feature (refer to Section 7.3) is intended to protect the processor from overheating when running high power code that exceeds the recommendations in this table. For more details on the usage of this feature, refer to Section 7.3. **In all cases the Thermal Monitor feature must be enabled for the processor to be in specification.** Table 29 also lists the maximum and minimum processor temperature specifications for T_{CASE}. A thermal solution should be designed to ensure the temperature of the processor never exceeds these specifications.

Table 29. Processor Thermal Design Power

Processor and Core Frequency (MHz)	Thermal Design Power (W)[2]	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
1.30 GHz	48.9	5	69	1
1.40 GHz	51.8	5	70	1
1.50 GHz	54.7	5	72	1

NOTES:
1. These values are specified at V_{CC_MID} for the processor. Systems must be designed to ensure that the processor not be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MID} + 0.055*(1 - I_{CC}/I_{CC_MAX}) [V]
2. The numbers in this column reflect Intel's recommended design point and are not indicative of the maximum power the processor can dissipate under worst case conditions. For more details refer to the *Intel® Pentium® 4 Processor Thermal Design Guidelines*.

6.2 Thermal Analysis

6.2.1 Measurements For Thermal Specifications

6.2.1.1 Processor Case Temperature Measurement

The maximum and minimum case temperature (T_{CASE}) for the Pentium 4 processor is specified in Table 29. This temperature specification is meant to ensure correct and reliable operation of the processor. Figure 24 illustrates where Intel recommends that T_{CASE} thermal measurements should be made. Figures 25 and 26 illustrate two possible measuring techniques. Refer to the *Intel® Pentium® 4 Processor Thermal Design Guidelines* for more information.

Figure 24. Guideline Locations for Case Temperature (T_{CASE}) Thermocouple Placement

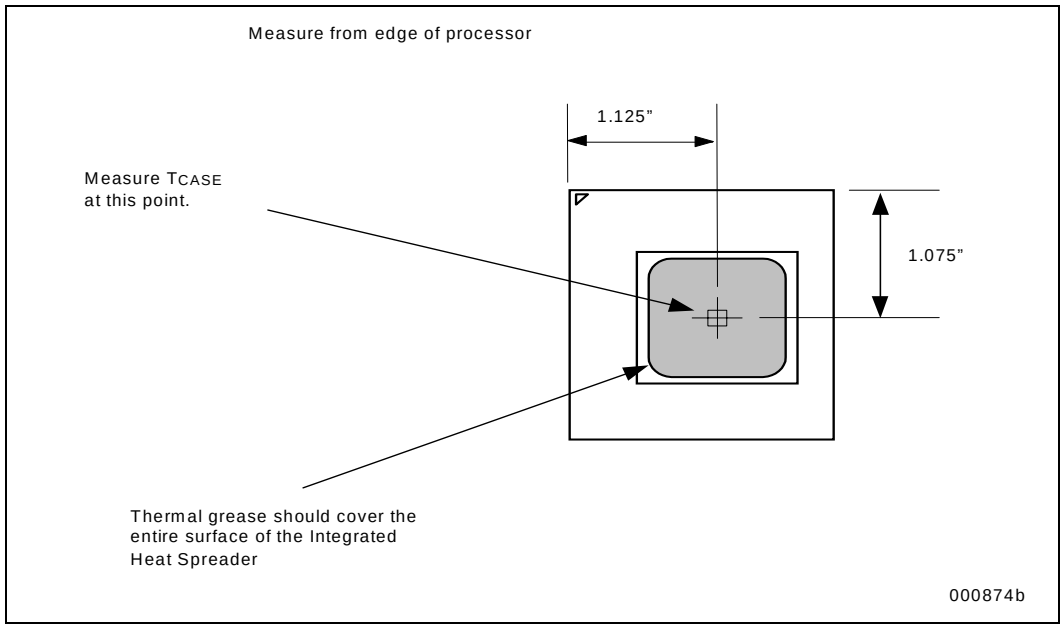


Figure 25. Technique for Measuring with 0 Degree Angle Attachment

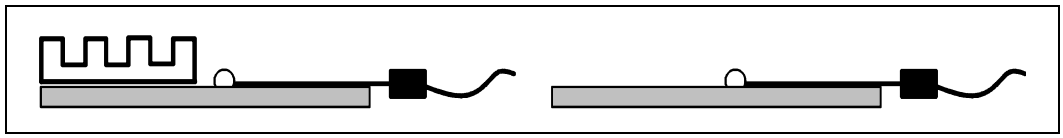
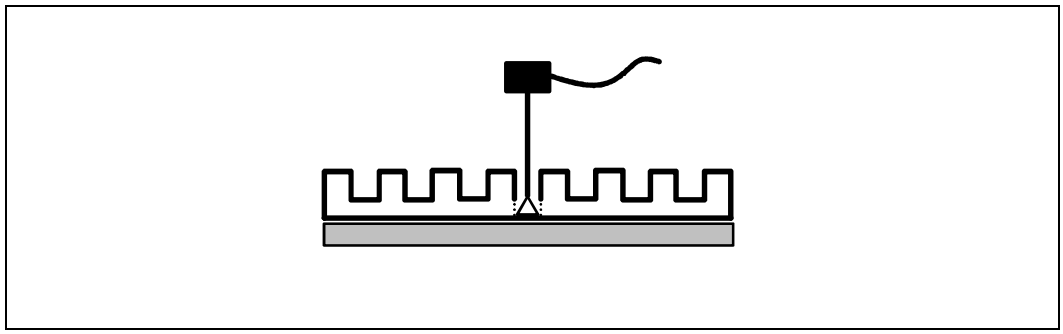


Figure 26. Technique for Measuring with 90 Degree Angle Attachment



7.0 Features

7.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Intel® Pentium® 4 Processor in the 423-pin Package sample its hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, please refer to Table 30.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except during another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a “warm” reset and a “power-on” reset.

Table 30. Power-On Configuration Option Pins

Configuration Option	Pin[1]
Output tristate	SMI#
Execute BIST	INIT#
In Order Queue pipelining (set IOQ depth to 1)	A7#
Disable MCERR# observation	A9#
Disable BINIT# observation	A10#
APIC Cluster ID (0-3)	A[12:11]#
Disable bus parking	A15#
Symmetric agent arbitration ID	BR0#

NOTE:
1. Asserting this signal during RESET# will select the corresponding option.

7.2 Clock Control and Low Power States

The use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states is allowed in Pentium 4 processor based systems to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 27 for a visual representation of the processor low power states.

7.2.1 Normal State—State 1

This is the normal operating state for the processor.

7.2.2 AutoHALT Powerdown State—State 2

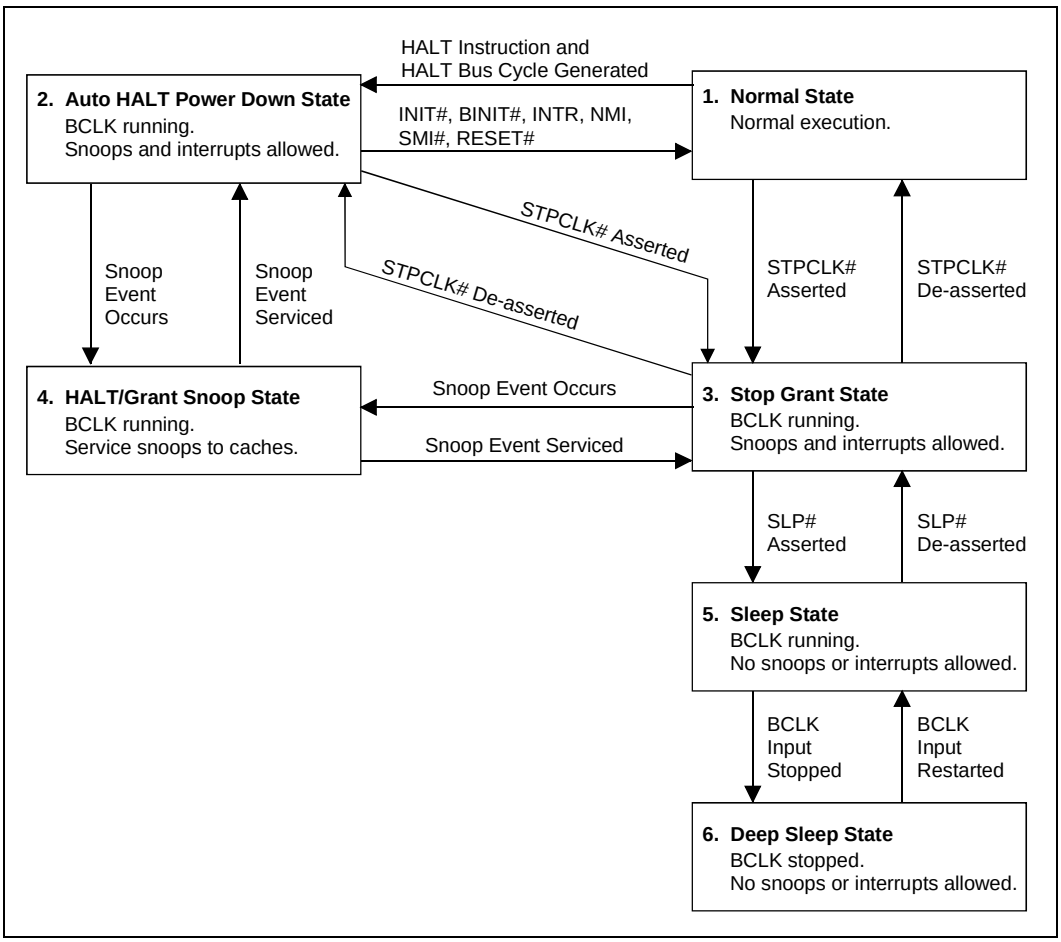
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer’s Manual, Volume III: System Programmer’s Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process bus snoops.

Figure 27. Stop Clock State Machine



7.2.3 Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop Grant state from the Sleep state, STPCLK# should only be de-asserted one or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 7.2.4). A transition to the Sleep state (see Section 7.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process a system bus snoop.

7.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

7.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the processor is in the Stop Grant state. SLP# assertions while the processor is not in the Stop Grant state is out of specification and may result in illegal operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behaviour.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK[1:0] inputs. (See Section 7.2.6). Once in the Sleep or Deep Sleep states, the SLP# pin must be de-asserted if another asynchronous system bus event needs to occur. The SLP# pin has a minimum assertion of one BCLK period.

When the processor is in Sleep state, it will not respond to interrupts or snoop transactions.

7.2.6 Deep Sleep State—State 6

Deep Sleep state is the lowest power state the processor can enter while maintaining context. Deep Sleep state is entered by stopping the BCLK[1:0] inputs (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK[1:0] is stopped. To provide maximum power conservation hold the BLCK0 input at V_{OL} and the BCLK1 input at V_{OH} during the Deep Sleep state. Stopping the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BLCK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behaviour.

When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions.

7.3 Thermal Monitor

Thermal Monitor is a new feature found in the Pentium 4 processor which allows system designers to design lower cost thermal solutions, without compromising system integrity or reliability. By using a factory-tuned, precision on-die thermal sensor, and a fast acting thermal control circuit (TCC), the processor, without the aid of any additional software or hardware, can keep the processors' die temperature within factory specifications under typical real world operating conditions. Thermal Monitor thus allows the processor and system thermal solutions to be designed much closer to the power envelopes of real applications, instead of being designed to the much higher maximum theoretical processor power envelopes.

Thermal Monitor controls the processor temperature by modulating the internal processor core clocks. The processor clocks are modulated when the TCC is activated. Thermal Monitor uses two modes to activate the TCC. Automatic mode and On-Demand mode. **Setting the Automatic Thermal Control Circuit Enable bit by the BIOS is a required specification.** Once automatic mode is enabled, the TCC will activate only when the internal die temperature is very near the temperature limits of the processor. When TCC is enabled, and a high temperature situation exists (i.e. TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a a 50% duty cycle. Clocks will not be off or on more than 3 µs when TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. Once the temperature has returned to a non-critical level, and the hysteresis timer has expired, modulation ceases and TCC goes inactive. Processor performance will be decreased by ~50% when the TCC is active (assuming a 50% duty cycle), however, with a properly designed and characterised thermal solution the TCC most likely will only be activated briefly when the system is near maximum temperature and during the most power intensive applications.

For automatic mode, the 50% duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers or interrupt handling routines.

The TCC may also be activated via On-Demand mode. If bit 4 of the ACPI Thermal Monitor Control Register is written to a "1" the TCC will be activated immediately, independent of the processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Thermal Monitor Control Register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used at the same time Automatic mode is enabled, however, if the system tries to enable the TCC via On-Demand mode at the same time automatic mode is enabled AND a high temperature condition exists, the 50% duty cycle of the automatic mode will override the duty cycle selected by the On-Demand mode.

An external signal, PROCHOT# (processor hot) is asserted any time the TCC is active (either in Automatic or On-Demand mode). Bus snooping and interrupt latching are also active while the TCC is active. The temperature at which the thermal control circuit activates is not user configurable and is not software visible.

Besides the thermal sensor and thermal control circuit, the Thermal Monitor feature also includes one ACPI register, one performance counter register, three model specific registers (MSR), and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Thermal Monitor feature. Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT# (i.e. upon the activation/deactivation of TCC).

If automatic mode is disabled the processor will be operating out of specification and cannot be guaranteed to provide reliable results. Regardless of enabling of the automatic or On-Demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 135 °C. At this point the system bus signal THERMTRIP# will go active and stay active until the processor has cooled down and RESET# has been initiated. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

7.3.1 Thermal Diode

The Pentium 4 processor incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the Pentium 4 processor for thermal management/long term die temperature change purposes. Table 31 and Table 32 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 31. Thermal Diode Parameters

Symbol	Min	Typ	Max	Unit	Notes[1]
$I_{forward\ bias}$	5		450	uA	2
n_ideality	0.9933	1.0045	1.0368		3, 4

NOTES:
1. Not 100% tested. Specified by design characterization.
2. Intel does not support or recommend operation of the thermal diode under reverse bias.
3. At room temperature with a forward bias of 630 mV.
4. n_ideality is the diode ideality factor parameter, as represented by the diode equation: I=Io(e (Vd*q)/(nkT) - 1).

Table 32. Thermal Diode Interface

Pin Name	Pin Number	Pin Description
THERMDA	H38	diode anode
THERMDC	E39	diode cathode

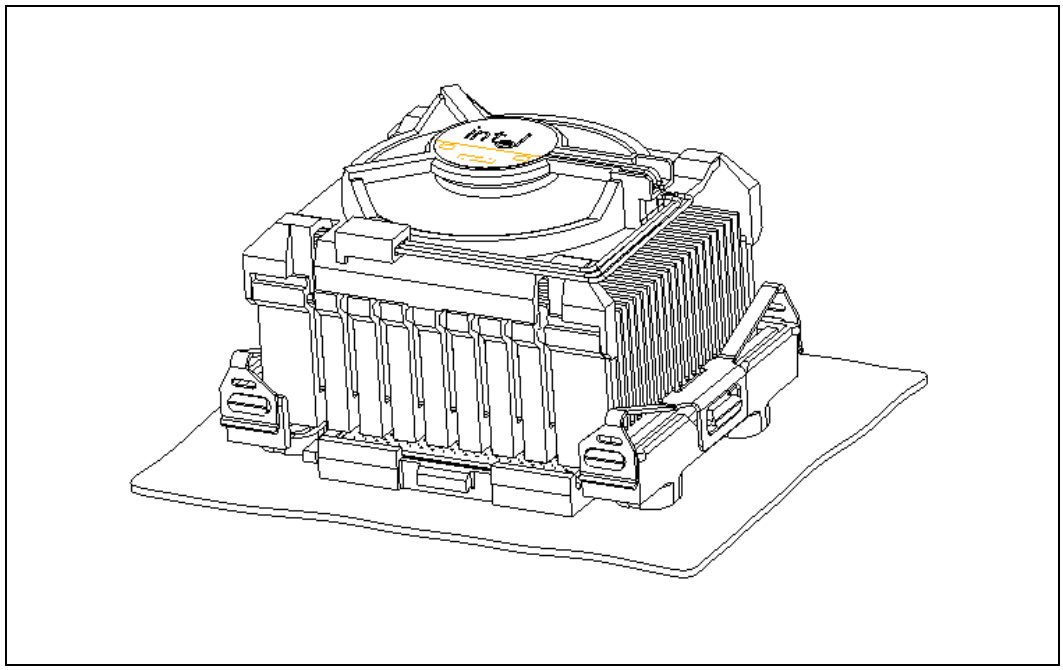
8.0 Boxed Processor Specifications

8.1 Introduction

The Intel® Pentium® 4 Processor in the 423-pin Package is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from system boards and components. The boxed Pentium 4 processor will be supplied with a cooling solution. This chapter documents platform and system requirements for the cooling solution that will be supplied with the boxed Pentium 4 processor. This chapter is particularly important for OEMs that manufacture platforms for system integrators. Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and in inches [in brackets]. Figure 28 shows a mechanical representation of a boxed Pentium 4 processor.

***NOTE* Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platform and chassis.**

Figure 28. Mechanical Representation of the Boxed Pentium 4 Processor



Note: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

8.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Pentium 4 processor fan heatsink.

8.2.1 Boxed Processor Fan Heatsink Dimensions

The boxed processor will be shipped with an unattached fan heatsink. Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling (see Figure 33 and Figure 34). The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 29 (Side Views), and Figure 30 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new platform and system designs. Airspace requirements are shown in Figure 33 and Figure 34. Note that some figures have datum shown (marked with alphabetic designations) to clarify relative dimensioning.

Figure 29. Side View Space Requirements for the Boxed Processor

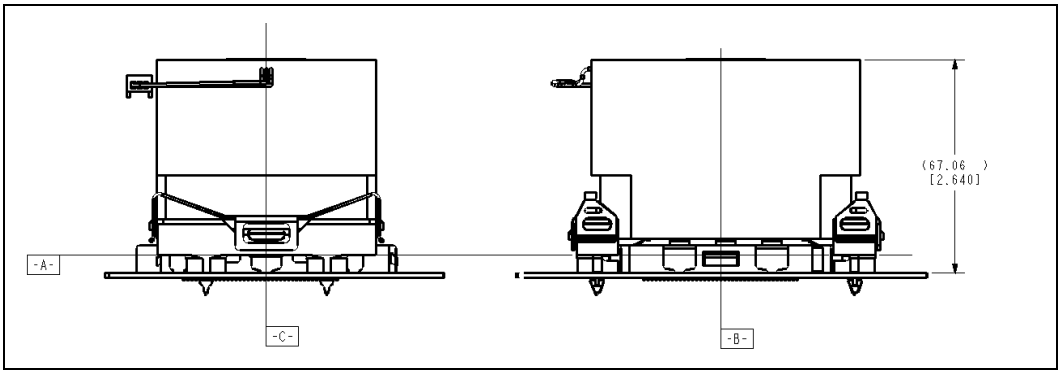
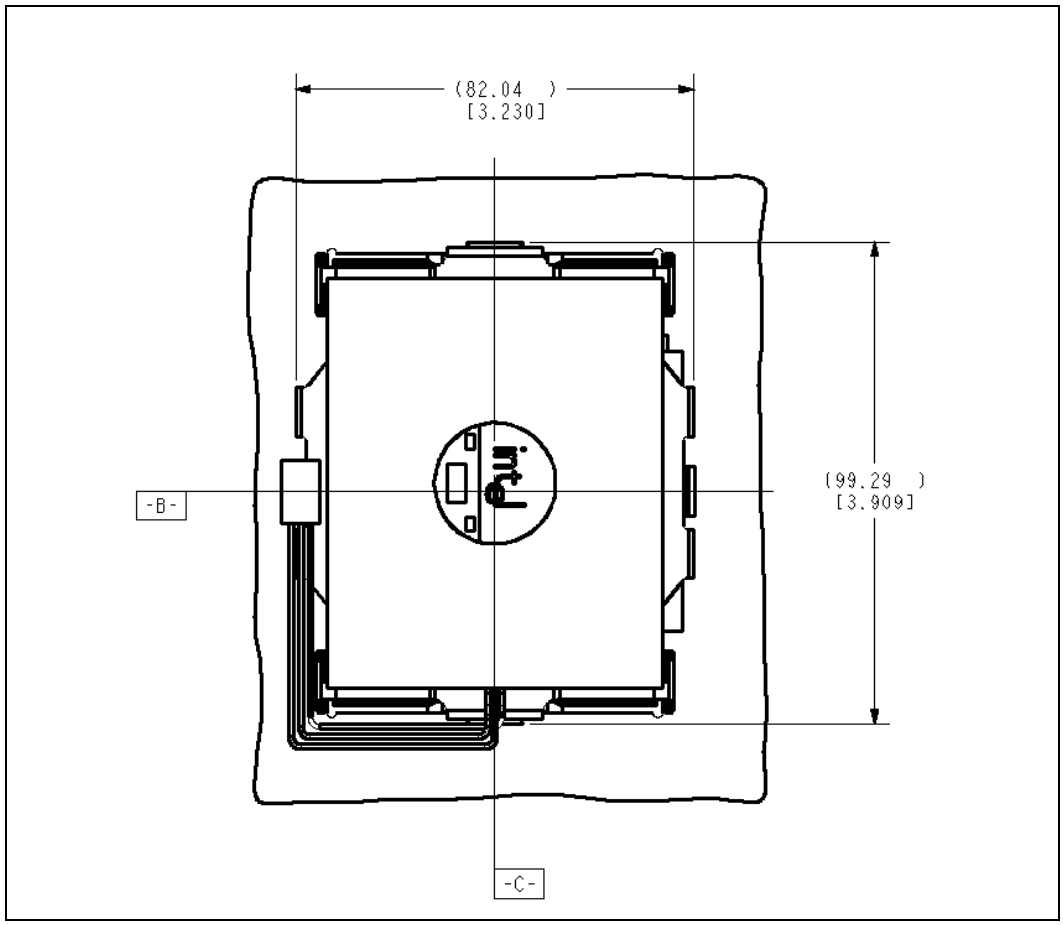


Figure 30. Top View Space Requirements for the Boxed Processor



8.2.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 450 grams. See Chapter 4.0 and the *Intel® Pentium® 4 Processor Thermal Design Guidelines* for details on the processor weight and heatsink requirements. The boxed Pentium 4 processor requires direct-attach of the retention mechanism to the chassis wall, as described in the *Intel® Pentium® 4 Processor Thermal-Mechanical Design Guide*.

8.2.3 Boxed Processor Retention Mechanism and Fan Heatsink Supports

The boxed processor requires processor retention mechanisms to secure the processor in the baseboard socket. The boxed processor will not ship with retention mechanisms, or cooling solution retention clips. Platforms designed for use by system integrators should include retention mechanisms, and clips that support the boxed Pentium 4 processor. System board documentation should include appropriate retention mechanism installation instructions.

8.3 Boxed Processor Requirements

8.3.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12V power supply. A fan power cable will be shipped with the boxed processor to draw power from a power header on the system board. The power cable connector and pinout are shown in Figure 31. Platforms must provide a matched power header to support the boxed processor. Table 33 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. A system board pull-up resistor provides VOH to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 32 shows the location of the fan power connector relative to the processor socket. The system board power header should be positioned within 4.33 inches from the center of the processor socket.

Figure 31. Boxed Processor Fan Heatsink Power Cable Connector Description

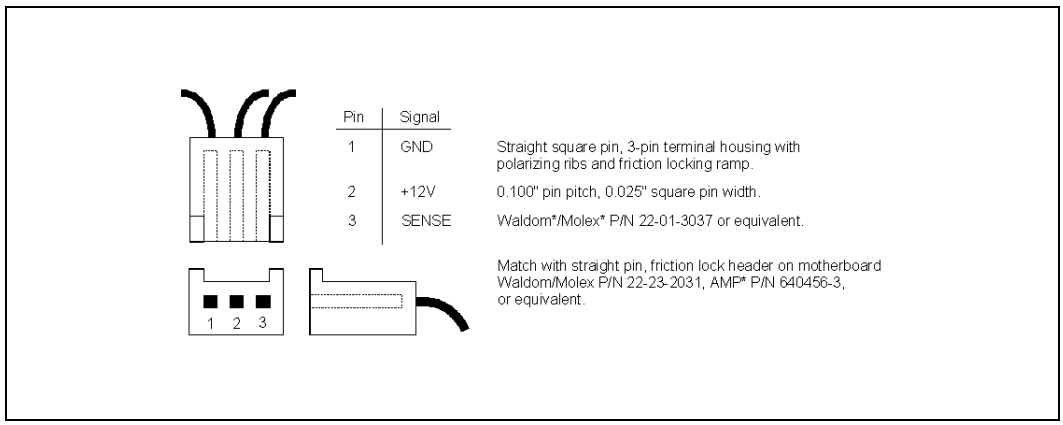
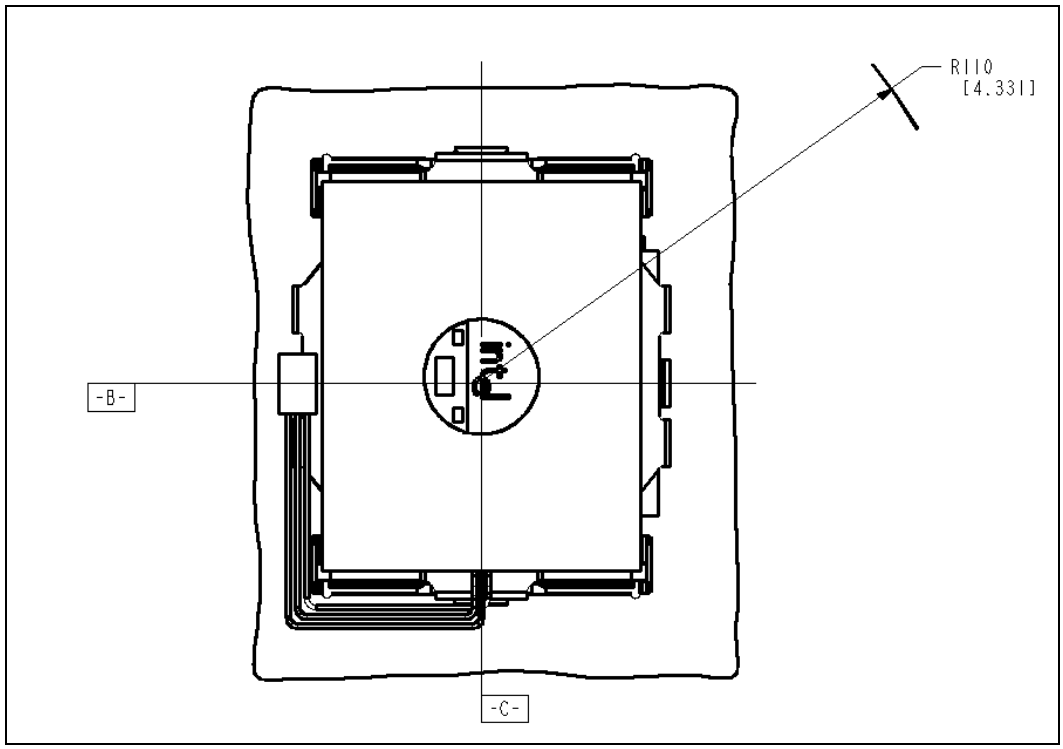


Table 33. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12V: 12 volt fan power supply	10.2	12	13.8	V	
IC: Fan current draw			300	mA	
SENSE: SENSE frequency		2		pulses/ rev	1

NOTE:
1. System board should pull this pin up to V_{CC} with a resistor.

Figure 32. Acceptable System Board Power Header Placement Relative to Processor Socket



8.4 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution utilized by the boxed processor.

8.4.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 6.0 of this document. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 29) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 33 and Figure 34 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan should be kept below 40°C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

Figure 33. Boxed Processor Fan Heatsink Airspace Keepout Requirements (side 1 view)

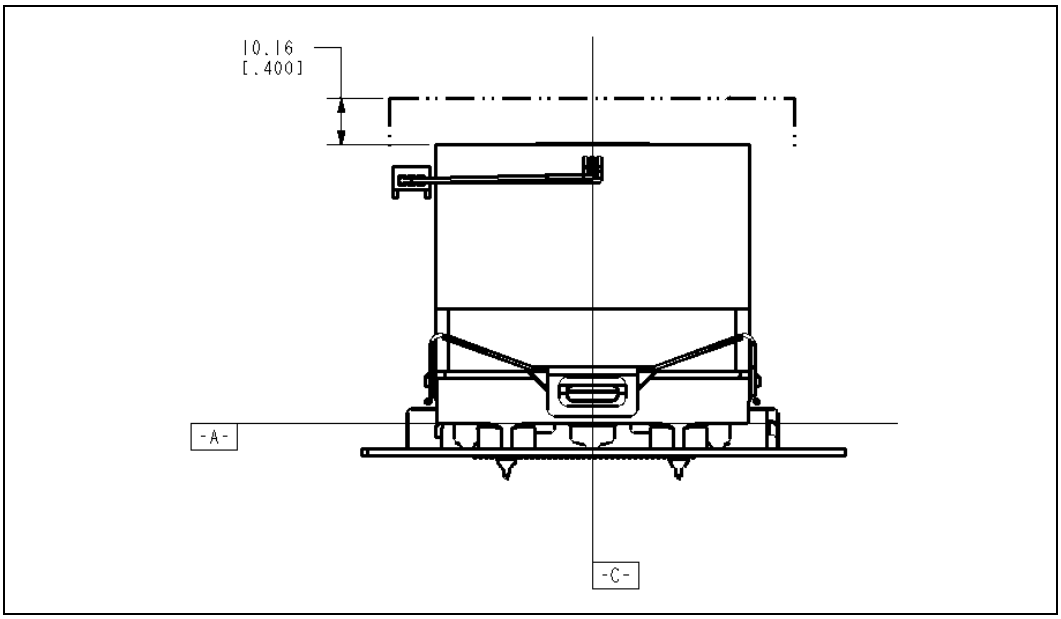
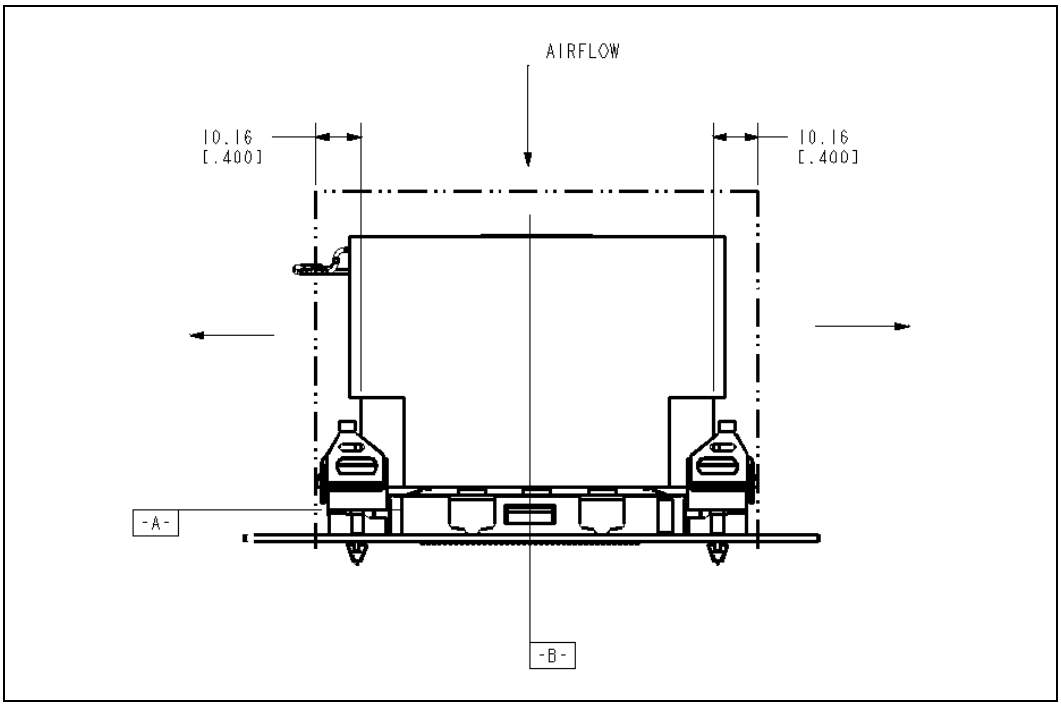


Figure 34. Boxed Processor Fan Heatsink Airspace Keepout Requirements (side 2 view)



8.4.2 Variable Speed Fan

The boxed processor fan will operate at different speeds over a short range of internal chassis temperatures. This allows the processor fan to operate at a lower speed while internal chassis temperatures are low. If internal chassis temperature increases beyond a lower set point, the fan speed will rise linearly with the internal temperature until the upper set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so does fan noise levels. Systems should be designed to provide adequate air around the boxed processor fan heatsink that remains below the lower set point. These set points, represented in Figure 35 and Table 34, can vary by a few degrees from fan heatsink to fan heatsink.

Figure 35. Boxed Processor Fan Heatsink Set Points

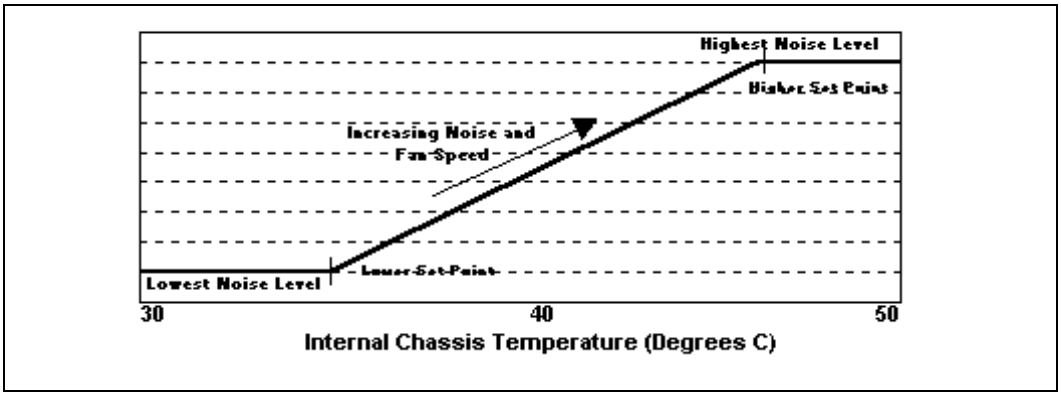


Table 34. Boxed Processor Fan Heatsink Set Points

Boxed Processor Fan Heatsink Set Point (°C)	Boxed Processor Fan Speed
36	When the internal chassis temperature is below this set point the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.
40	When the internal chassis temperature is at this point the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst case operating environment.
45	When the internal chassis temperature is above this set point the fan operates at its highest speed.

NOTES:
1. Set points may vary ±1°C.

The internal chassis temperature should be kept below 40°C. When the internal chassis temperature increases above 45°C, the Thermal Monitor may become active (see Section 7.3). Meeting the processor's temperature specification (see Chapter 6.0) is the responsibility of the system integrator.

9.0 Debug Tools Specifications

This chapter describes the Intel® Pentium® 4 Processor in the 423-pin Package debug port (TAP), In-Target Probe (ITP), and logic analyzer interface (LAI) specifications for Pentium 4 processor system debug.

9.1 Debug Port System Requirements

The Pentium 4 processor debug port (TAP) is the command and control interface for the In-Target Probe (ITP) debugger. The ITP enables run-time control of the Pentium 4 processor for system debug. The debug port, which is connected to the system bus, is a combination of the system, JTAG and execution signals. There are several mechanical, electrical and functional constraints on the debug port which must be followed. The mechanical constraint requires the debug port connector to be installed in the system with adequate physical clearance. The electrical constraint requires the debug port to operate at the speed of the Pentium 4 processor system bus and use the JTAG signals at high speed. The functional constraint requires the debug port to use the JTAG system via a handshake and multiplexing scheme.

In general, the information in this chapter may be used as a basis for including all run-control tools in Pentium 4 processor-based system designs, including tools from vendors other than Intel.

Note: The debug port and JTAG signal chain must be designed into the processor board to utilize the full capabilities of the ITP for debug purposes. A solution is available permitting debug with an ITP/ interposer.

9.1.1 Mechanical Requirements

The ITP Debug Port Adapter (DPA) hardware connects to a Debug Port connector located on the processor board. A 2-meter cable connects the ITP DPA hardware to a half-size PCI card in a host system. In order for the ITP cabling to egress the system under test, an aperture of 2 inches minimum width by 1 inch minimum height must be available. Please contact your run-control tool vendor for complete mechanical constraints for other tools.

An acceptable debug port connector is a Berg #61641-303 which is a 25 pin, through-hole mount header shown in Figure 36. Also available is the Berg #61698-302TR which is a surface-mount version of this connector. The through-hole mount version is recommended for durability reasons. Full specification of the connectors including PCB layout guidelines are available from Berg Electronics through their FAX-back service or from a Berg sales representative. Figure 37 through Figure 39 detail the mechanical volume occupied by the ITP DPA hardware when connected into the debug port connector. All dimensions in the following diagrams are in units of inches.

Note that pin 26 is not used (see Figure 36).

Figure 36. Top View of Debug Port Connector

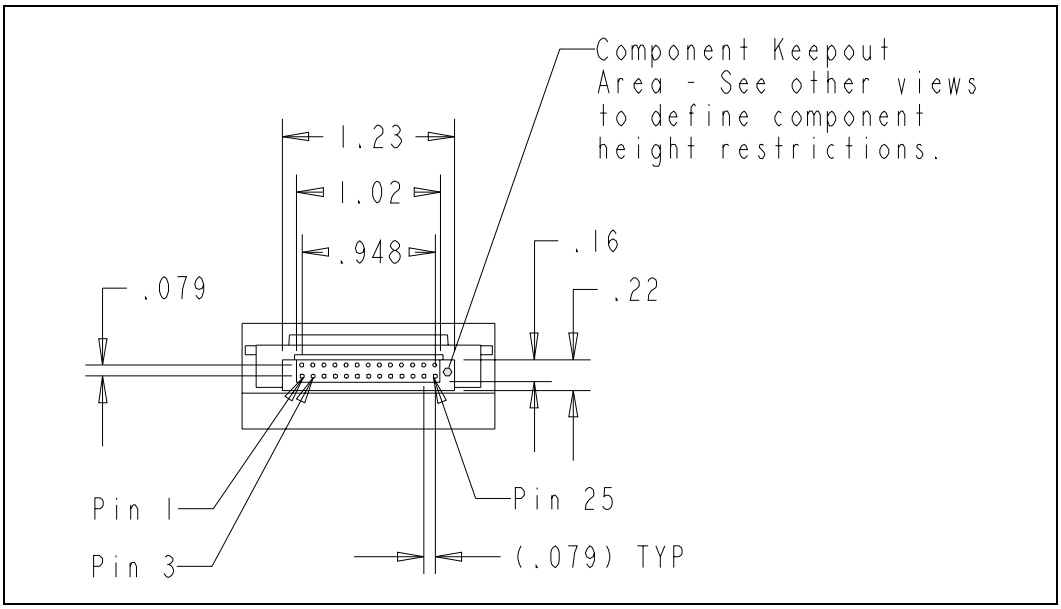


Figure 37. Isometric View of Mechanical Volume Occupied by ITP32 Interface

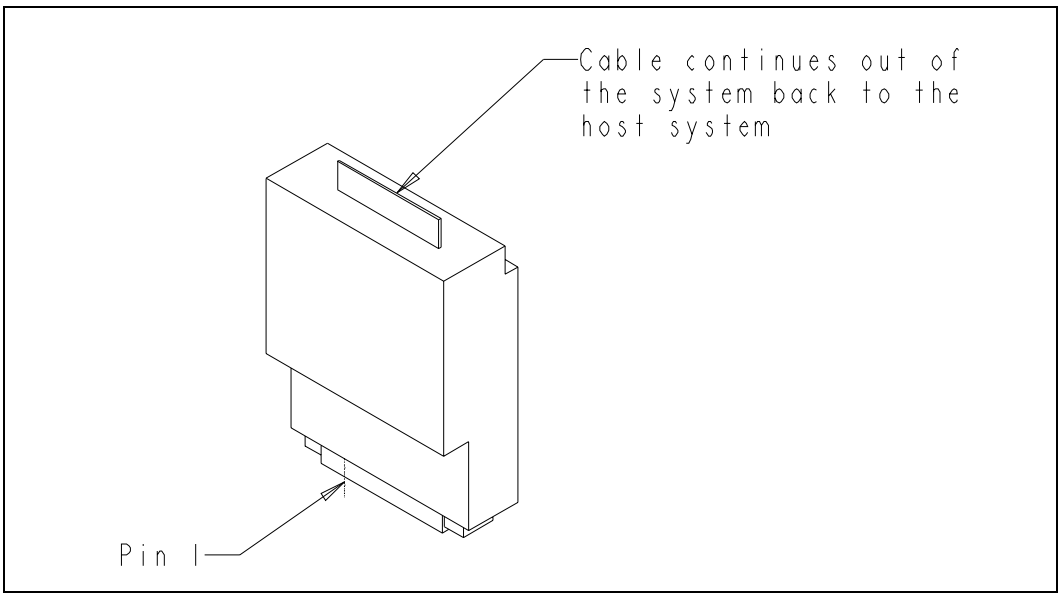


Figure 38. Front View of Mechanical Volume Occupied by ITP32 Interface

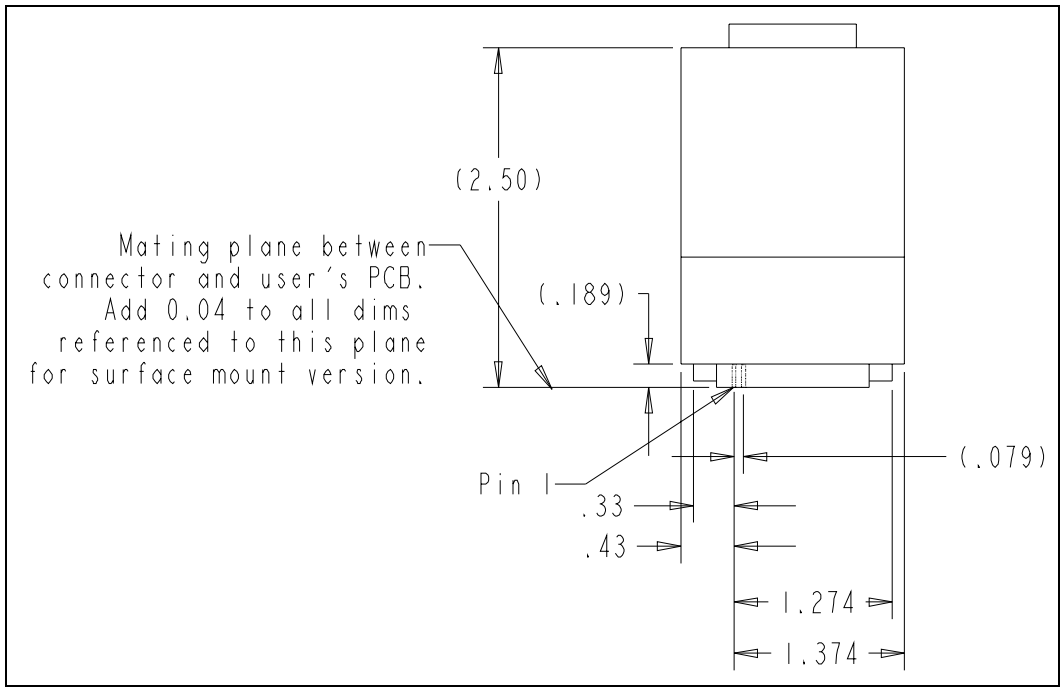
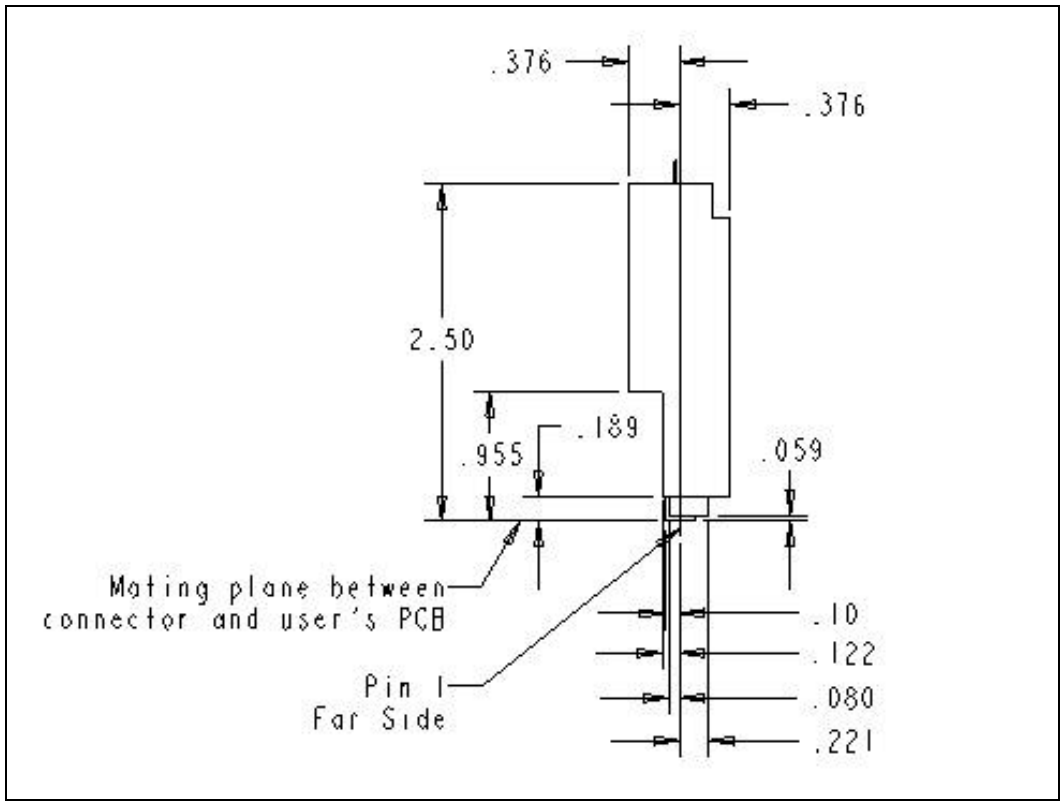


Figure 39. Side View of Mechanical Volume Occupied by ITP32 Interface



9.1.2 Electrical Requirements

The signals used by the ITP are divided into three categories: system, JTAG, and execution. The system signal inputs are PWR and BCLK, and the outputs are DBR# (debugger reset) and DBA# (debugger active). The JTAG signal group consists of the five standard JTAG pins. The signalling levels for the JTAG operations have been changed from the 2.5V CMOS to the processor V_{CC}, similar to GTL+. The execution signal group contains the Pentium 4 processor signal RESET# and the six breakpoint pins BPM[5:0]#. BPM5# and BPM4# are used by the ITP to indicate the break and busy conditions. The lower four BPM[3:0]# signals are monitored and reported in an event status window. These signals are all AGTL+ levels and must be carefully connected to the debug port. The debug port connector pinout is shown in Figure 40.

Note that a simulation model representation is available from Intel. Intel highly recommends that customers include this model in platform simulations.

9.1.2.1 JTAG Signals Electrical Specifications

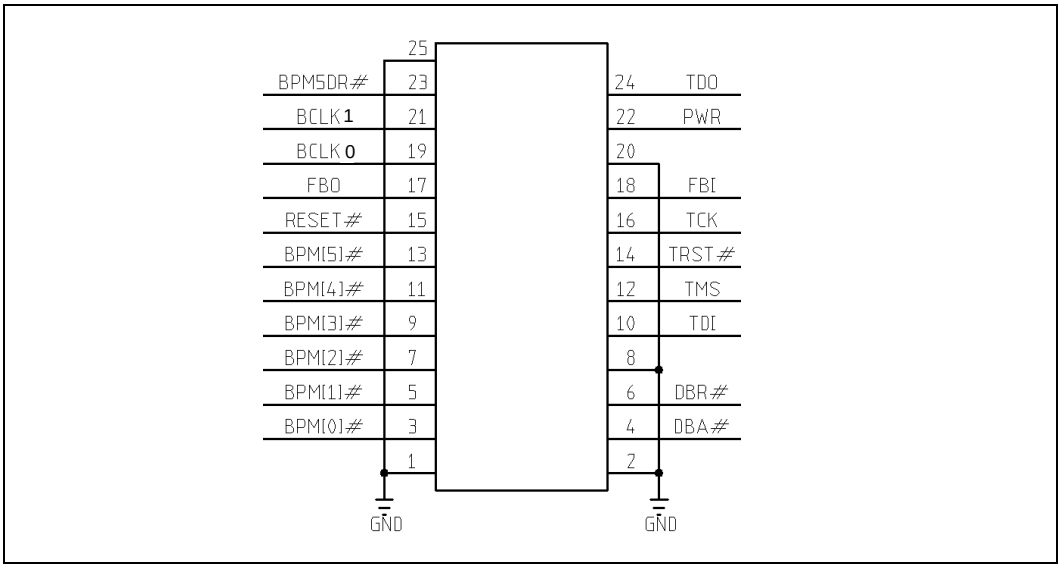
Table 35 lists the DC specifications for the JTAG signals relative to the debug port. Note that relative to the debug port, TCK, TDI, TMS, and TRST# are outputs and TDO is an input. Care should be taken to read all notes associated with each parameter.

Table 35. TAP Signal DC Specifications for the Debug Port

Signal	Symbol	Parameter	Min	Max	Unit	Notes
TDI, TMS, TRST#	V_{OL}	Output Low Voltage		0.525	V	1
TDI, TMS, TRST#	V_{OH}	Output High Voltage	1.30	2.00	V	1
TCK	V_{OL}	Output Low Voltage		0,525	V	1
TCK	V_{OH}	Output High Voltage	1.25		V	1

NOTES:
1. As delivered into termination resistors on the systemboard.

Figure 40. Bottom View of Connector Pinout



9.1.3 Signal Descriptions

The following are complete descriptions of the signals in each signal group and the I/O status with respect to the debug port. Local JTAG refers to a resident JTAG system that has been installed on a system as part of a system designer's manufacturing process. If a local JTAG exists, the PWR and DBA# signals from the ITP are used to arbitrate for the processor cluster scan chain.

9.1.3.1 System Signals Descriptions

Table 36. System Signal Description (I/O Direction for the Debug Port)

Signal	I/O	Description
PWR	Input	PWR is derived from the target system V_{CC}. It is used: first, to generate the 2/3 V_{CC} recovery reference for BPM[5:0]#, RESET#, TDO, and FBO; second to sense the target system interface voltage; and third, with DBA# to arbitrate for the processor cluster scan chain if a local TAP connection exists. If PWR is asserted, the Debug Port will be allowed access to the scan chain, however if PWR is de-asserted (pulled low by an open drain on the target), the JTAG output signals will be tristated.
BCLK[1:0]	Input	Differentially driven low voltage bus clock of target system. Used to sample Execution signals, and to phase align signals driven from the Debug Port. Note BCLK is a detected event. This signal is routing critical.[1]
DBA#	Output	DBA# is the debugger active signal which is output from the ITP to the system JTAG interface. This signal is an open drain output of the Debug Port and must be pulled up on the processor board. This signal can be applied to the system JTAG Mux. There is a switch protocol that can be observed with this signal in conjunction with the PWR and BCLK system outputs.
FBI	Output	FBI is the same signal as TCK without the passive edge rate control. When a buffered copy of TCK is required for routing to the processor or level shifting, use FBI as the source signal. This signal is routing critical.[1]
FBO	Input	FBO is used to register TDO into the ITP tool. FBO is either connected to a tightly matched output of the processor TCK buffer, or connected to TCK at the first processor and routed to the Debug Port to maintain the TCK/BCLK phase relationship to the ITP. The level is compared to 2/3 V_{CC} as delivered to the ITP via the PWR signal on the Debug Port. This signal is routing critical.[1]
DBR#	Output	DBR# is the debugger reset signal which is output from the ITP or run-control tool to the system reset controller. This signal is used to tell the target system to initiate the reset sequence. DBR# is an open drain output of the Debug Port and must be pulled up on the processor board. The signal can be asserted for a configurable period.

NOTE:
1. See the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for routing guidelines.

Table 37. JTAG Signals Descriptions

Signal	I/O	Description
TCK	Output	JTAG master clock. IDLE state must be LOW for target system. Debug Port drives at up to 16MHz if so enabled; in general, it will be substantially slower. Routed to all devices in Processor Cluster. This signal is routing critical.[1] Note: When a buffered copy of TCK is required for routing to the processor or level shifting, use FBI as the source signal.
TDI	Output	TDI transitions are sampled on the rising edge of TCK. JTAG TAP data input signal to the target. This signal must be pulled HI in the target. TDI will require bypass logic for devices that are optionally installed. TDI is driven on TCK's falling edge and should be sampled on TCK's rising edge. This signal is routing critical.[1]
TDO	Input	JTAG TAP data output signal from the target. TDO should be a pull HI to the expected JTAG logic level on the target physically next to and past the Debug Port. The TDO signal passes through the Debug Port en route to the pull up termination. TDO is sampled on the rising edge of FBO (TCK).
TMS	Output	JTAG TAP state management signal. This signal must be pulled HI in target system (generating TCK will eventually lead to Test Logic Reset state in this event). Routed to all devices in Processor Cluster. TMS is driven on TCK's falling edge and should be sampled on TCK's rising edge.
TRST#	Output	TRST# transitions asynchronous to TCK. Test Logic (asynch) Reset. Should be pulled LOW in the target system. The ITP DPA will immediately deassert when active and will thereafter ONLY use TMS to manage target TAP. TRST# is an optional signal to all TAP devices and is not to be counted on.

NOTE:
1. See the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for routing guidelines.

9.1.3.2 Execution Signals Descriptions

The execution signals are sampled on the BCLK rising edge transition. When BCLK is disabled, in-target execution is assumed to be suspended and the execution signals other than RESET# are ignored by the run-control tool.

Table 38. Execution Signals Descriptions (I/O Direction for the Debug Port)

Signal	I/O	Description
BPM5#	Input	BPM5# is an AGTL+ level input break point signal from the Pentium 4 processor system. The level is compared to 2/3 V_{CC}. V_{CC} is delivered to the ITP or run-control tool via the PWR signal on the Debug Port. BPM5# must be connected to BPM5DR# on the processor board at the Debug Port. This signal is routing critical.[1]
BPM[4:0]#	Input	BPM[4:0]# are AGTL+ level input break point signals from the Pentium 4 processor system. The level is compared to 2/3 V_{CC}. V_{CC} is delivered to the ITP via the PWR signal on the debug port. These signals are routing critical.[1]
RESET#	Input	RESET# is a AGTL+ level input reset signal from the Pentium 4 processor system. The level is compared to 2/3 V_{CC} as delivered to the ITP or run-control tool via the PWR signal on the Debug Port. This signal is routing critical.[1]
BPM5DR#	Output	BPM5DR# is the debugger break-at-reset signal. This signal is connected to BPM5# and is driven asynchronously from 50 ns after RESET# assertion until at least 25 ns after de-assertion by the ITP.

NOTE:
1. See the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for routing guidelines.

9.1.4 Signal Termination Requirements

The following table lists signal termination requirements.

Table 39. Execution Signals Descriptions (I/O Direction for the Debug Port)

Signal	Termination Value	Termination Voltage	Notes
System Signals			
PWR	1.5 kΩ	V_{CC}	
BCLK[1:0]			1
FBO	No termination Required		
DBA#	150-240 Ω	V_{CC}	
DBR#	150-240 Ω	V_{CC}	
FBI	220 Ω	GND	2
JTAG Signals			
TCK	27 Ω	GND	
TDI	150 Ω	V_{CC}	
TDO	75 Ω	V_{CC}	
TMS	39 Ω	V_{CC}	
TRST#	680 Ω	GND	
Execution Signals			
BPM5DR#	Connected at Debug Port to BPM[5]#	BPM[5]#	

NOTES:
1. Refer to the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide* for proper BCLK[1:0] and BPM[5:0]# routing and termination guidelines.
2. When FBI is used as an input to a TCK buffer or a bridge, terminate with ~220 ohms to GND.

9.2 Target System Implementation

9.2.1 System Implementation

Specific connectivity and layout guidelines for the Debug Port are provided in the *Intel® Pentium® 4 Processor and Intel® 850 Chipset Platform Design Guide.*

9.3 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Pentium 4 processor systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Pentium 4 processor systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor system that can make use of an LAI: mechanical and electrical.

9.3.1 Mechanical Considerations

The LAI is installed between the processor socket and the Pentium 4 processor. The LAI pins plug into the socket, while the Pentium 4 processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Pentium 4 processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the Pentium 4 processor heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

9.3.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

Numerics

A

B

C

D

E

F

G

T

U

V