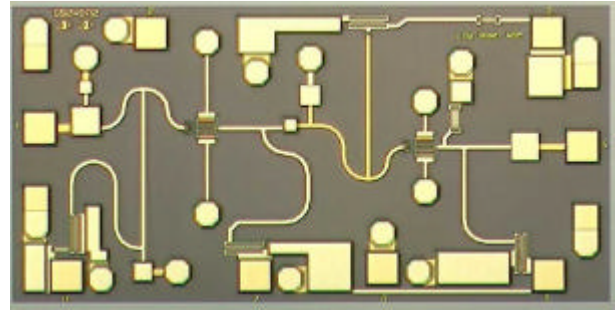


HEMT MMIC LNA

17 - 24GHz

Features

- Typical 2dB Noise Figure @ 24GHz
- Small 1.8 x 0.94mm Die Size



Description

The P35-5115-000-200 is a 17-24GHz Gallium Arsenide low noise amplifier. This product is intended for use in fixed-point and point to point microwave systems.

The die is fabricated using Caswell Technology's 0.20 μ m gate length, pHEMT process and is fully protected using Silicon Nitride passivation for excellent performance and reliability.

Electrical Performance

Ambient Temperature = 22 $\pm$ 3° C, Z_0 = 50 Ω , Vdd = 2V, Vg1 set for Id1 = 13mA, Vg2 set for Id2 = 22mA

Parameter	Conditions	Min	Typ	Max	Units
Small Signal Gain	18-24GHz	-	18	-	dB
Input Return Loss	18-24GHz	-	12	-	dB
Output Return Loss	18-24GHz	-	15	-	dB
Noise Figure	18-24GHz	-	2.1	-	dB
P1dB	18-24GHz	-	5	-	dBm
Drain current, Id1		-	13	-	mA
Drain current, Id2		-	22	-	mA
Supply Voltage; Vdd		-	2	-	V
Gate Voltage; Vg1		-	-0.6	-	V
Gate Voltage; Vg2		-	-0.4	-	V

Notes

1. All parameters measured on wafer

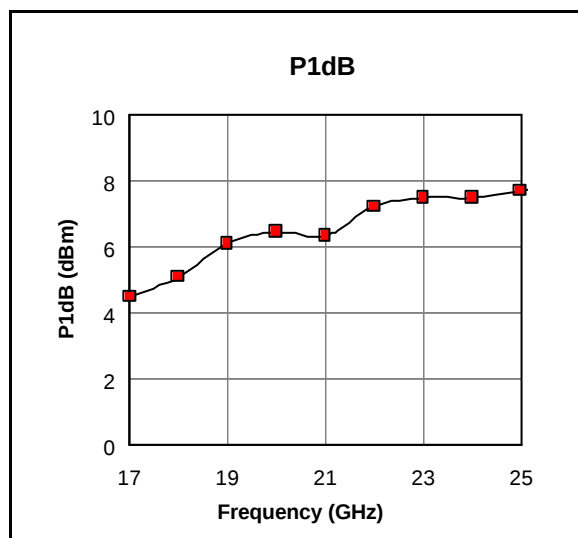
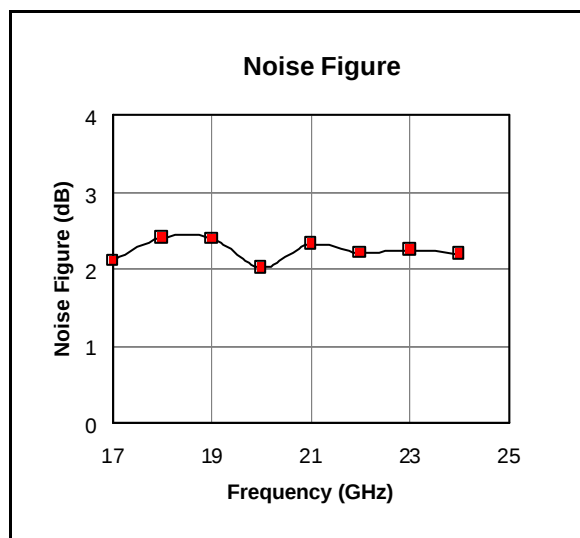
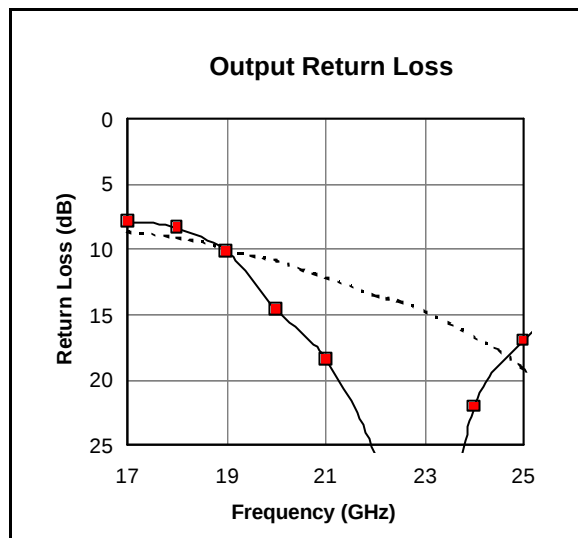
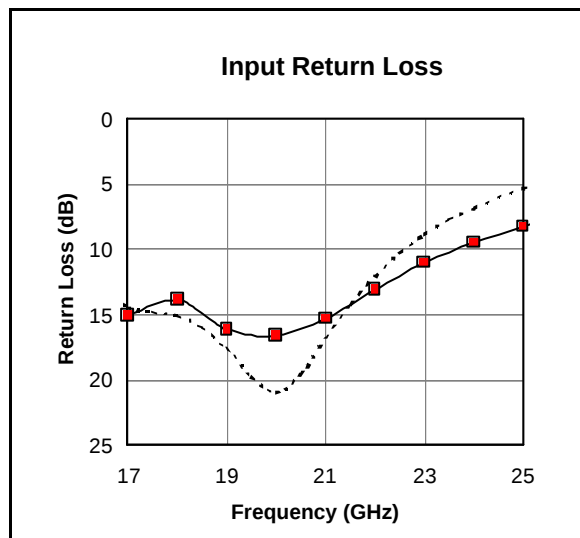
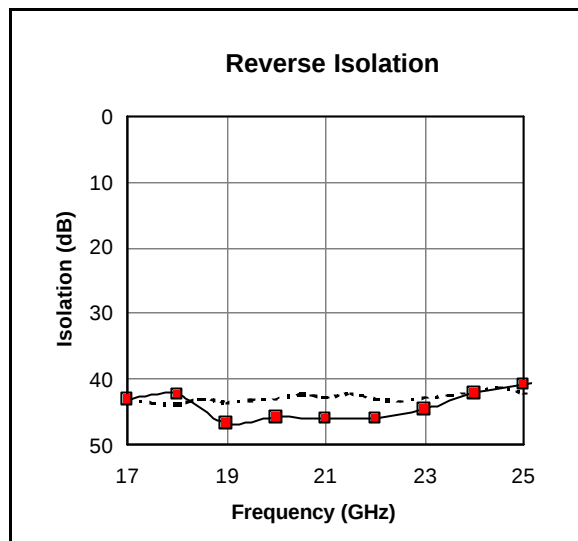
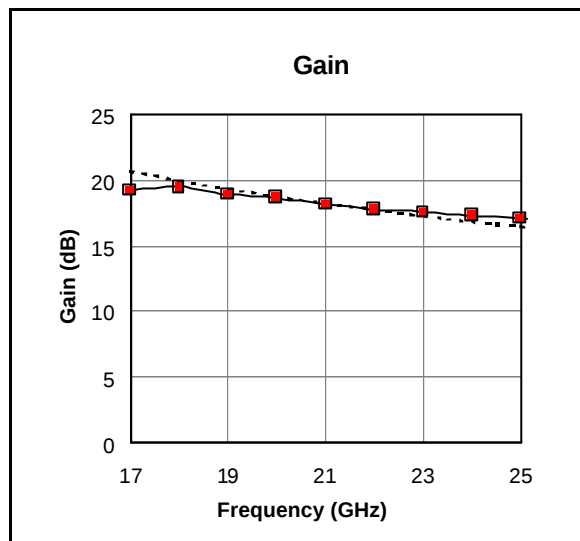
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Typical RFOW Performance (----- Measured in Jig)



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Typical S-parameters (RFOW)

Frequency (GHz)	S11		S21		S12		S22	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
18	0.24	-8.1	8.40	-80.4	0.0066	-178.9	0.37	-149.4
18.2	0.27	-15.9	7.70	-86.2	0.0082	174.8	0.38	-151.3
18.4	0.29	-33.8	7.25	-83.1	0.0068	162.3	0.39	-159.9
18.6	0.24	-48.3	8.20	-84.4	0.0066	158.4	0.35	-161.8
18.8	0.20	-53.8	8.81	-91.5	0.0052	147.6	0.34	-166.5
19	0.18	-57.2	9.10	-98.8	0.0043	144.7	0.32	-172.3
19.2	0.17	-58.8	9.18	-106.3	0.005	146.8	0.29	-176.6
19.4	0.17	-62.8	9.18	-112.8	0.0047	153.3	0.27	179.1
19.6	0.16	-68.2	9.20	-119.3	0.0045	148.4	0.24	173.8
19.8	0.16	-73.4	9.11	-125.8	0.0048	151.8	0.20	172
20	0.17	-79.4	8.96	-131.8	0.0048	149.9	0.18	175.5
20.2	0.17	-87.1	8.87	-137.2	0.0058	139.2	0.18	174.5
20.4	0.17	-94.6	8.82	-142.6	0.0061	130.4	0.16	171.4
20.6	0.17	-102.4	8.72	-148.1	0.0058	130.7	0.15	167.5
20.8	0.17	-109.2	8.63	-153.4	0.0059	120.1	0.13	164.8
21	0.18	-115.7	8.53	-158.6	0.0059	118.6	0.11	162.1
21.2	0.18	-122.7	8.41	-163.6	0.0051	106.1	0.10	161.9
21.4	0.19	-128.3	8.31	-168.1	0.006	109.2	0.09	160.9
21.6	0.20	-134.9	8.28	-172.6	0.0064	111.1	0.08	155
21.8	0.21	-140.7	8.27	-177.5	0.0075	97.5	0.07	147
22	0.22	-147	8.20	177.6	0.0065	93.5	0.05	140.3
22.2	0.23	-152.8	8.16	172.8	0.0057	98.3	0.04	129.9
22.4	0.24	-158.8	8.10	168	0.0067	87.9	0.03	113.5
22.6	0.25	-164.1	8.07	163.4	0.0072	85.7	0.03	86
22.8	0.27	-169.1	8.02	158.7	0.0064	83.2	0.02	46.2
23	0.28	-174.8	7.97	153.9	0.0072	79	0.03	16.6
23.2	0.29	-179.5	7.89	149.4	0.007	76.6	0.04	3.5
23.4	0.30	176.5	7.85	144.9	0.0067	74.1	0.05	-6.1
23.6	0.31	172.1	7.83	140.6	0.0073	71.1	0.05	-10.2
23.8	0.33	167.7	7.84	136.3	0.0079	74.6	0.07	-11.9
24	0.35	162	7.83	131.2	0.0082	60.6	0.08	-16.5
24.2	0.36	156.7	7.78	126.4	0.0081	56.4	0.10	-21.4
24.4	0.37	152.1	7.73	121.7	0.009	51.2	0.11	-26.7
24.6	0.38	147.8	7.65	117.2	0.0092	51.3	0.12	-31.3
24.8	0.39	143.6	7.61	112.9	0.0087	40.6	0.13	-34.2
25	0.40	139.6	7.58	108.2	0.0092	40.6	0.14	-36.5
25.2	0.41	135.5	7.53	103.7	0.0096	36.4	0.15	-40.1
25.4	0.42	131.6	7.51	99.2	0.0089	30	0.16	-42.4
25.6	0.43	127.7	7.49	94.7	0.0101	25.9	0.17	-44.2
25.8	0.44	123.6	7.47	89.7	0.0102	24.8	0.19	-47.2
26	0.45	119.4	7.42	84.8	0.011	19.4	0.21	-50.5

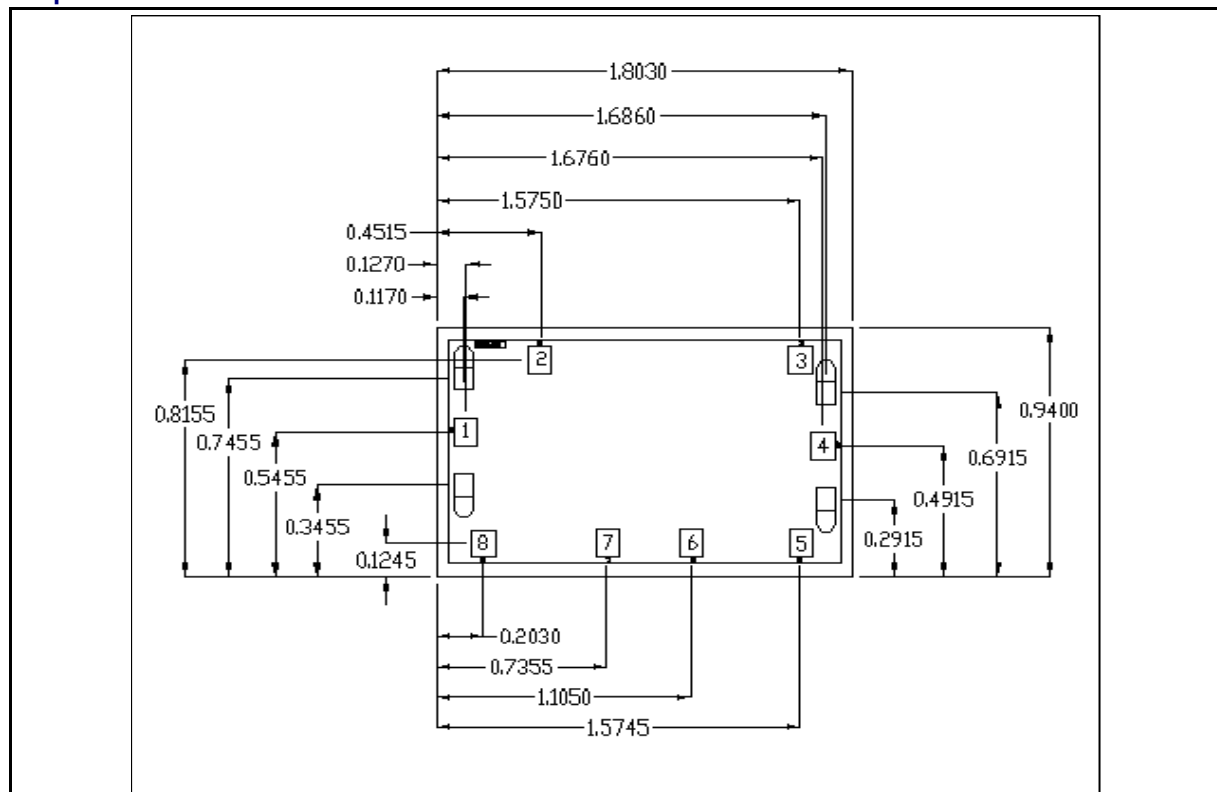
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Chip Outline



Die size: 1.80 x 0.94mm
 RF bond pads (1 & 4): 120μm x 120μm
 All other bond pads: 120μm x 120μm
 Die Thickness: 100μm

Pad Details

Pad	Function
1	RF Input
2	N/C
3	Vg2
4	RF Output
5	Vdd
6	N/C
7	N/C
8	Vg1

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Handling and Assembly Information

Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Dice are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

GaAs Products from Caswell Technology's pHEMT Foundry process are 100µm thick and have through GaAs vias to enable grounding to the circuit. Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die.

The surface to which the die are to be attached should be cleaned with a proprietary de-greasing cleaner.

Conductive epoxy mounting is recommended. Recommended epoxies are Ablestick 84-1LMI or 84-1LMIT cured at 150°C for 1 hour in a nitrogen atmosphere. The epoxy should be applied sparingly to avoid encroachment of the epoxy on to the top surface of the die. An epoxy fillet should be visible around the total die periphery.

Eutectic mounting can be used and entails the use of a gold-tin (AuSn) preform, approximately 0.001" thick, placed between the die and the attachment surface. The preferred method of mounting is the use of a machine such as a Mullins 8-140 die bonder. This utilises a heated collet and workstation with a facility for applying a scrubbing action to ensure total wetting and avoid the formation of voids. Dry nitrogen gas is directed across the work piece.

The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280°C (Note: Gold Germanium with a higher melting temperature should be avoided, in particular for MMICs). The work station temperature should be 310°C ± 10°C. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. The strength of the bonding formed by this method will result in fracture of the die, rather than the bond under die strength testing.

The P35-5115-000-200 amplifier die has gold bond pads. The recommended wire bonding procedure uses 25µm (0.001") 99.99% pure gold wire with 0.5-2% elongation. Thermo-compression wedge bonding is preferred though thermosonic wire bonding may be used providing the ultrasonic content of the bond is minimised. A work station temperature of 260°C ± 10°C with a wedge tip temperature of 120°C ± 10°C is recommended. The wedge force should be 45 ± 5 grams. Bonds should be made from the bond pads on the die to the package or substrate.

The RF bond pads at the input and output are 120µm x 120µm; all other bond pads are 120µm x 120µm.

The P35-5115-000-200 has been designed to include the inductance of two 25µm bond wires at both the input and output, facilitating the integration of the die into a 50Ω environment, these should be kept to a minimum length.

Operating and Biasing of the P35-5115-000-200

The P35-5115-000-200 is a two-stage low noise amplifier. The drain biases for both stages (Vd1 & Vd2) are ganged together (Vdd) and should be set to 2 volts. The gate voltages (Vg1 & Vg2) are typically set to give 13mA of drain current in the first stage and 22mA in the second stage. To bias the device, 2V should be applied to Vdd and with Vg2 set to -1.5V, Vg1 is adjusted to give a drain current of 13mA (approx -0.6V); then set Vg1 to -1.5V and adjust Vg2 to give 22mA drain current (Approx -0.4V); apply the two gate voltages to the corresponding gate to give a total drain current of around 35mA. DC bias supplies should be decoupled to ground using 100pF chip capacitors placed close to the chip with short bondwires to the amplifier bond pads.

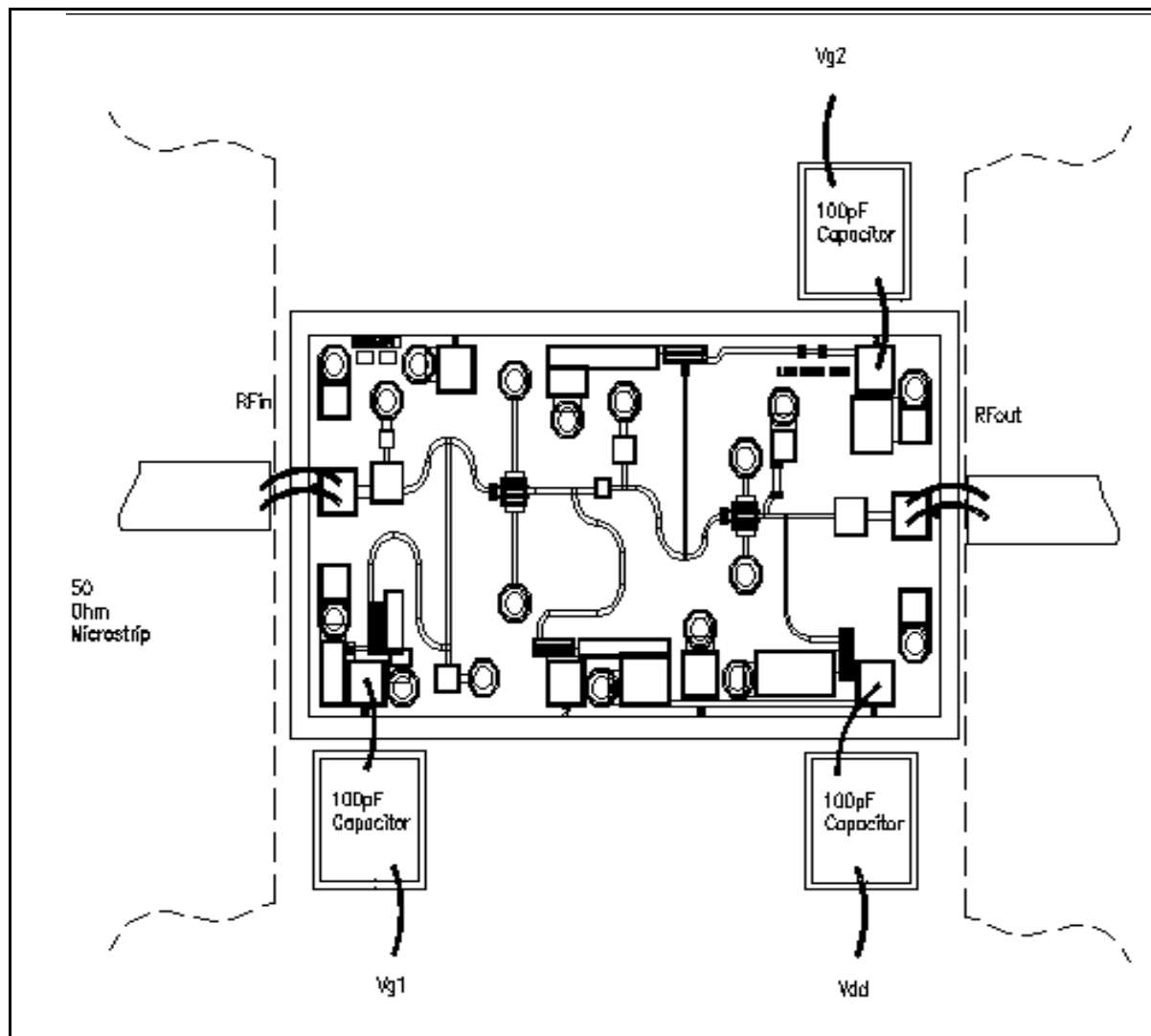
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Typical bonding detail



Absolute maximum Ratings

Max V _{dd}	+5V
Max V _{gg}	-2V
Max channel temperature	150°C
Storage temperature	-65°C to +150°C

Ordering Information

P35-5115-000-200

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