3.3V 64K x 32 Fast CMOS Synchronous Static RAM with Burst Counter

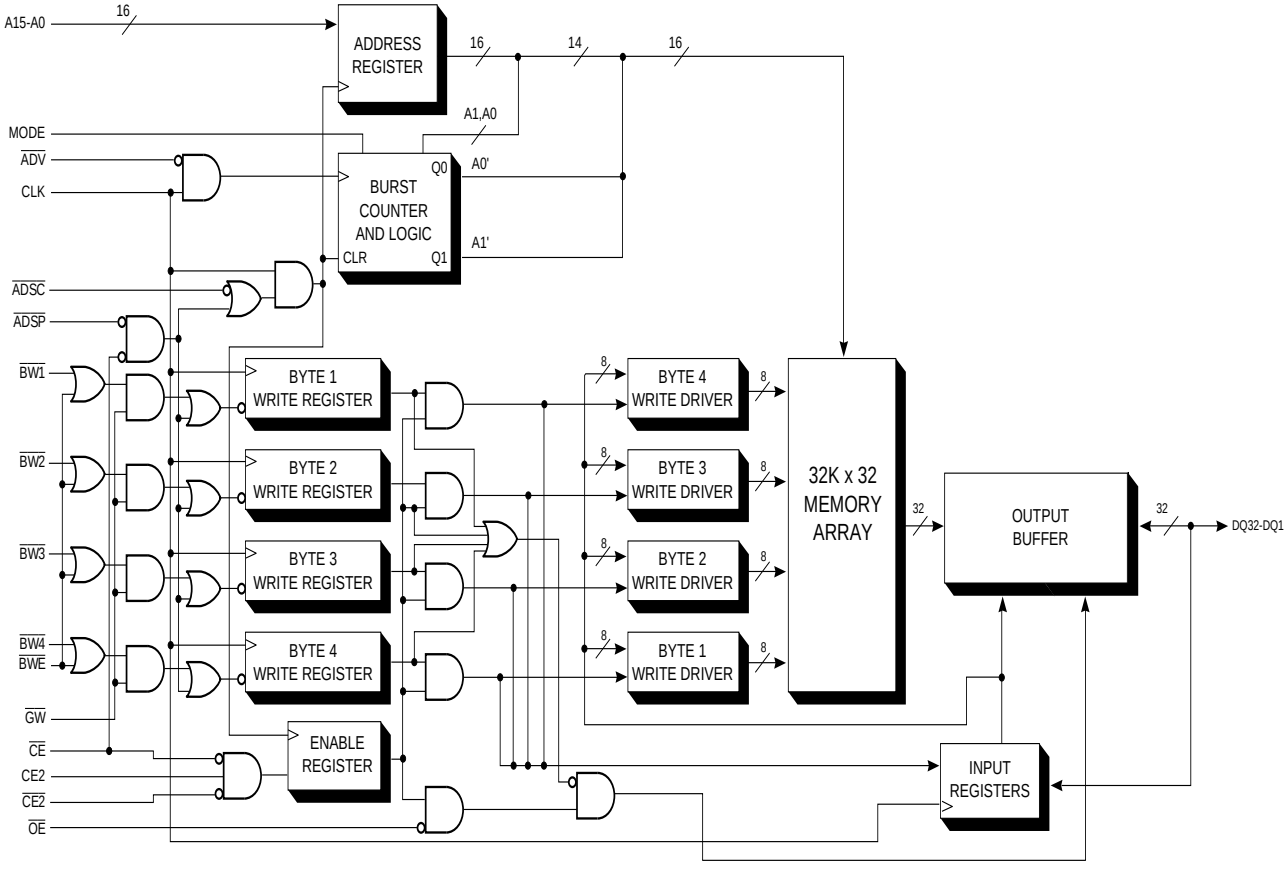
Features

- ☐ Interfaces directly with the x86, Pentium™, 680X0 and PowerPC™ processors
- ☐ Single 3.3V power supply
- ☐ Mode selectable for interleaved or linear burst:
  Interleaved for x86 and Pentium
  Linear for 680x0 and PowerPC
- ☐ Fast access times:
  9, 10, 12 and 15 ns
- ☐ High-density 64K x 32 architecture with burst address counter
- ☐ Fully registered inputs
- ☐ High-output drive: 30 pF at rated T_A
- ☐ Asynchronous output enable
- ☐ Self-timed write cycle
- ☐ Separate byte write enables and one global write enable
- ☐ Internal burst read/write address counter
- ☐ Internal registers for address, data, controls
- ☐ Burst mode selectable
- ☐ Sleep mode
- ☐ Packages:
  100-pin QFP - (Q)
  100-pin TQFP - (TQ)

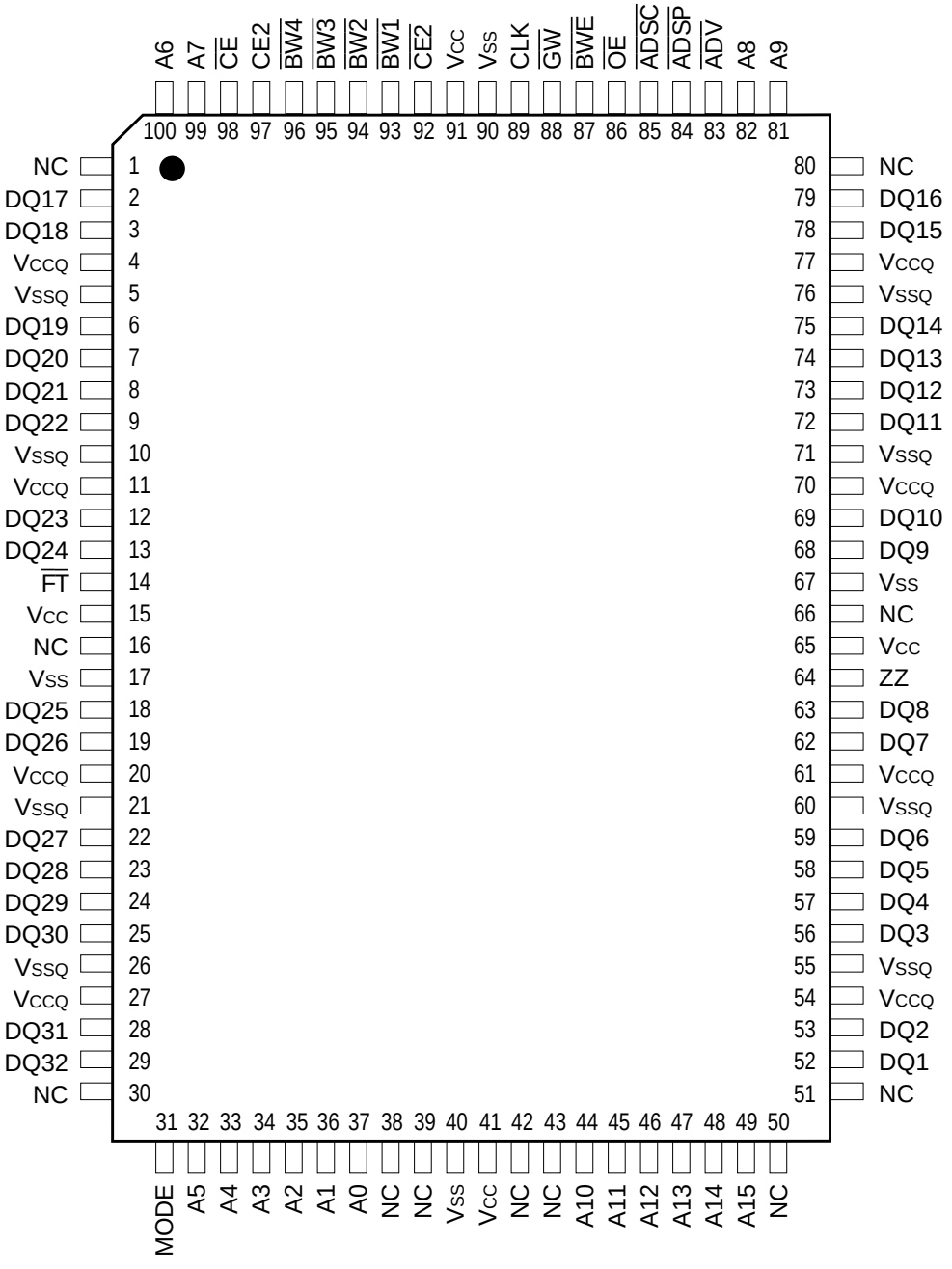
Description

The PDM34089 is a 2,097,152 bit synchronous random access memory organized as 65,536 x 32 bits. It is designed with burst mode capability and interface controls to provide high-performance in second level cache designs for x86, Pentium, 680x0, and PowerPC microprocessors. Addresses, write data and all control signals except output enable are controlled through positive edge-triggered registers. Write cycles are self-timed and are also initiated by the rising edge of the clock. Controls are provided to allow burst reads and writes of up to four words in length. A 2-bit burst address counter controls the two least-significant bits of the address during burst reads and writes. The burst address counter selectively uses the 2-bit counting scheme required by the x86 and Pentium or 680x0 and PowerPC microprocessors as controlled by the mode pin. Individual write strobes provide byte write for the four 8-bit bytes of data. An asynchronous output enable simplifies interface to high-speed buses.

Functional Block Diagram



PDM34089 Pinout



Pinout

Name	I/O	Description	Name	I/O	Description
A14-A2	I	Address Inputs A14-A2	$\overline{CE}$, CE2, $\overline{CE2}$	I	Chip Enables
A1, A0	I	Address Inputs A1 & A0	$\overline{BWE}$	I	Byte Write Enable
DQ1-DQ32	I/O	Read/Write Data	$\overline{BW1}$-$\overline{BW4}$	I	Byte Write Enables
NC	—	No Connect	$\overline{OE}$	I	Output Enable
MODE(1)	I	Burst Sequence Select	CLK	I	Clock
$\overline{ADV}$	I	Burst Counter Advance	ZZ	I	Sleep Mode
$\overline{ADSC}$	I	Controller Address Status	V_{CC}	—	Power Supply (+3.3V)
$\overline{ADSP}$	I	Processor Address Status	V_{CCQ}	—	Output Power for DQ's (+3.3V ±5%)
$\overline{GW}$	I	Global Write	V_{SS}	—	Array Ground
$\overline{FT}$(1)	I	Must be tied LOW for proper operation	V_{SSQ}	—	Output Ground for DQ's

Note: 1.MODE and $\overline{FT}$ are DC operated pins. Do not alter input state while device is operating.

Burst Sequence Table

Burst Sequence	Interleaved(1) Mode = NC or V_{CC}	Linear(2) Mode = V_{SS}			
External Address	A15-A2, A1, A0	A15-A2,0,0	A15-A2,0,1	A15-A2,1,0	A15-A2,1,1
1st Burst Address	A15-A2, A1, $\overline{A0}$	A15-A2,0,1	A15-A2,1,0	A15-A2,1,1	A15-A2,0,0
2nd Burst Address	A15-A2, $\overline{A1}$, A0	A15-A2,1,0	A15-A2,1,1	A15-A2,0,0	A15-A2,0,1
3rd Burst Address	A15-A2, $\overline{A1}$, $\overline{A0}$	A15-A2,1,1	A15-A2,0,0	A15-A2,0,1	A15-A2,1,0

Note: 1. Interleaved = x86 and Pentium.
2. Linear = 680x0 and PowerPC compatible.

Asynchronous Truth Table

Operation	ZZ	$\overline{OE}$	I/O Status
Read	L	L	Data Out
Read	L	H	High-Z
Write	L	X	High-Z: Write Data In
Deselected	L	X	High-Z
Sleep	H	X	High-Z

NOTE: 1. L = Low, H = High, X = Don't Care.
2. For a write operation following a read operation, $\overline{OE}$ must be high before the input data required setup time and held high through the input data hold time.
3. This device contains circuitry that will ensure the outputs will be in high-Z during powerup.

Partial Truth Table for Writes

$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$	Function
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE Byte 1
H	L	L	L	L	L	WRITE All Bytes
L	X	X	X	X	X	WRITE All Bytes

NOTE: 1. L = Low, H = High, X = Don't Care.
2. Using $\overline{BWE}$ and $\overline{BW1}$ through $\overline{BW4}$, any one or more bytes may be written.

Synchronous Truth Table (See Notes 1 through 3)

$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{BWx}$	CLK	Address	Operation
H	X	X	X	L	X	X	↑	N/A	Deselected
L	X	L	L	X	X	X	↑	N/A	Deselected
L	H	X	L	X	X	X	↑	N/A	Deselected
L	X	L	H	L	X	X	↑	N/A	Deselected
L	H	X	H	L	X	X	↑	N/A	Deselected
L	L	H	L	X	X	X	↑	External	Read Cycle, Begin Burst
L	L	H	H	L	X	X	↑	External	Read Cycle, Begin Burst
X	X	X	H	H	L	H	↑	Next	Read Cycle, Continue Burst
H	X	X	X	H	L	H	↑	Next	Read Cycle, Continue Burst
X	X	X	H	H	H	H	↑	Current	Read Cycle, Suspend Burst
H	X	X	X	H	H	H	↑	Current	Read Cycle, Suspend Burst
L	L	H	H	L	X	L	↑	External	Write Cycle, Begin Burst
X	X	X	H	H	L	L	↑	Next	Write Cycle, Continue Burst
H	X	X	X	H	L	L	↑	Next	Write Cycle, Continue Burst
X	X	X	H	H	H	L	↑	Current	Write Cycle, Suspend Burst
H	X	X	H	H	H	L	↑	Current	Write Cycle, Suspend Burst

NOTES:
1. X = Don't Care, H = logic High, L = logic Low, $\overline{BWx}$ = any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and $\overline{BWE}$ are low, or $\overline{GW}$ is low.
2. $\overline{BW1}$ enables $\overline{BWx}$ to Byte 1 (DQ1-DQ8). $\overline{BW2}$ enables $\overline{BWx}$ to Byte 2 (DQ9-DQ16). $\overline{BW3}$ enables $\overline{BWx}$ to Byte 3 (DQ17-DQ24), $\overline{BW4}$ enables $\overline{BWx}$ to Byte 4 (DQ25-DQ32).
3. $\overline{ADV}$ must always be high at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a write cycle is desired (to ensure use of correct address).

Burst Mode Operation

This is a synchronous part. All activities are initiated by the positive, low-to-high edge of the clock (CLK). This part can perform burst reads and writes with burst lengths of up to four words. The four-word burst is created by using a burst counter to drive the two least-significant bits of the internal RAM address. The burst counter is loaded at the start of the burst and is incremented for each word of the burst. The sequence is given in the Burst Sequence Table.

Burst transfers are initiated by the $\overline{ADSC}$ or $\overline{ADSP}$ signals. When the $\overline{ADSP}$ and $\overline{CE}$ signals are sampled low, a read cycle is started (independent of $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$; $\overline{BWE}$, $\overline{GW}$ and $\overline{ADSC}$), and prior burst activity is terminated. $\overline{ADSP}$ is gated by $\overline{CE}$, so both must be active for $\overline{ADSP}$ to load the address register and to initiate a read cycle. The address and the chip enable input ($\overline{CE}$) are sampled by the same edge that samples $\overline{ADSP}$. Read data is valid at the output after the specified delay from the clock edge.

When $\overline{ADSC}$ is sampled low and $\overline{ADSP}$ is sampled high, a read or write cycle is started depending on the state of $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$; $\overline{BWE}$, and $\overline{GW}$. If $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, and $\overline{GW}$ are all sampled high, a read cycle is started, as described above. If $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, or $\overline{BW4}$; $\overline{BWE}$, and $\overline{GW}$ is sampled low, a write cycle is begun. The address, write data, and the chip enable inputs ($\overline{CE}$, CE2 and $\overline{CE2}$) are sampled by the same edge that samples $\overline{ADSC}$ and $\overline{BW1}$–$\overline{BW4}$, $\overline{BWE}$ and $\overline{GW}$. The $\overline{ADV}$ line is held high for this clock edge to maintain the correct address for the internal write operation which will follow this second clock edge.

After the first cycle of the write burst, the state of $\overline{BW1}$-$\overline{BW4}$, $\overline{BWE}$ and $\overline{GW}$ determines whether the next cycle is a read or write cycle, and $\overline{ADV}$ controls the advance of the address counter. The $\overline{ADV}$ signal advances the address counter. This increments the address to the next available RAM address. You write the next word in the burst by taking $\overline{ADV}$ low and presenting the write data at the positive edge of the clock. If $\overline{ADV}$ is sampled low, the burst counter advances and the write data (which is sampled by the same clock) is written into the internal RAM during the time following the clock edge.

Absolute Maximum Ratings

Symbol	Rating	Com'l.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	100	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.1	3.3	3.6	V
V_{CCQ}	Supply voltage	3.1	3.3	3.6	V
V_{SS}	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V, All Temperature Ranges)

Symbol	Description	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{IN} = 0V to V_{CC}	–2	2	µA
$\|I_{LO}\|$	Output Leakage Current	Outputs Disabled, $V_{I/O}$ = 0V to V_{CC}	–2	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8 mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –5 mA	2.4	—	V
V_{IH}	Input HIGH Voltage		2.0	3.6	V
V_{IL}	Input LOW Voltage(1)		–0.3	0.8	V

NOTES: 1. Undershoots to –2.0 for 10 ns are allowed once per cycle.
2. MODE, $\overline{FT}$ and ZZ pins have an internal pullup and exhibit an input leakage current of ±400 µA.

Power Supply Characteristics

Symbol	Description	Test Conditions	-7 ns	-10 ns	-12 ns	-15 ns	Unit
I_{CC}	Active Supply Current	Device Deselected $V_{IN} \le V_{IL}$ or $\ge V_{IH}$, $I_{I/O}$ = 0	315	230	210	190	mA
I_{SB}	Standby Current:	Device Deselected $V_{IN} \le V_{IL}$ or $\ge V_{IH}$, 0 MHz All inputs static	25	20	20	20	mA
I_{SB1}	Standby Current:	Device Deselected $V_{IN} \le 0.2V$ or $\ge V_{CC} - 0.2V$ All inputs static, 0 MHz	5	3	3	3	mA
I_{SB2}	Standby Current:	Device Deselected $V_{IN} \le V_{IL}$ or $\ge V_{IH}$, All inputs static	55	45	40	35	mA
I_{SB3}	Sleep Mode Standby Current:	Device Deselected $ZZ \ge V_{CCQ} - 0.2V$	5	3	3	3	mA

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTES: 1. Characterized values, not currently tested.

AC Test Conditions

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	1.5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

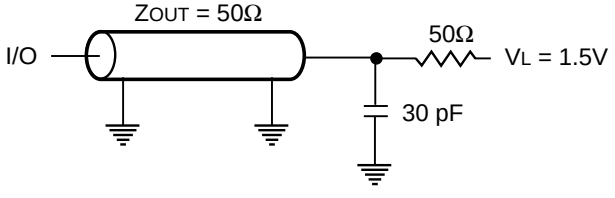


Figure 1. Output Load

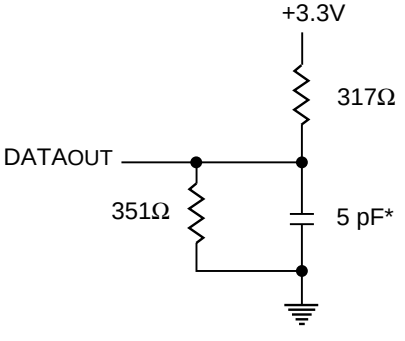


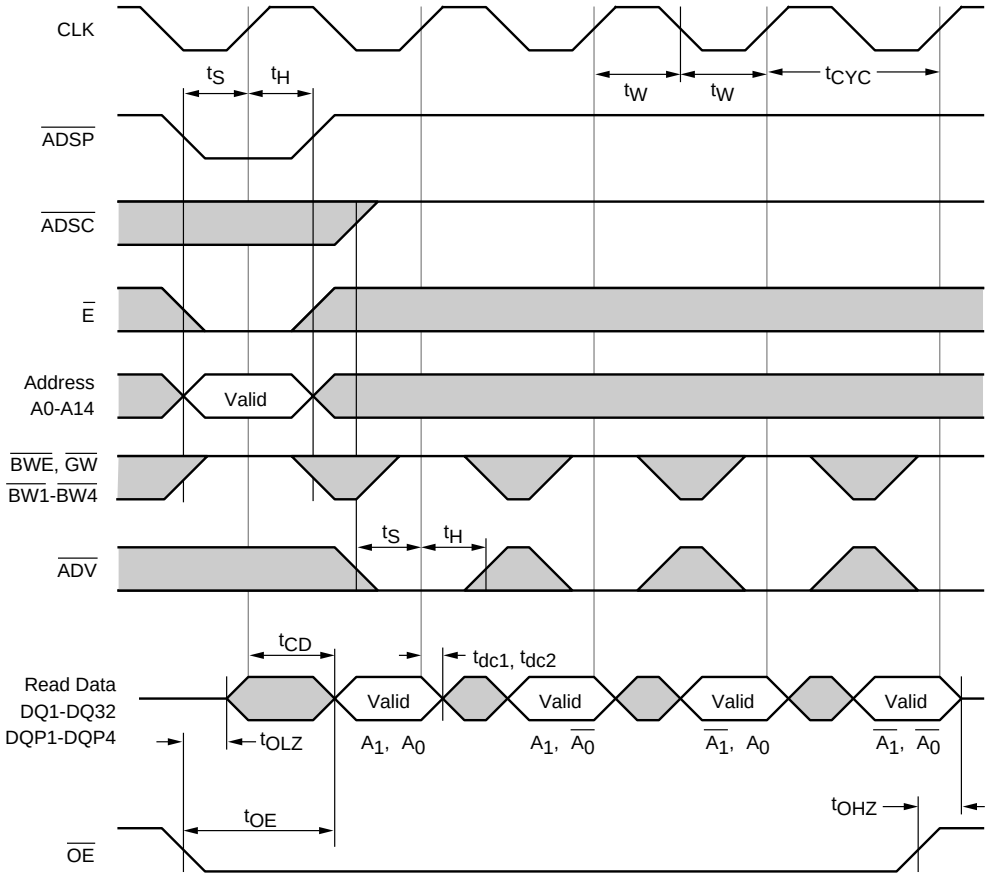
Figure 2. Output Load

t_{CQ}, t_{OLZ}, t_{OHZ}, t_{CZ}

AC Electrical Characteristics

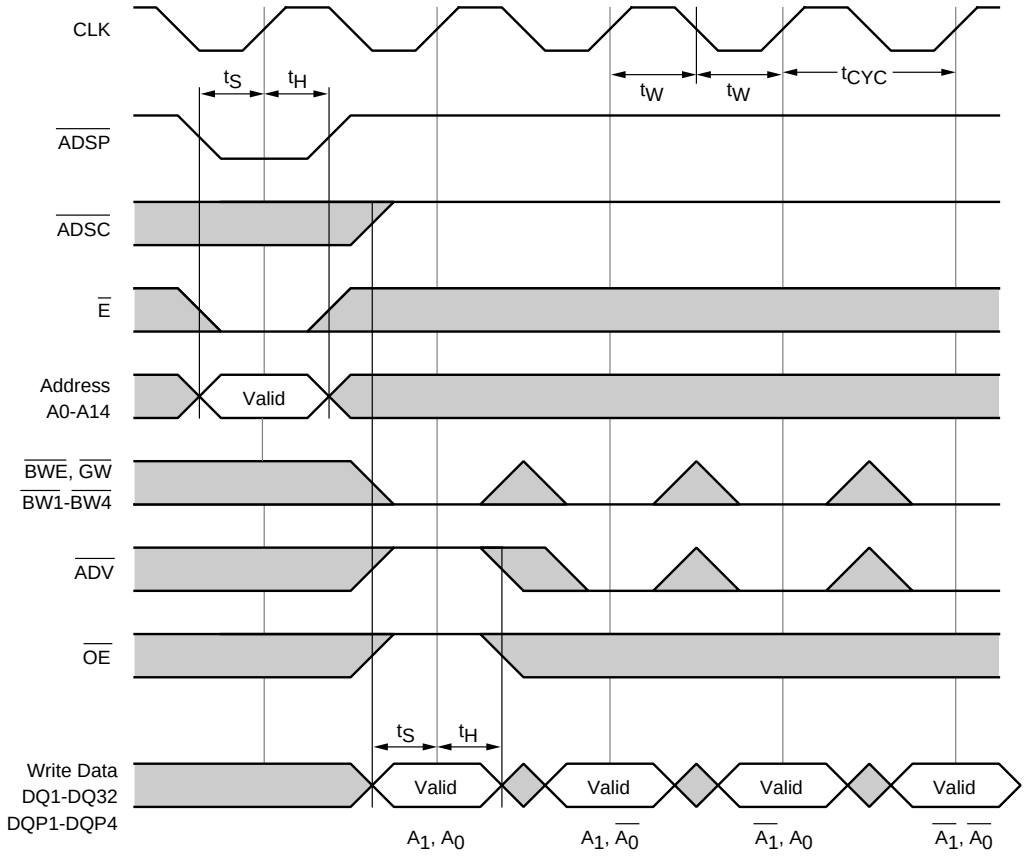
Parameter	Symbol	-7 ns	-10 ns	-12 ns	-15 ns	Type	Units
Cycle time	t_{CYC}	12	16.7	20	25	Min.	ns
Clock access time (0 pF load)	t_{CQ0}	8.5	9	11	13	Max.	ns
Clock to output valid (Std. load)	t_{CQ}	9	10	12	14	Max.	ns
Clock to output invalid	t_{CQX}	3	2	2	2	Min.	ns
Clock to output high-Z	t_{CHZ}	5	2	2	2	Min.	ns
		12	16.7	20	25	Max.	
Clock pulse width high	t_{CH}	4.5	6	6	6	Min.	ns
Clock pulse width low	t_{CL}	4.5	6	6	6	Min.	ns
$\overline{OE}$ to output valid	t_{OE}	5	6	6	6	Min.	ns
$\overline{OE}$ to output low-Z	t_{OLZ}	0	0	0	0	Min.	ns
$\overline{OE}$ to output high-Z	t_{OHZ}	5	6	6	6	Max.	ns
ZZ standby time	t_{ZZS}	100	100	100	100	Max.	ns
ZZ recovery time	t_{ZZREC}	100	100	100	100	Min.	ns
SETUP TIMES							
Address	t_{AS}	2.5	2.5	3	3	Min.	ns
Address status ($\overline{ADSC}$, $\overline{ADSP}$)	t_{AAS}	2.5	2.5	3	3	Min.	ns
Address advance setup ($\overline{ADV}$)	t_{AAS}	2.5	2.5	3	3	Min.	ns
Write signals ($\overline{BWx}$, $\overline{GW}$)	t_{WS}	2.5	2.5	3	3	Min.	ns
Data in	t_{DS}	2.5	2.5	3	3	Min.	ns
Chip enables ($\overline{CE}$, $\overline{CE2}$, CE2)	t_{CES}	2.5	2.5	3	3	Min.	ns
HOLD TIMES							
Address	t_{AH}	0.5	0.5	0.5	0.5	Min.	ns
Address status ($\overline{ADSC}$, $\overline{DSP}$)	t_{ADSH}	0.5	0.5	0.5	0.5	Min.	ns
Address advance ($\overline{ADV}$)	t_{AAH}	0.5	0.5	0.5	0.5	Min.	ns
Write eignals ($\overline{BWx}$, $\overline{GW}$)	t_{WH}	0.5	0.5	0.5	0.5	Min.	ns
Data in	t_{DH}	0.5	0.5	0.5	0.5	Min.	ns
Chip enables ($\overline{CE}$, $\overline{CE2}$, CE2)	t_{CEH}	0.5	0.5	0.5	0.5	Min.	ns

$\overline{\text{ADSP}}$ Read Timing Diagram



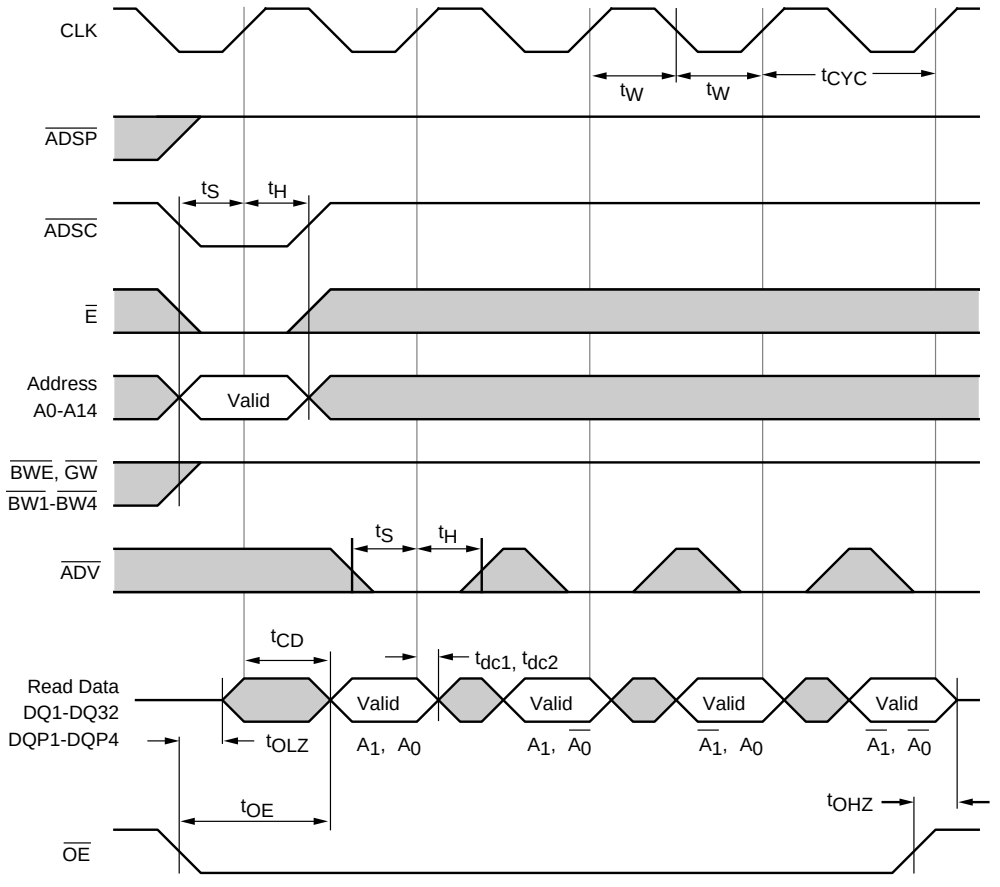
NOTE:
1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.

$\overline{\text{ADSP}}$ Write Timing Diagram



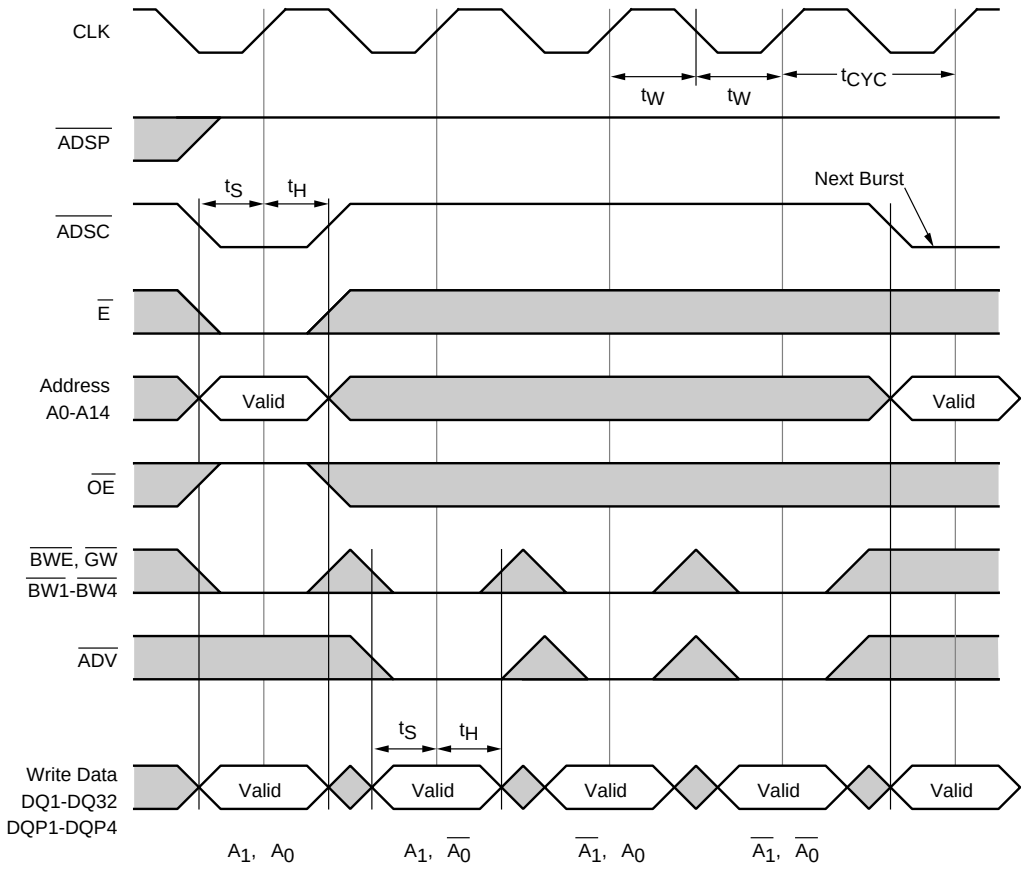
NOTES:
1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.
2. $\overline{BWx}$ and $\overline{GW}$ are ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new address into the address-counter and forces the first cycle to be a read cycle.
3. $\overline{OE}$ is high before data input setup.

ADSC Read Timing Diagram



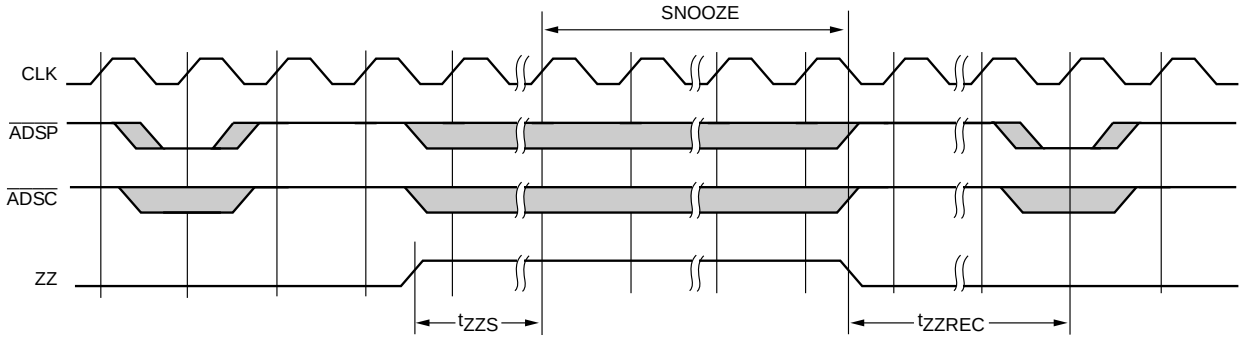
NOTES: 1.
1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.

ADSP Write Timing Diagram



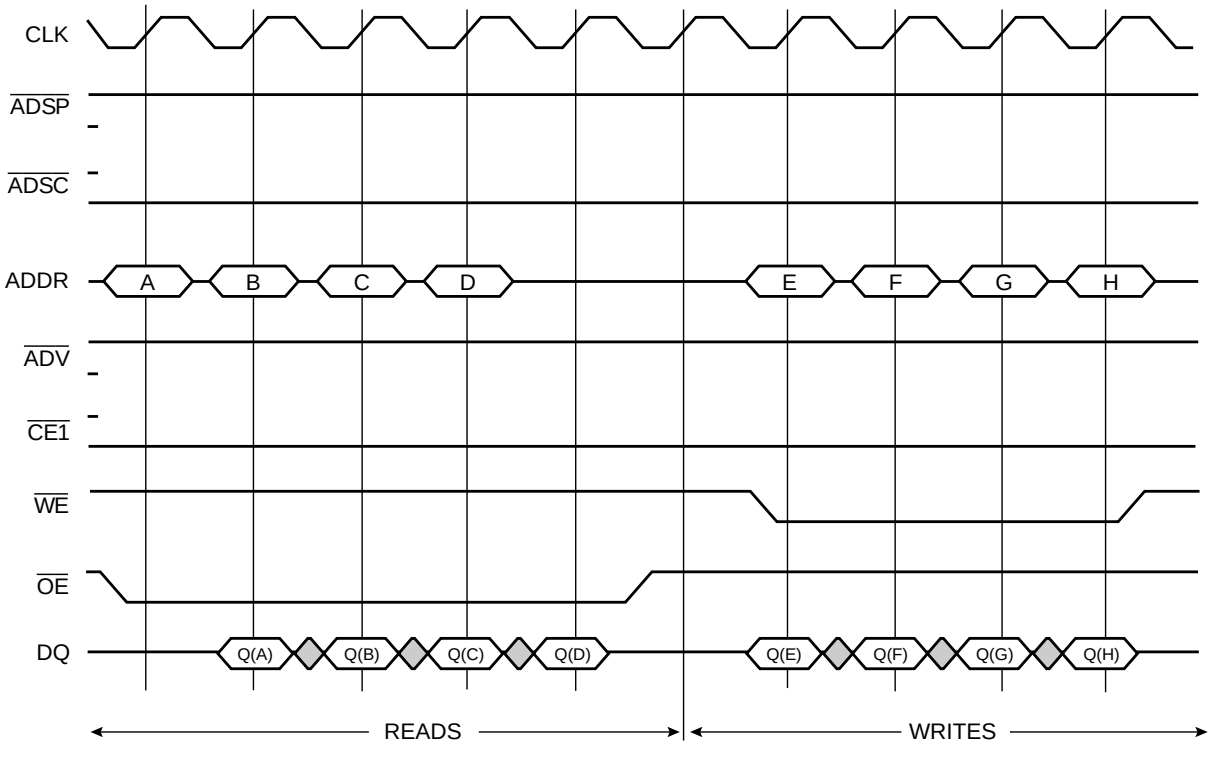
NOTES:
1. $\overline{E}$ is low when $\overline{CE}$ = low, CE2 = high and $\overline{CE2}$ = low. $\overline{E}$ is high otherwise.
2. $\overline{BWx}$ and $\overline{GW}$ are ignored for the first cycle when $\overline{ADSP}$ initiates the burst. $\overline{ADSP}$ active loads a new address into the address counter and forces the first cycle to be a read cycle.
3. $\overline{OE}$ is high before data input setup.

Sleep Mode Timing Diagram



NOTES: 1. Data retention is guaranteed when ZZ is asserted and clock remains active.
2. $\overline{ADSC}$ and $\overline{ADSP}$ must not be asserted for at least 100 ns after leaving ZZ state.

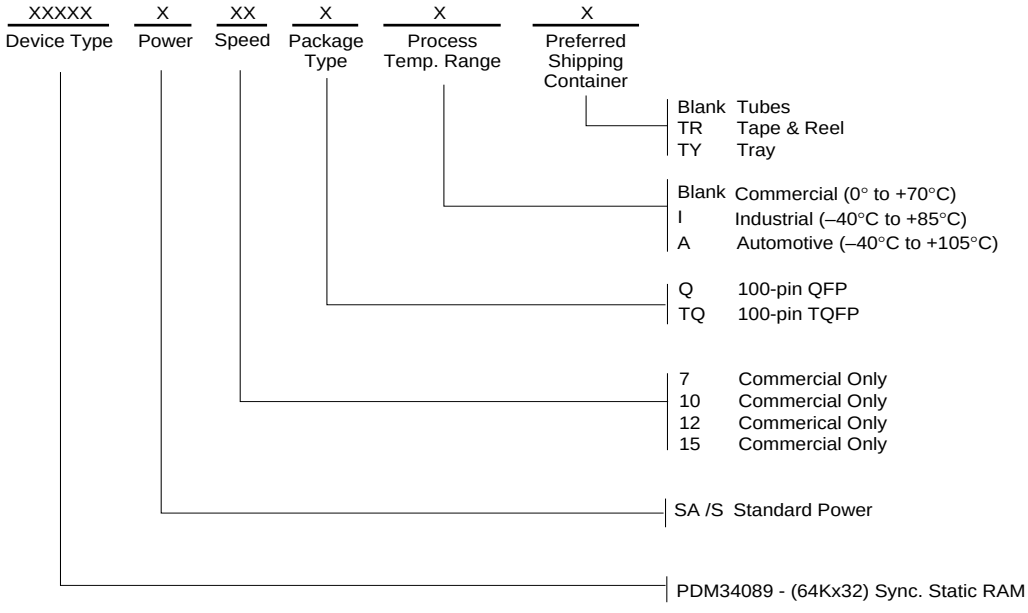
Sequential Non-burst Read and Write Timing Diagram



NOTES:

1. $\overline{ADSP}$ = high, $\overline{ADSC}$ = low, $\overline{ADV}$ = high, $\overline{CE1}$ = low.
2. $H \geq V_{IH}$, $L \leq V_{IL}$.

Ordering Information



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