PPP Packet Processor 155 Mbps MegaCore Function (PP155)

December 14, 2000; ver. 1.00 Data Sheet

Features

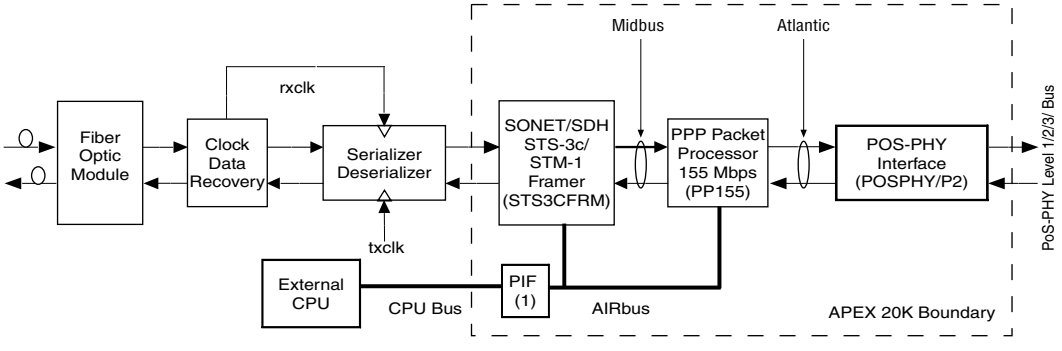
- Easy-to-use MegaWizard® Plug-In generates MegaCore® variants
- Quartus™ software and OpenCore™ feature allow place-and-route, and static timing analysis of designs prior to licensing
- Secure Register Transfer Level (RTL) simulation models allow simulation with user design in third-party simulators
- Full-duplex processing capability
- Octet-synchronous mode operation
- High-Level Data Link Control (HDLC)-type framing
- Up to 155.52 megabits per second (Mbps) transmission rate
- 16- or 32-bit Frame Check Sequence (FCS)
- Single channel processor (no interleaving)
- Internet Request For Comments (RFC) 1662 compliant (some sections are not implemented)
- Optimized for the Altera® APEX™ 20KE device architecture

Typical Applications

Figure 1 shows an example system implementation of the PP155 interfacing with two other Altera MegaCore variants to achieve PPP over SONET. The Midbus and Atlantic interfaces allow the PP155 to connect to several other devices including:

- T3 carrier processor
- Ethernet Media Access Controller (MAC)
- Direct Memory Access (DMA) controller
- Packet switch router

Figure 1. Typical Application



Note:
(1) PIF—Processor Interface Block

A-DS-IP155PACK-01

Functional Description

The PP155 is capable of performing HDLC-type framing. It operates in full-duplex mode, and comprises two blocks, as illustrated in Figure 2.

The following list of functions is based on a full feature PP155.

- High-Level Data Link Control Receiver (RXHDLC)
  - Inputs packets from the Midbus interface
  - Aligns the receive bytes (software programmable)
  - Descrambles the receive frame and between-frame flags using a self-synchronizing scrambler (software programmable)
  - Detects the Start Of Frame (SOF)
  - Decodes and removes byte stuffing
  - Checks the receive FCS, and removes the FCS from the frame (software programmable)
  - Outputs packets to the Atlantic interface

- High-Level Data Link Control Transmitter (TXHDLC)
  - Takes packets from the Atlantic interface
  - Byte stuffs control bytes for data transparency
  - Calculates the FCS on the packet data (before stuffing), and appends the FCS to the end of the packet
  - Sends one or more HDLC flag(s) after the end of the FCS until a new packet is available
  - Scrambles the transmit frame and between-frame flags using a self-synchronizing scrambler (software programmable)
  - Outputs frames to the Midbus interface

Interfaces & Protocols

Three interfaces support the PP155: the Middle interface (Midbus), the Access to Internal Registers (AIRbus) interface, and the Atlantic interface.

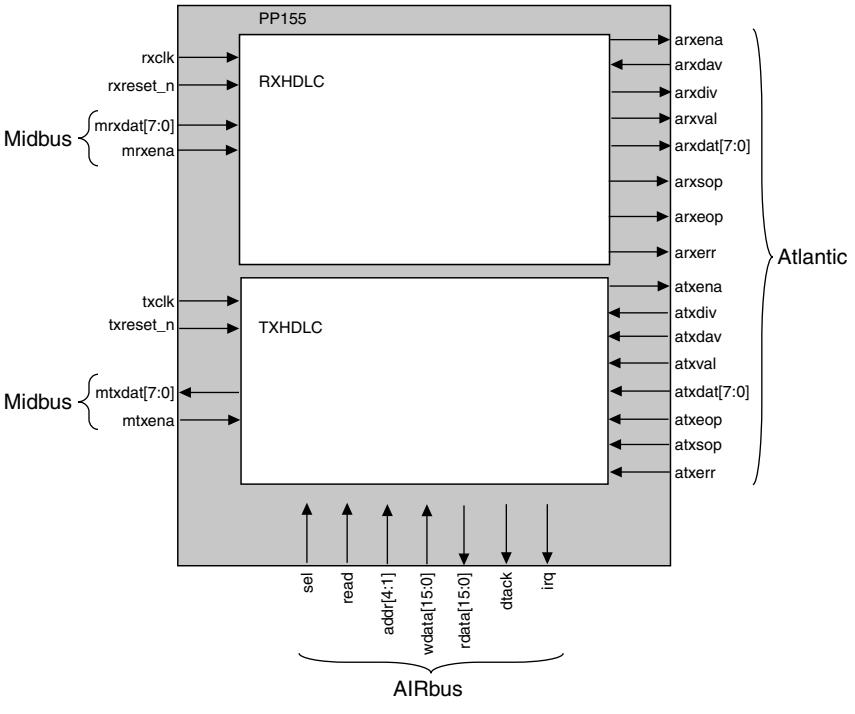
The Midbus interface is a simple synchronous full-duplex data path bus. The PP155 Midbus runs at 19.44 MHz over a single byte lane in each direction. In the receive direction (RX), data is transferred from the Midbus master to the slave (PP155). In the transmit direction (TX), data is transferred from the slave (PP155) to the master. In each direction, the Midbus can carry eight bits per clock cycle. It includes midbus receive data (`mrxdat[7:0]`) and midbus receive enable (`mrxena`) lines to indicate valid data transfers in the RX direction, and midbus transmit data (`mtxdat[7:0]`) and midbus transmit enable (`mtxena`) lines to indicate valid data requests in the TX direction. Since the PP155 is a slave to the Midbus it can work with any Midbus master.

The AIRbus interface provides access to internal registers using a simple synchronous internal bus protocol. This consists of separate read data (`rdata[15:0]`) and write data (`wdata[15:0]`) buses, a data transfer acknowledge (`dtack`) signal, and a select (`sel`) signal. An address (`addr[4:1]`) bus and read (`read`) signal indicate the location and type of access within the block. The `rdata` buses and `dtack` signals can be merged from multiple blocks using a simple OR function. The `dtack` signal is sustained until the block `sel` is removed (four-way handshaking) meaning the AIRbus can cross clock domain boundaries. The PP155 is an AIRbus slave with a data width of 16 bits.

The Atlantic interface is a full-duplex synchronous bus protocol supporting both packets and cells. The PP155 is an Atlantic interface master using an 8-bit wide data path to deliver packets to the slave. An example of a slave is the POS-PHY MegaCore variant shown in Figure 1. The POS-PHY MegaCore variant includes a First In First Out (FIFO) buffer for crossing the clock domain.

More detailed information on the Midbus, AIRbus, and Atlantic is available from the Altera web site at **http://www.altera.com/IPmegastore**.

Figure 2. Block Diagram



Pin-Outs

The following lists the ports for the PP155. The signal direction is indicated by (I) for input and (O) for output.

RX Clock Domain Signal: `rxclk` (I); **Midbus Signals:** `mrxdat[7:0]` (I), `mrxena` (I); **Atlantic Signals:** `arxena` (O), `arxdav` (I), `arxdiv` (O), `arxval` (O), `arxdat[7:0]` (O), `arxsop` (O), `arxeop` (O), `arxerr` (O).

AIRbus Signals: `sel` (I), `read` (I), `addr[4:1]` (I), `wdata[15:0]` (I), `rdata[15:0]` (O), `dtack` (O), `irq` (O).

TX Clock Domain Signals: `txclk` (I), `txreset_n` (I); **Midbus Signals:** `mtxdat[7:0]` (O), `mtxena` (I); **Atlantic Signals:** `atxena` (O), `atxdiv` (I), `atxdav` (I), `atxval` (I), `atxdat[7:0]` (I), `atxsop` (I), `atxeop` (I), `atxerr` (I).

Performance

Table 1 shows the required speed and estimated gate count of PP155 in an APEX 20KE device.

Table 1. Performance *Note (1)*

LEs	ESBs	f_{MAX} (MHz)
1,251	0	19.44 required to support 155.52 Mbps

Note:
(1) The numbers for the Logic Elements (LEs) and Embedded System Blocks (ESBs) are approximate as of Dec. 13, 2000.

Licensing

No license is required to perform the following trial operations using your own custom logic:

- Instantiation
- Place-and-Route
- Static Timing Analysis
- Simulation on a third-party simulator

Only when you are ready to generate programming files, do you need to obtain licenses through your local Altera sales representative.

All current variants use a single license with ordering code: PLSM-PP155.

Deliverables

The following elements are provided with the PP155 package:

- Data Sheet
- User Guide
- Interface Functional Specifications (AIRbus, Midbus, Atlantic, etc.)
- MegaWizard Plug-In
  - Encrypted gate level netlist
  - Place and Route constraints (where necessary)
  - Secure RTL simulation model
- Sanity test bench
- Access to problem reporting system

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