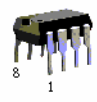
PJ393
Dual Voltage Comparator

The PJ393 is dual independent precision voltage comparators capable of single- or split-supply operation.
specifications as low as 2.0 mV make this device an excellentground level with single-supply operation. Input offset-voltage selection for many applications in consumer automotive, and It is designed to permit a common mode range-to- industrial electronics.

DIP-8 SOP-8



Pin : 1. Output 5. Input B
2. Input A 6. Input B
3. Input A 7. Output B
4. Gnd 8. Vcc

FEATURES

- Output voltage compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels
- Low input bias current -25 nA
- Low input offset current -5.0 nA
- Low input offset voltage --5.0 mV(max)
- Input common mode range to ground level
- Differential lnput voltage range equal to power supply voltage
- Very low current drain independent of supply voltage - 0.4 mA
- Wide single-supply range - 2.0 Vdc to 36 Vdc
- Split-supply range - ±1.0 Vdc to ±18 Vdc

ORDERING INFORMATION

Device	Operating Temperature	Package
PJ393CD	-20℃ +85℃	DIP-8
PJ393CS		SOP-8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to 36	Vdc
Input Current (2) (Vin -0.3 Vdc)	I_{in}	50	mA
Output Short Circuit Duration	I_{SC}	Continuous	mA
Output Sink Current (1)	I_{sink}	20	
Power Dissipation@T_A=25 ℃ Plastic DIP			
Derate above 25℃	P_D	570	mW
	$1/R_{\theta JA}$	5.7	mW/℃
Maximum Operating Junction Temperature	$T_{J(max)}$	125	℃
PJ393	T_{stg}	-65 to 150	℃

ELECTRICAL CHARACTERISTICS

(V_{CC} = 50Vdc, 0℃≤T_A≤ 70℃ unless otherwise stated)

Characteristics	Symbol	PJ393 Min	PJ393 Typ	PJ393 Max	Unit
Input Offset Voltage (3)	V_{IO}				mV
T_A =25 ℃		--	±1.0	±5.0	
-20 ℃≤ T_A ≤85 ℃		--	--	9.0	
Input Offset Current	I_{IO}				nA
T_A =25 ℃		--	±5.0	±50	
-20 ℃ ≤ T_A ≤85℃		--	--	±150	
Input Offset Current (4)	I_{IB}				nA
T_A =25℃		--	25	250	
-20 ℃ ≤T_A ≤ 85 ℃		--	--	400	
Input Common Mode Voltage Range (4)	V_{ICR}			V_{CC}-1.5	Volts
T_A =25℃		0	--	V_{CC}-2.0	
-20 ℃≤T_A ≤85 ℃		0	--		
Voltage Gain	A_{VOL}	50	200	--	V/mV
R_L≥15K , V_{CC} = 15 Vdc.					
T_A =25 ℃					
Large Signal Response Time	--	--	300	--	ns
Vin = TTL Logic Swing.					
Vref = 1.4 Vdc					
VRL = 5.0 Vdc. RL 5.1 KΩ					
T_A =25 ℃					
Response Time (6)	t_{TLH}	--	1.3	--	μs
VRL = 5.0 Vdc RK = 5.1 KΩ					
T_A =25℃					
Input Differentral Voltage (7)	V_{ID}	--	--	V_{CC}	V
All Vin ≥ Gnd or V-Supply					
(if used)					
Output Sink Current	L_{sink}	60	16	--	mA
V_{in-} ≥ 1.0 Vdc V_{in+} = 0 Vdc					
V_{O-} ≤15 Vdc T_A =25 ℃					
Output Saturation Voltage	V_{OL}				mV
V_{in-} ≥ 1.0 Vdc. V_{in+} = 0		--	150	400	
I_{sink} ≤ 4.0 mA, T_A = 25 ℃					
-20 ℃ ≤ T_A ≤ 85 ℃		--	--	700	
Output Leakage Current	I_{OL}				nA
V_{in-} = 0V, V_{in+}≥ 1.0Vdc		--	0.1	--	
VP = 50 Vdc. T_A =25℃					
V_{in-} = 0V, V_{in+} ≥ 1.0 Vdc		--	--	1000	
V_O =30 Vdc -20℃ ≤ T_A ≤ 85℃					
Supply Current	L_{CC}				mA
R_L = ∞ T_A =25℃		--	0.4	1.0	
R_L = ∞ V_{CC} =30 V		--	--	2.5	

Notes:

1. The max. Output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the input leads are driven more negative than guound or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative.This will not destroy the device and normal output states will recover when the inputs become -0.3 V of ground or negative supply.
3. At output switch point, V_O = 1.4 Vdc, R_S = 0Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common-mode
4. Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.
5. Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} - 1.5 V but either or both inputs can betaken to as high as 30 volts without damage.
6. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
7. The comparator will inhibit proper output state if one of the inputs become greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than -0.3 volts of ground of minus supply.

FIGURE 1- CIRCUIT SCHEMATIC
(Diagram shown is for 1 comparator)

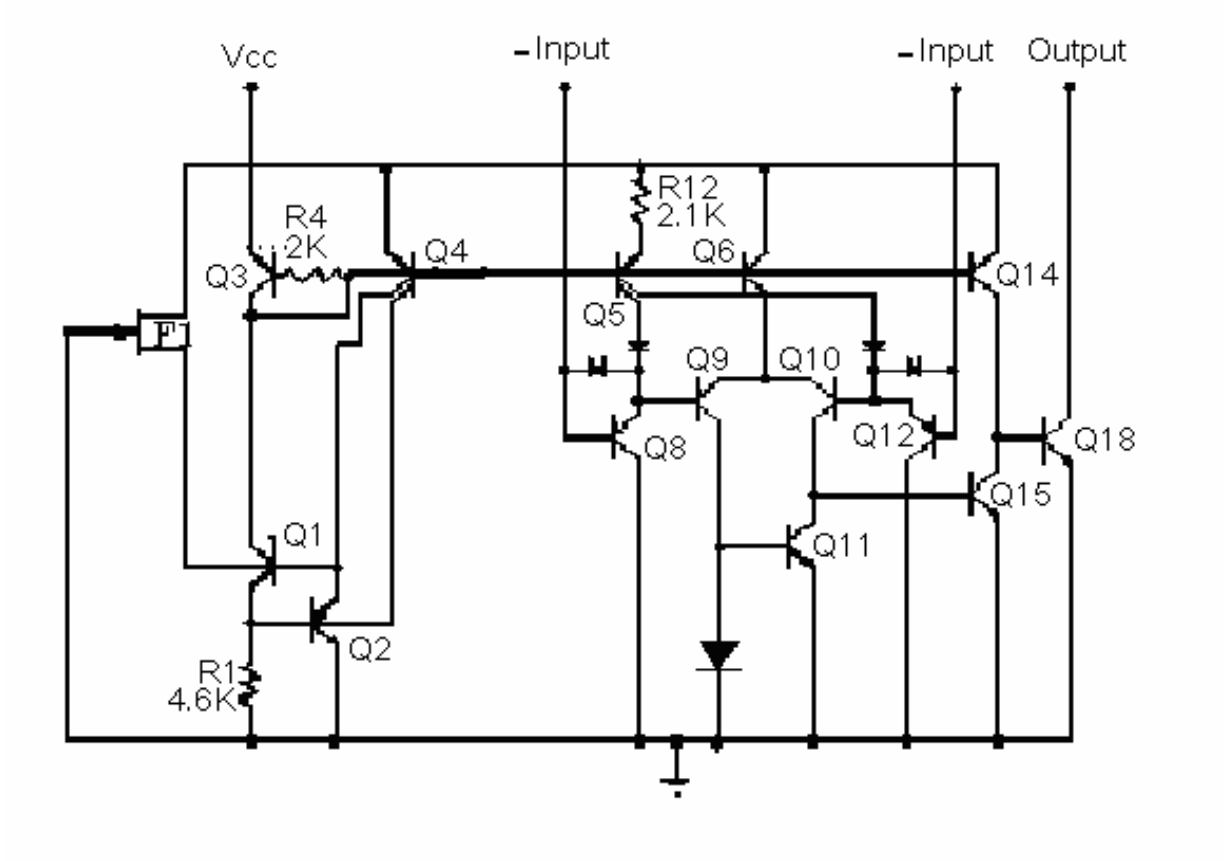


FIGURE 2 - INPUT BIAS CURRENT versus POWER SUPPLY VOLTAGE

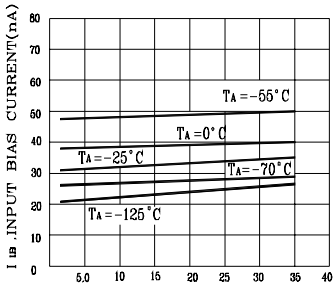


FIGURE 4 - POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

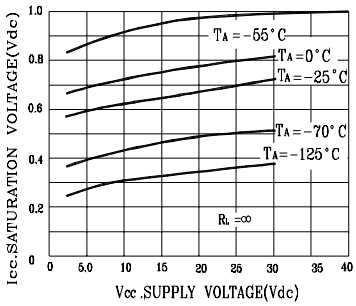
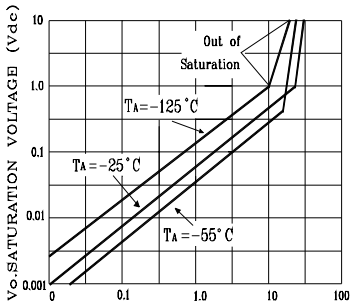


FIGURE 3 - OUTPUT SATURATION VOLTAGE versus OUTPUT SINK CURRENT



APPLICATIONS INFORMATION

This dual comparator feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capactively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors <10KΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3 V should not be used.

FIGURE 5 - ZERO CROSSING DETECTOR (Single Supply)

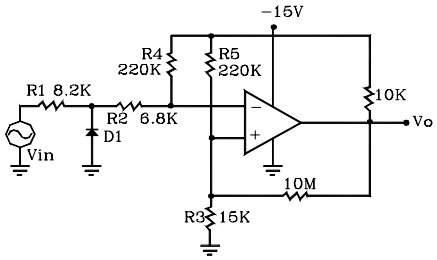


FIGURE 6 - ZERO CROSSING DETECTOR (Split Supplies)

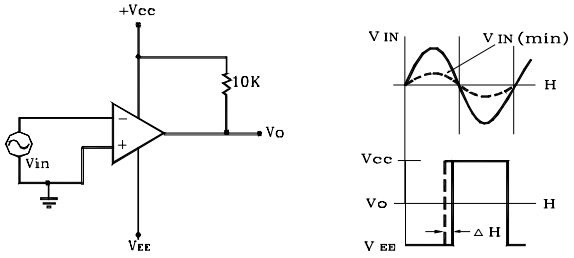


FIGURE 7 - ZERO CROSSING DETECTOR

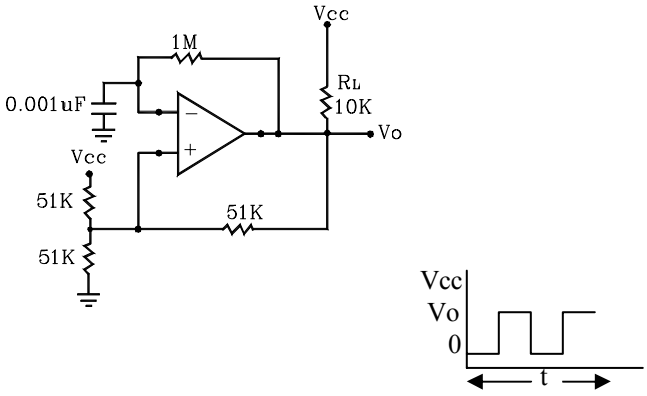


FIGURE 8 - TIME DELAY GENERATOR

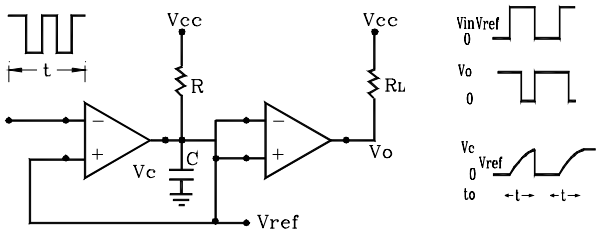
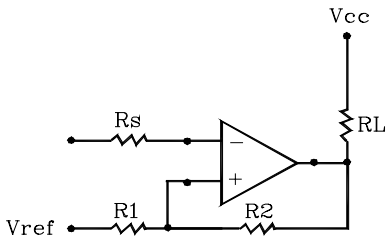


FIGURE 9 - COMPARATOR WITH HYSTERESIS

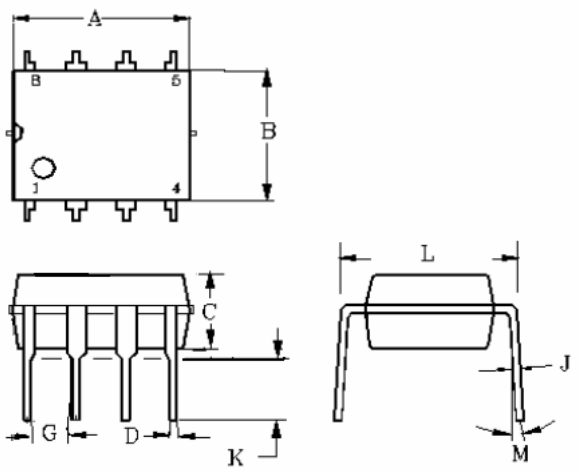
$R_S = R1 = R2$

$$Vth1 = Vref * \frac{(Vcc * Vref) * R1}{R1 * R2 * R_L}$$

$$Vth2 = Vref * \frac{(Vref * VoLow) * R1}{R1 * R2 * R_L}$$

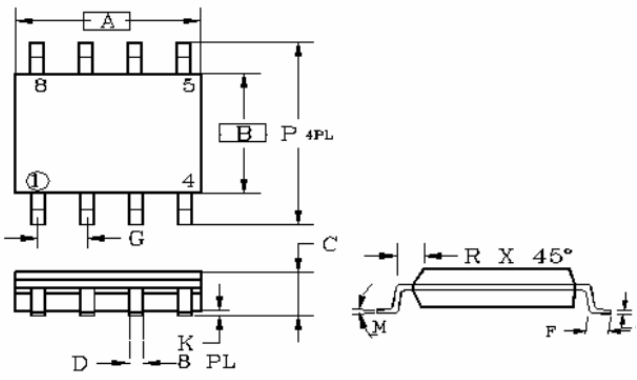


DIP-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	9.32	0.357	0.367
B	6.22	6.48	0.245	0.255
C	3.18	4.43	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54BSC		0.10BSC	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10°	-	10°

SOP-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019