SHORT FORM SPECIFICATION

P16WA032

Smart*XA*-Family

Secure 16-bit Smart Card Controller

Short Form Specification
Revision 1.0

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Philips
Semiconductors

PHILIPS

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Note: Specification may be changed without further notice.

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1 DESCRIPTION

Philips Semiconductors Smart*XA* (eXtended Architecture) is a secured 16-bit microcontroller, manufactured in an advanced CMOS process. It is specifically designed for security application in a multi-application and multi-provider environment.

As a member of the Philips Smart Card Controller family the Smart*XA* provides continuously enhanced security features, which make the device suited for high-end safeguarded applications. It is designed for embedding into chip cards according to ISO 7816.

Special attention was drawn to the design of the security architecture, in order to achieve the high degree of protection against attacks. Each security measure is designed to act as an integral part of the complete security system in order to strengthen the design as a whole. The security measures are solely controlled by hardware and do not allow for software guided exceptions.

The EEPROM memory can be used as data memory or as program memory. It contains a high reliability cell which guarantees data integrity. This is especially important when the EEPROM is used as memory for native programs.

The Philips Semiconductors Smart*XA* family of 16-bit single-chip Smart Card Controllers is powerful enough to easily handle the requirements of high performance, high security applications, yet inexpensive enough to compete in the market for high-volume, low-cost applications.

The Smart*XA* family provides an upward compatibility path for Smart Card Controller based on 80C51 (like the P83C8xx/P83W8xx Family of Crypto and Non-Crypto Controllers from Philips). Existing 80C51 code can also easily be translated to run on Smart*XA* microcontrollers.

Smart*XA* is the right choice for users looking for high performance, more memory capabilities and two operation modes - System and User mode - providing hardware firewall security. Thus, application access to memories and peripheral functions like I/O, Timer, Crypto co-processor is restricted by a hardware protection scheme under control of the System mode only.

The performance of the Smart*XA* architecture supports the comprehensive bit-oriented operations of the 80C51 while incorporating support for multi-tasking operating systems and high-level languages such as C. The speed of the Smart*XA* architecture, 10 to 100 times that of the 80C51, gives designers an easy path to truly high performance embedded control.

The integrated co-processor Fame*X* accelerates the encipherment for Public Key encryption algorithms. This widens the field of applications for this device, since it can be used as a tamper-resistant security tool for secured and authenticated communication in open networks.

The bi-directional communication with the device can be performed through two serial interface I/Os according to ISO standard 7816-3. The I/Os can run under full control of the kernel operating system (System mode) software in order to allow for conditional controlled access to the different internal memories.

Further functionality is provided by a UART for fast serial data transfer according ISO/IEC 7816-3 to accomplish fast personalization time, two 16-bit timers, which can be used as baud rate generator or time-out of serial data transmission and task timing control, seven vectorized interrupts from the I/Os, timers, UART, EEPROM and Fame*X* co-processor.

The Smart*XA* provides three power saving modes with reduced activity: the IDLE, the SLEEP and the CLOCK STOP mode. These modes are activated by software.

The P16WA032 operates with a single 3 V or 5 V power supply at a maximum clock frequency of 8 MHz.

The software development for the User ROM is supported by

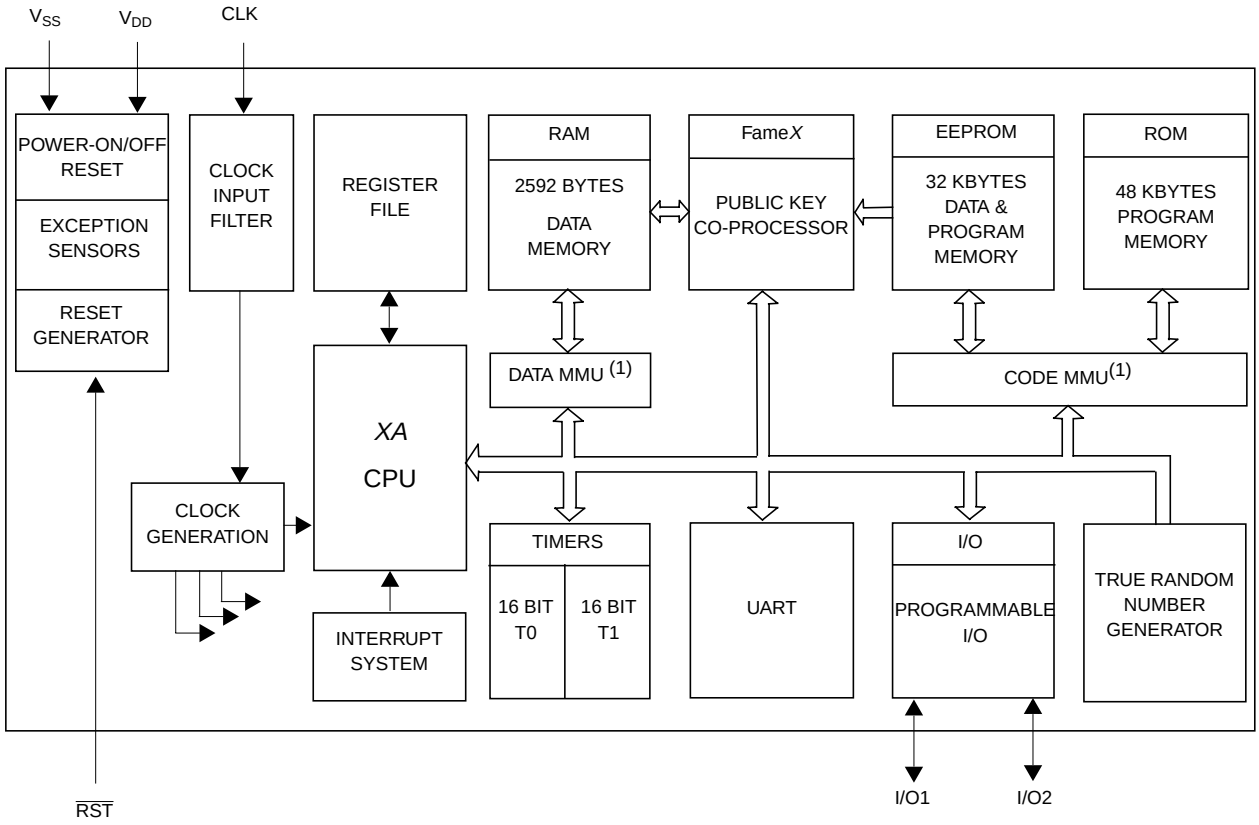
- Ashling Ultra-Emulator platform, stand alone ROM prototyping boards and ISO 7816 card interface board *(www.ashling.com)*
- Raisonance, RKitPXA, RKitEXA Development Suite (includes RIDE, C-Compiler, Assembler, Simulator, card interface board and Realtime Emulator) *(www.raisonance.com)*
- the SCP Smart*XA* Prototyping Board for stand-alone execution of prototype Smart*XA* programs

for real-time testing of the firmware especially in the Smart Card terminal environment.

On-chip hardware functions are controlled via Special Function Registers (SFRs). Their usage is described in the respective sections of this specification as the SFRs are correlated to the activities of CPU, Memory Management Unit, EEPROM, Interrupt, I/O, Timer 0/1, etc.

The P16WA032 is available as sawn wafer and as semi-finished IC-card micro module. Prototyping is supported by a small-outline package (SO28).

2 BLOCK DIAGRAM



(1) MMU = Memory Management Unit

Fig.1 Block Diagram P16WA032.

3 FEATURES

3.1 FAMILY STANDARD FEATURES

- Full 16-bit architecture
  - 16-bit fully static CPU
  - Harvard architecture: separate data- and program memory
  - EEPROM for data storage and program execution
- Hardware firewall security providing System mode and User mode with memory protection
- Dynamic Memory Management Unit (MMU) for program and data memory
- 80C51 compatible submode
- 16 Mbytes program memory address range with ROM and EEPROM
- 1 MByte data memory address range with RAM and EEPROM
- Versatile page mode EEPROM programming
- Byte/Wordwise EEPROM read access
- True Random Number Generator
- UART for fast serial data transfer
  - according ISO/IEC 7816-3, supporting protocol types T=0 and T=1
  - to accomplish fast personalization
  - to provide fast application download capabilities
- 21 16-bit CPU registers
  - 4 banks of R0 to R3 registers for fast context switching plus R4 to R7 registers, each capable of performing all arithmetic and logic operations
  - separate stack pointers for System mode and User mode
- Complex instruction set
  - all commands scalable as 8 or 16-bit
  - tailored for high level languages
  - including bit-wise operations as well as fast 16 x 16 multiply and 32/16 divide
- Multi-tasking and real-time executive support with
  - flexible interrupt structure
  - segmented data memory
  - multiple stacks for easy context-switching
- Multiple source vectorized interrupt system comprising
  - 16 software trap interrupts
  - 7 hardware event interrupts
  - 7 software interrupts
  - 7 system exception interrupts
- Multiple source reset system
- Power-saving IDLE mode
- Low-power SLEEP and CLOCK STOP mode
- I/O-interface for S/W, and H/W functions UART and External Interrupt
- Pad configuration according to ISO 7816-3: V_{SS}, V_{DD}, CLK, $\overline{RST}$, I/O1
- Second 1-bit I/O port for full-duplex serial data communication; can be left unconnected if only one I/O is required.

3.2 SECURITY FEATURES

- Hardware firewall and dynamic MMU
- Power-on reset
- Low supply voltage sensor (LVS)
- High supply voltage sensor (HVS)
- Low clock frequency sensor (LFS)
- High clock frequency sensor (HFS)
- High temperature sensor (HTS)
- Low temperature sensor (LTS)
- Clock input filter for protection against spikes
- On-chip self test utilizing signature techniques
- EEPROM programming timing independent from external clock
- EEPROM programming operation controlled by hardware sequencer
- On-chip EEPROM programming voltage generation
- Electronic fuses for safeguarded mode and write access control
- 32 EEPROM bytes for customer-defined security FabKey, featuring batch-, wafer- or die-individual security data

3.3 PRODUCT SPECIFIC FEATURES

- 48 KBytes User ROM
- 2592 bytes DATA RAM
- 32 KBytes EEPROM
- Versatile page mode EEPROM programming of 1 to 64 bytes at a time
- Typical EEPROM page mode programming time: 4.0 ms
- 1 s typical personalisation time for full 32 KBytes EEPROM (program-only mode)
- EEPROM endurance: minimum 100.000 programming cycles per byte
- EEPROM data retention time: 10 years minimum
- Crypto co-processor Fame*X* (Fast Accelerator for Modular Exponentiation-e*X*tended) optimized for public key cryptographic calculations
  - the major Public Key Cryptosystems like RSA, El'Gamal, DSS, Diffie-Hellmann, Guillou-Quisquater, Fiat-Shamir and elliptic curve cryptosystems (ECC) are supported
  - 2048 bits maximum key length for RSA with randomly chosen modulus
  - 3 register banks for fast operation mode switching
  - < 400 ms typical encryption time of 1024-bit RSA with randomly chosen modulus
  - 32-bit key length increments
  - boolean operations for acceleration of standard, symmetric cipher algorithms
- Software configurable clock system for CPU and co-processor Fame*X*
  - supporting CPU clock equal to external CLK
    - 2 × external CLK
    - $^1/_2$ external CLK
    - $^1/_4$ external CLK
    - $^1/_8$ external CLK
  - supporting Fame*X* clock equal to external CLK
    - 8 MHz (internal)
    - 16 MHz (internal)
    - 32 MHz (internal)
- Two 16-bit timers, providing three modes of operation and four prescaler ratios, using the external CLK signal as the basic clock source.
- 1 MHz to 8 MHz external CLK frequency
- Wake-up from SLEEP and CLOCK STOP mode by Reset or External Interrupt
- Wake-up from IDLE mode by Reset, External Interrupt, Timer or UART Interrupts
- 2.7 V to 5.5 V extended operating voltage range
- –25 to +85 °C operating ambient temperature range
- 3.5 kV Electro Static Discharge (ESD) protection on ISO pads according to MIL Standard 883-C Method 3015.
- I_{DDQ} testing for enhanced product reliability.

3.4 SUPPORT

- Deliverable as sawn wafer on film frame carrier
- Deliverable as ISO7816 contact module
- Samples in small quantities in SO28 package
- Development support:
  - Ashling Microsystems development system with Windows based user interface
  - Raisonance RKitPXA, RKitEXA development suite
- Preservation of customer investments ensured by
  - Instruction set identical with Philips 80C51 XA [same (C) compiler, (macro) assembler and libraries (of tools or self-developed)]
  - Upward compatibility with 8-bit 80C51 submode (assembler source level)
  - Smooth design transitions for upgrades

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	VERSION	
P16WA032AEV/x..x	Module	8-contact modules on 35 mm film	SOT456DD4	–25 to +85
P16WA032AEW/x..x	FFC	sawn wafer on film frame carrier	–	

5 PINNING INFORMATION

5.1 Smart Card contacts

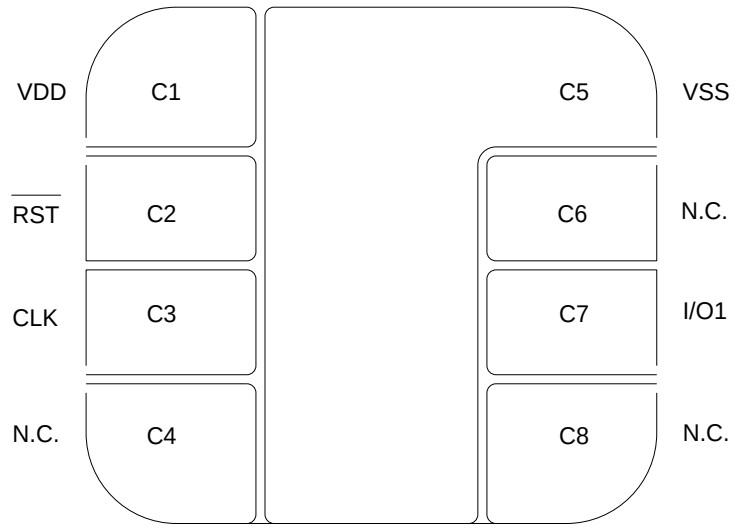


Fig.2 ISO contact assignments for SOT456DD4.

Table 1 Pin description

ISO 7816		P16WA032	
CONTACTS	SYMBOL	SYMBOL	DESCRIPTION
C1	VCC	VDD	Power supply voltage
C2	RST	$\overline{\text{RST}}$	Reset active LOW
C3	CLK	CLK	Clock
C4	reserved	N.C.	not connected
C5	GND	VSS	Ground (reference voltage)
C6	VPP	N.C.	not connected
C7	I/O	I/O1	Input/Output #1 for serial data
C8	reserved	N.C.	not connected

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