Philips P8xC591

CAN 2.0B Microcontroller

P8xC591 with CAN 2.0B is available in 44-pin PQFP & PLCC

The P8xC591 is a single-chip 80C51 microcontroller with an on-chip CAN controller. It uses the powerful 80C51 instruction set and includes the successful PeliCAN functionality of the SJA1000 stand-alone CAN controller.

The fully static core provides extended power save provisions because the oscillator can be stopped and easily restarted without loss of data. A key feature of the P8xC591 is its six clock operation (per machine cycle), which doubles the performance of the conventional 80C51; this is 500 ns instruction cycle time at 12 MHz external clock rate. Or, by keeping the same throughput, the clock frequency can be reduced in half, thus dramatically reducing the electromagnetic interference. So, a 12 MHz P8xC591 becomes a 24 MHz equivalent at a substantially improved EMC.

The P8xC591 is designed for use in industrial control applications such as medical equipment, office equipment, large industrial equipment, |and factory floor applications where reliability is a concern in a noisy environment. The 8xC591 incorporates all the functions of the Philips Rx+ core plus:

- CAN 2.0B controller (PeliCAN)
- PeliCAN features
- Six clocks for enhanced performance (500 ns at 12 MHz)
- Low active reset
- Six-input 10-bit ADC
- 32 I/Os
- Packaged in 44-pin PQFP or PLCC

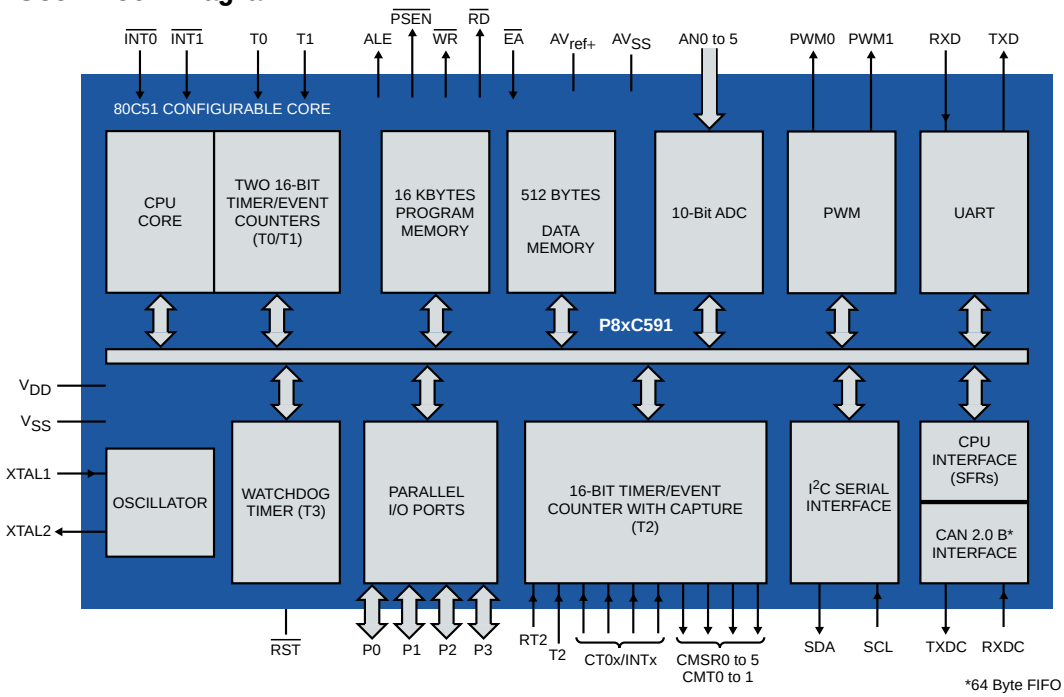
CAN Features of the 8xC591

- CAN 2.0B active controller, supporting 11-bit standard and 29-bit extended identifiers
- Up to 1 Mbit/s CAN bus speed at 8MHz clock
- 64-byte receive FIFO (can capture sequential data frames from the same source as required by the transport layer of higher protocols such as DeviceNet, CANopen and OSEK)
- 13-byte transmit buffer
- Enhanced PeliCAN core (CAN2.0B controller)
- Byte-oriented 1^2C master for external EEPROM store of device profiles

PeliCAN Features

- Controlled by five SF-register (fast access, no MOVX required)
- Fully integrated in C51 architecture (bit addressable)
- Four independently configurable acceptance filters
- Each acceptance filter has two 32-bit specifiers: a 32-bit match and a 32-bit mask
- 32-bits of mask per acceptance filter allows unique group addressing per acceptance filter
- Higher layer protocols especially supported in standard CAN format with:
  - up to four 11-bit ID acceptance filters that also screen the first two data bytes i.e., data frames are screened by CAN ID and by data byte content
- Up to eight 11-bit ID acceptance filters half of which also screens the first data byte
- All acceptance filters are changeable “on the fly”
- Bus arbitration and reception without CPU involvement
- DMA-access of FIFO by C51-core and PeliCAN
- Listen-only mode, self-test mode
- CAN Analyzer capabilities to monitor bus activity without participating in normal CAN acknowledgements
- Error code capture, arbitration lost capture, error counters with read/write access

P8xC591Block Diagram



*64 Byte FIFO Receiver with content and priority sensitive interrupts.

80C51 Features of the 8xC591

- Fully static 80C51 CPU available as OTP, ROM and ROM-less
- Second DPTR register
- 16 Kbytes internal program memory expandable externally to 64 Kbytes
- 512 bytes on-chip data RAM expandable externally to 64 Kbytes
- Three 16-bit timers/counters T0, T1 (standard 80C51) and additional T2 (capture & compare)
- 10-bit ADC with six multiplexed analog inputs with fast 8-bit ADC option
- Two 8-bit resolution, pulse width modulated outputs
- 32 I/O port pins in the standard 80C51 pin-out
- I^{2}C-bus serial I/O port with byte-oriented master and slave functions
- On-chip watchdog timer T3
- Extended temperature range: -40˚ to +85˚C
- Accelerated (prescaler 1:1) instruction cycle time 500ns at 12 MHz
- Operation voltage range: 5.0V +/-5%
- Security bits: ROM version has two bits, OTP/EPROM version has three bits
- 64-byte encryption array
- Four-level priority interrupt, 15 interrupt sources
- Full-duplex enhanced UART with programmable baud-rate generator
- Power control modes: Clock can be stopped and resumed, idle mode, power-down mode
- ALE inhibit for EMI reduction
- Programmable I/O port pins (pseudo bidirectional, push-pull, input only, open drain)
- Wake-up from power-down by external interrupts
- Software reset bit (AUXR1.5)
- Low active reset pin
- Power-on detect reset to allow operation with no external reset components
- ONCE (On Circuit Emulation Mode)

For more information, contact your Philips Semiconductors distributor or www.semiconductors.philips.com

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