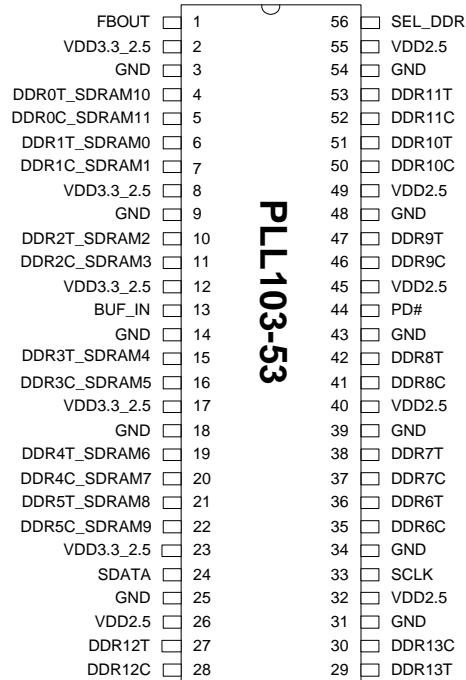


## DDR SDRAM Buffer with 5 DDR or 3 SDR/3 DDR DIMMS

### FEATURES

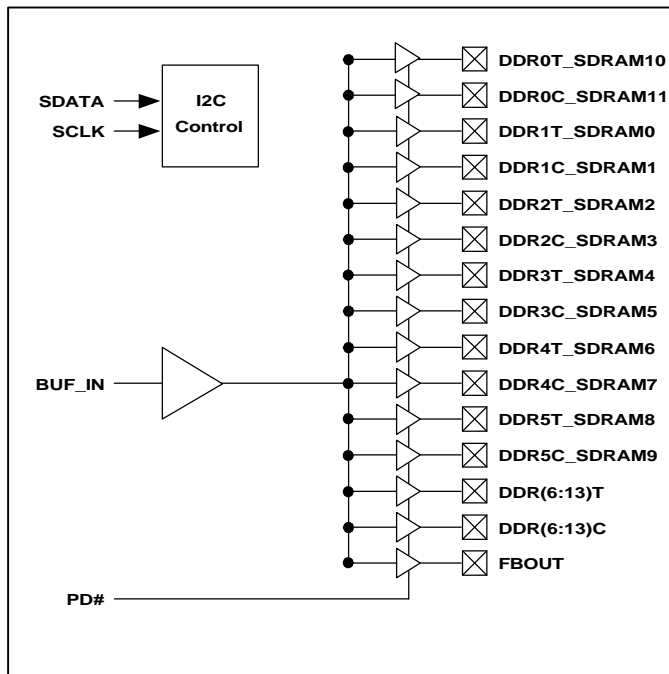
- Generates 30-output buffers from one input.
- Supports up to 4 DDR DIMMS or 3 SDR DIMMS and 2 DDR DIMMS.
- Supports 266MHz DDR SDRAM.
- One additional output for feedback.
- Less than 5ns delay.
- Skew between any outputs is less than 100 ps.
- 2.5V or 3.3V Supply range.
- Enhanced DDR and SDRAM Output Drive selected by I2C.
- Available in 56 pin SSOP.

### PIN CONFIGURATION



Note: #: Active Low

### BLOCK DIAGRAM



### DESCRIPTIONS

The PLL103-53 is designed as a 3.3V/2.5V buffer to distribute high-speed clocks in PC applications. The device has 30 outputs. These outputs can be configured to support 4 unbuffered DDR (Double Data Rate) DIMMS or to support 3 unbuffered standard SDR (Single Data Rate) DIMMS and 2 DDR DIMMS. The PLL103-53 can be used in conjunction with the PLL202-14/-54 or similar clock synthesizer for the VIA Pro 266 chipset.

The PLL103-53 also has an I2C interface, which can enable or disable each output clock. When power up, all output clocks are enabled (has internal pull up).

**DDR SDRAM Buffer with 5 DDR or 3 SDR/3 DDR DIMMS**
**PIN DESCRIPTIONS**

Name	Number	Type	Description
FBOUT	1	O	Feedback clock for chipset. Output voltage depends on VDD3.3_2.5V.
BUF_IN	13	I	Reference input from chipset. 3.3V input for STANDARD SDRAM mode; 2.5V input for DDR-ONLY mode.
PD	44	I	Power Down Control input. When low, it will tri-state all outputs.
SEL_DDR	56	I	Input configure for DDR-ONLY mode or STANDARD SDR mode. 1 = DDR-ONLY mode (when VDD3.3_2.5 select 2.5V); 0 = SDR mode (when VDD3.3_2.5 select 3.3V). In DDR-ONLY mode, all outputs will be configured as DDR outputs. In STANDARD SDR mode, pin 4, 5, 6, 7, 10, 11, 15, 16, 19, 20, 21 and 22 will be configured as STANDARD SDR outputs, and pin 27, 28, 29, 30, 35, 36, 37, 38, 41, 42, 46, 47, 50, 51, 52 and 53 will be configured as DDR outputs.
DDR[6:13]T	36,38,42,47, 51,53,27,29	O	These outputs provide True copies of BUF_IN.
DDR[6:13]C	35,37,41,46, 50,52,28,30	O	These outputs provide complementary copies of BUF_IN.
DDR[0,1:5]T_SDRAM [10,0,2,4,6,8]	4,6,10,15, 19,21	O	When SEL_DDR=1, these outputs provide DDR mode outputs; when SEL_DDR=0, these outputs provide standard SDRAM mode outputs. Voltage swing depends on VDD3.3_2.5.
DDR[0,1:5]C_SDRAM [11,1,3,5,7,9]	5,7,11,16, 20,22	O	When SEL_DDR=1, these outputs provide complementary copies of BUF_IN; when SEL_DDR=0, these outputs provide standard SDRAM mode outputs. Voltage swing depends on VDD3.3_2.5.
VDD3.3_2.5	2,8,12,17,23	P	When VDD=2.5V, SEL_DDR=1. DDR-ONLY mode is selected; when VDD=3.3V, SEL_DDR=0. STANDARD SDRAM mode is selected.
VDD2.5	32,40,45, 49,55	P	2.5V power supply.
GND	3,9,14,18, 25,31,34,39, 43,48,54	P	Ground.

**DDR SDRAM Buffer with 5 DDR or 3 SDR/3 DDR DIMMS**
**I2C BUS CONFIGURATION SETTING**

Address Assignment	A6 1	A5 1	A4 0	A3 1	A2 0	A1 0	A0 1	R/W —
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	<p>This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).</p> <p>Following the acknowledge of this address byte, in <b>Write Mode</b>: the <b>Command Byte</b> and <b>Byte Count Byte</b> must be sent by the master but ignored by the slave, in <b>Read Mode</b>: the <b>Byte Count Byte</b> will be read by the master then all other <b>Data Byte</b>. <b>Byte Count Byte</b> default at power-up is = (0x09).</p>							

**I2C CONTROL REGISTERS**
**1. BYTE 6: Outputs Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description			
Bit 7	56	1	SEL_DDR ( I2C is ready only, value is set through pin56 )			
Bit 6	-	0	SDRAM Drive.			
Bit 5	-	0	DDR Drive.			
Enhance Drive Control			Bit6	Bit5	DDR Drive	SDRAM Drive
			X	0	Enhanced 25%	Enhanced 25%
			0	1	Normal	Normal
			1	1	Normal	Enhanced 25%
Bit 4	27,28,29,30	1	DDR12T, DDR12C, DDR13T, DDR13C			
Bit 3	53, 52	1	DDR11T, DDR11C			
Bit 2	51, 50	1	DDR10T, DDR10C			
Bit 1	47, 46	1	DDR9T, DDR9C			
Bit 0	42, 41	1	DDR8T, DDR8C			

## DDR SDRAM Buffer with 5 DDR or 3 SDR/3 DDR DIMMS

### 2. BYTE 7: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	38, 37	1	DDR7T, DDR7C
Bit 6	36, 35	1	DDR6T, DDR6C
Bit 5	21, 22	1	DDR5T_SDRAM8, DDR5C_SDRAM9
Bit 4	19, 20	1	DDR4T_SDRAM6, DDR4C_SDRAM7
Bit 3	15, 16	1	DDR3T_SDRAM4, DDR3C_SDRAM5
Bit 2	10, 11	1	DDR2T_SDRAM2, DDR2C_SDRAM3
Bit 1	6, 7	1	DDR1T_SDRAM0, DDR1C_SDRAM1
Bit 0	4, 5	1	DDR0T_SDRAM10, DDR0C_SDRAM11

**DDR SDRAM Buffer with 5 DDR or 3 SDR/3 DDR DIMMS**
**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$	$V_{SS}-0.5$	7.0	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature	$T_A$	0	70	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

**2. Operating Conditions**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD3.3}$	3.135	3.465	V
Supply Voltage	$V_{DD2.5}$	2.375	2.625	V
Input Capacitance	$C_{IN}$		5	pF
Output Capacitance	$C_{OUT}$		6	pF

**3. Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	$V_{IH}$	All Inputs except I2C	2.0		$V_{DD}+0.3$	V
Input Low Voltage	$V_{IL}$	All inputs except I2C	$V_{SS}-0.3$		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$			TBM	uA
Input Low Current	$I_{IL}$	$V_{IN} = 0$			TBM	uA
Output High Voltage	$V_{OH}$	$I_{OL} = -12mA$ , $V_{DD} = 2.375V$	1.7			V
Output Low Voltage	$V_{OL}$	$I_{OL} = 12mA$ , $V_{DD} = 2.375V$			0.6	V
Output High Current	$I_{OH}$	$V_{DD} = 2.375V$ , $V_{OUT}=1V$	-18	-32		mA
Output Low Current	$I_{OL}$	$V_{DD} = 2.375V$ , $V_{OUT}=1.2V$	26	35		mA

**Note:** TBM: To be measured

**DDR SDRAM Buffer with 5 DDR or 3 SDR/3 DDR DIMMS**

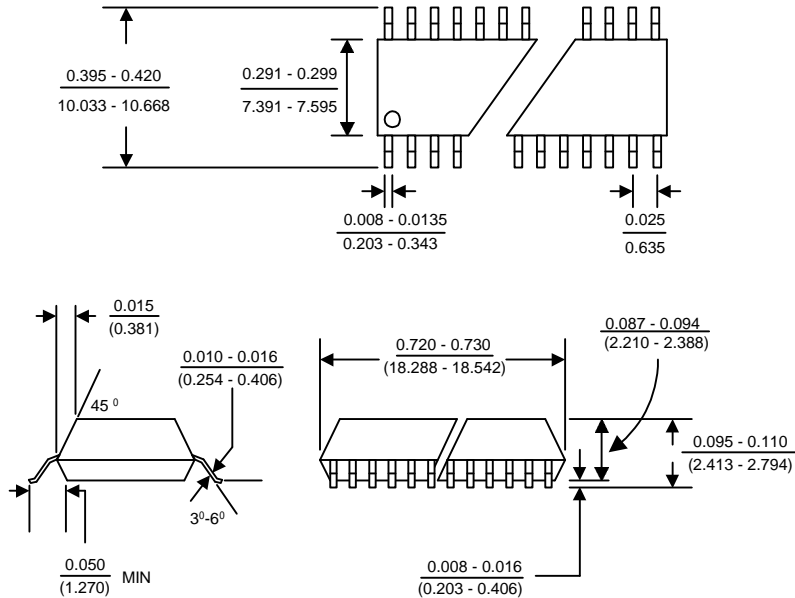
**3. Electrical Specifications (Continued)**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (DDR-only mode)	I <sub>DD</sub>	Unloaded outputs, 133MHz			TBM	mA
Supply Current (SDRAM mode)	I <sub>DD</sub>	Unloaded outputs, 133MHz			TBM	mA
Supply Current	I <sub>DDS</sub>	PD = 0			TBM	mA
Output Crossing Voltage	V <sub>OC</sub>		(VDD/2) - 0.1	VDD/2	(VDD/2) + 0.1	V
Output Voltage Swing	V <sub>OUT</sub>		1.1		VDD-0.4	V
Duty Cycle	D <sub>T</sub>	Measured @ 1.5V	45	50	55	%
Max. Operating Frequency			66		170	MHz
Rising Edge Rate	T <sub>OR</sub>	Measured @ 0.4V ~ 2.4V	1.0	1.5	2.0	V/ns
Falling Edge Rate	T <sub>OF</sub>	Measured @ 2.4V ~ 0.4V	1.0	1.5	2.0	V/ns
Clock Skew ( pin to pin )	T <sub>SKEW</sub>	All outputs equally loaded			100	ps
Stabilization Time	T <sub>ST</sub>				0.1	ms

**Note:** TBM: To be measured

**DDR SDRAM Buffer with 5 DDR or 3 SDR/3 DDR DIMMS**

**PACKAGE INFORMATION**



**56PIN SSOP**

**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range

**PLL103-53 X C**

PART NUMBER

TEMPERATURATURE  
C=COMMERCIAL  
M=MILITARY  
I=INDUSTRAL  
PACKAGE TYPE  
X=SSOP

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