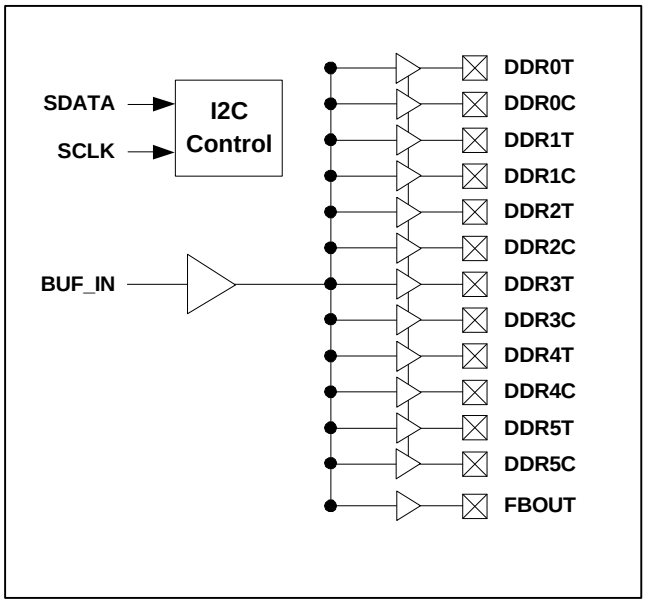
2 DIMM DDR Fanout Buffer

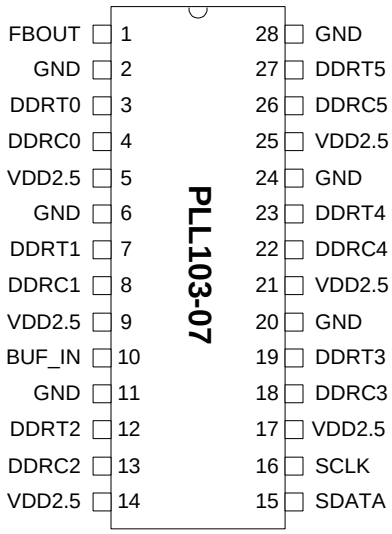
FEATURES

- Generates 12-output buffers from one input.
- Supports VIA Pro266 DDR chipset.
- Supports up to 2 DDR DIMMS.
- Supports up to 400MHz DDR, SDRAMS.
- One additional output for feedback.
- 6 differential clock distribution.
- Less than 5ns delay.
- Skew between any outputs is less than 100 ps.
- 2.5V Supply range.
- Available in 28-pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: #: Active Low

DESCRIPTIONS

The PLL103-07 is designed as a 2.5V buffer to distribute high-speed clocks in PC applications. The device has 12 outputs. These outputs can be configured to support 2 DDR DIMMs. The PLL103-07 can be used in conjunction with the PLL202-04 or similar clock synthesizer for the VIA Pro 266 chipset.

PIN DESCRIPTIONS

Name	Number	Type	Description
FBOUT	1	O	Feedback clock for chipset.
BUF_IN	10	I	Reference input from chipset.
DDRT[0:5]	3,7,12,19, 23,27	O	True clocks of differential pair outputs.
DDRC[0:5]	4,8,13,18, 22,26	O	Complementary clocks of differential pair outputs.
VDD2.5	5,9,14, 17,21,25	P	2.5V power supply.
GND	6,11,20,24	P	Ground.

I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in **Write Mode:** the **Command Byte** and **Byte Count Byte must be sent by the master** but ignored by the slave, in **Read Mode:** the **Byte Count Byte** will be **read by the master** then all other **Data Byte**. **Byte Count Byte** default at power-up is = (0x09).							

I2C CONTROL REGISTERS

1. BYTE 6: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	1	Reserved
Bit 2	27, 26	1	DDRT5, DDRC5
Bit 1	23, 22	1	DDRT4, DDRC4
Bit 0	19, 18	1	DDRT3, DDRC3

2. BYTE 7: Outputs Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	12, 13	1	DDRT2, DDRC2
Bit 3	-	1	Reserved
Bit 2	7, 8	1	DDRT1, DDRC1
Bit 1	-	1	Reserved
Bit 0	3, 4	1	DDRT0, DDRC0

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7.0	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. Operating Conditions

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD2.5}$	2.375	2.625	V
Input Capacitance	C_{IN}		5	pF
Output Capacitance	C_{OUT}		6	pF

3. Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except I2C	2.0		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except I2C	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			TBM	uA
Input Low Current	I_{IL}	$V_{IN} = 0$			TBM	uA
Output High Voltage	V_{OH}	IOL = -12mA, VDD = 2.375V	1.7			V
Output Low Voltage	V_{OL}	IOL = 12mA, VDD = 2.375V			0.6	V
Output High Current	I_{OH}	VDD = 2.375V, VOUT=1V	-18	-32		mA
Output Low Current	I_{OL}	VDD = 2.375V, VOUT=1.2V	26	35		mA

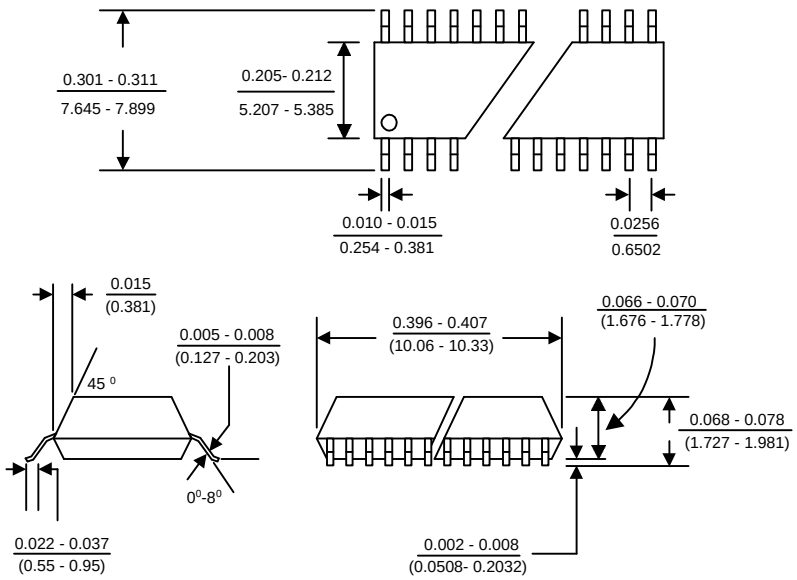
Note: TBM: To be measured

3. Electrical Specifications (Continued)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (DDR-only mode)	I_{DD}	Unloaded outputs, 133MHz			TBM	mA
Supply Current (SDRAM mode)	I_{DD}	Unloaded outputs, 133MHz			TBM	mA
Supply Current	I_{DDS}	PD = 0			TBM	mA
Output Crossing Voltage	V_{OC}		(VDD/2) -0.1	VDD/2	(VDD/2)+ 0.1	V
Output Voltage Swing	V_{OUT}		0.7		VDD-0.4	V
Duty Cycle	D_T	Measured @ 1.5V	45	50	55	%
Max. Operating Frequency			66		170	MHz
Rising Edge Rate	T_{OR}	Measured @ 0.4V ~ 2.4V	1.0	1.5	2.0	V/ns
Falling Edge Rate	T_{OF}	Measured @ 2.4V ~ 0.4V	1.0	1.5	2.0	V/ns
DDR Rising Edge Rate	T_{OR}	Measured between 20% to 80% of output	0.25	0.6	1.0	V/ns
DDR Falling Edge Rate	T_{OF}	Measured between 20% to 80% of output	0.25	0.6	1.0	V/ns
Clock Skew(pin to pin)	T_{SKEW}	All outputs equally loaded			100	ps
Stabilization Time	T_{ST}				0.1	ms

Note: TBM: To be measured

PACKAGE INFORMATION



28 PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL103-07 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP