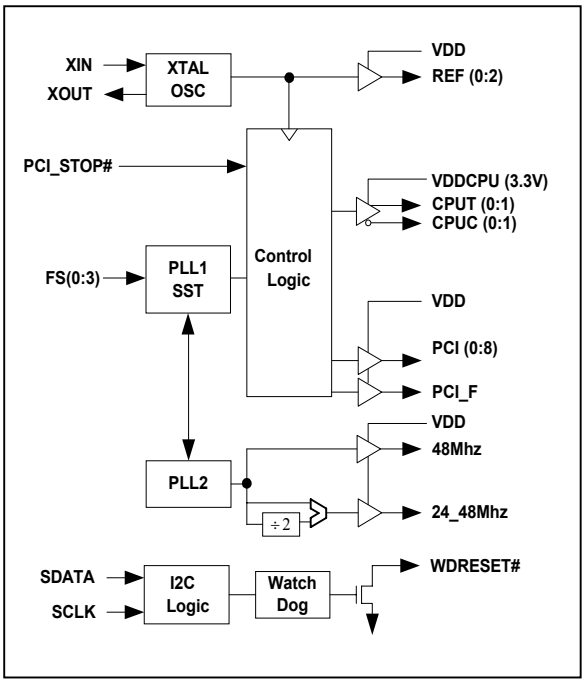
Programmable Clock Generator for AMD – K8™ and VIA – K8 ™

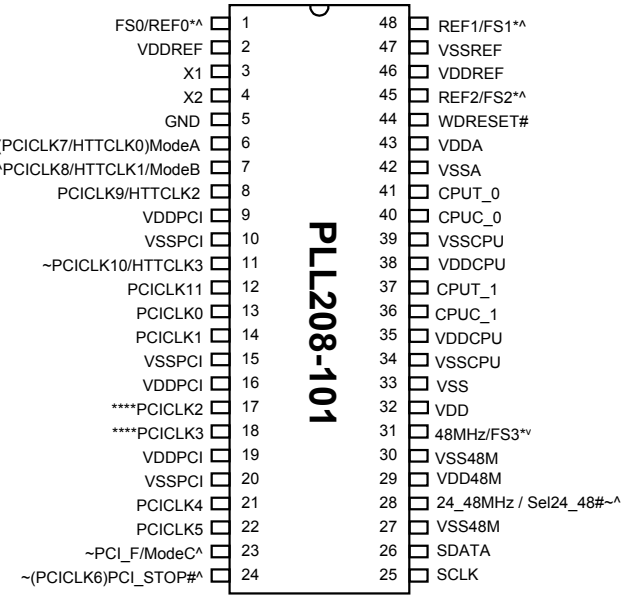
FEATURES

- Selectable Spread Spectrum Modulation between ±0.3% and -0.5%.
- AccuSkew ™ Programmable Precision skew tuning channel with maximum ±5% precision over the variation of temperature, process and voltage with step size as small as 80ps.
- AccuDrive ™ Programmable Output Buffer drive strength with 6mA step size.
- Programmable VCO frequency with one variable
- Programmable Output Divider for CPU, HTT and PCI clock.
- 2 - Differential pair push-pull CPUCLK.
- 9 - PCI (including 1 free running) with I^2C selectable doubled driving strength on PCI.
- 4 - Selectable PCI /HTT clock.
- 1 - 48MHZ for USB @3.3V fixed.
- 3 - REF 14.318MHz clock outputs.
- 1 - programmable 24MHz or 48MHz for SIO.
- I^2C serial interface for programmability features.
- Built-in programmable watchdog timer
- Available in 300 mil 48 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: ^ : Internal Pull Up (120kΩ), ᵛ : Internal Pull down (120kΩ),
* : Bi-directional latched at power-up
~ : This Output has 2X Drive Strength.
**** : This Output has 2.3X Drive Strength. # : Active low.

POWER GROUP

- VDDREF (3.3V), VSSREF: REF, XIN, XOUT
- VDDPCI (3.3V), VSSPCI: PCI
- VDD48M (3.3V), VSS48M: 48MHz, 24_48MHz
- VDDCPU (3.3V), VSSCPU: CPUT/C_[0:1]
- VDDA (3.3V), VSSA: PLL Analog
- VDDHTT (3.3V), VSSHTT: HTTT/C[0:1]

KEY SPECIFICATIONS

- CPU - CPU Output Skew < 150ps.
- PCI - PCI Output Skew <500ps
- CPU (early) to PCI Skew: 1 to 4 ns (Typ 2ns).
- CPU TO HTT Skew < 150ps.

Pin Descriptions

Name	Number	Type	Description
REF[0:2]/FS[0:2]	1,45,48	I/O	14.318MHz reference clock output. This pin latch FS[0:2] value at power-up.(See Frequency Selection table).
XIN	3	IN	14.318MHz crystal input to be connected to one end of the crystal.
XOUT	4	OUT	14.318Mhz crystal output
(PC1CLK7/HTTCLK0) ModeA	6	I/O	PCI clock output / Hyper Transport output / Mode selection pin, this input is activated by the ModeB selection pin.
(PCICLK8/HTTCLK1) ModeB	7	I/O	PCI clock output / Hyper Transport output / Mode selection latch input pin.
PCICLK9/HTTCLK2	8	OUT	PCI Clock output / Hyper Transport output.
~PCICLK10/HTTCLK3	11	OUT	PCI Clock output / Hyper Transport output.
PCICLK11	12	OUT	PCI Clock output.
PCICLK0	13	OUT	PCI Clock output.
PCICLK1	14	OUT	PCI Clock output.
****PCICLK2	17	I/O	3.3V LVTTL input for selection the current multiplier for CPU outputs / 3.3V PCI clock output.
****PCICLK3	18	I/O	Early/Normal PCI clock output latched at power up.
PCICLK4	21	OUT	PCI Clock output.
PCICLK5	22	OUT	PCI Clock output.
~^PCI_F/ModeC	23	I/O	Free running PCI clock not affected by PCI_STOP# / Mode selection latch input pin.
~^(PCICLK6)PCI_STOP#	24	I/O	PCI Clock output, this output is activated by the Mode selection pin / Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low.
SCLK	25	IN	Serial data inputs for serial interface port.
SDATA	26	I/O	Serial data inputs for serial interface port.
24_48MHz/ Sel24_48#~^	28	I/O	24MHz clock output / Latched select input for 24/48MHz output. 0 = 48MHz 1 = 24MHz
48MHz/FS3*ˇ	31	I/O	Frequency select latch input pin / Fixed 48MHz clock output.
CPU[C/T]_1	36,37	OUT	Differential push-pull K8 pair output.
CPU[C/T]_0	40,41	OUT	Differential push-pull K8 pair output.
WDRESET#	44	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
VDDPCI	9,16,19	PWR	3.3V Power Supply for PCI clock
VDD48M	29	PWR	3.3V Power Supply for 24/48MHz clock outputs.
VDDA	43	PWR	3.3V power for internal PLL.

VDDCPU	35,38	PWR	3.3V power supply for CPU clocks.
VDDREF	2,46	PWR	3.3V power supply for REF clocks
VDD	32	PWR	3.3V power supply
VSS	5,10,15, 20,27,30, 33,34,39, 42,47	PWR	Ground.

Mode Functionality Tables

ModeA	ModeB	Pin6	Pin7	Pin8	Pin11
0	0	HTTCLK0	HTTCLK1	HTTCLK2	PCICLK10
0	1	ModeA (Input only)	HTTCLK1	HTTCLK2	HTTCLK3
1	0	PCICLK7	PCICLK8	PCICLK9	PCICLK10
1	1	ModeA (Input only)	PCICLK8	PCICLK9	PCICLK10

ModeC	Pin24
0	PCICLK6
1	PCI_STOP#

Programmable Clock Generator for AMD – K8™ and VIA – K8 ™

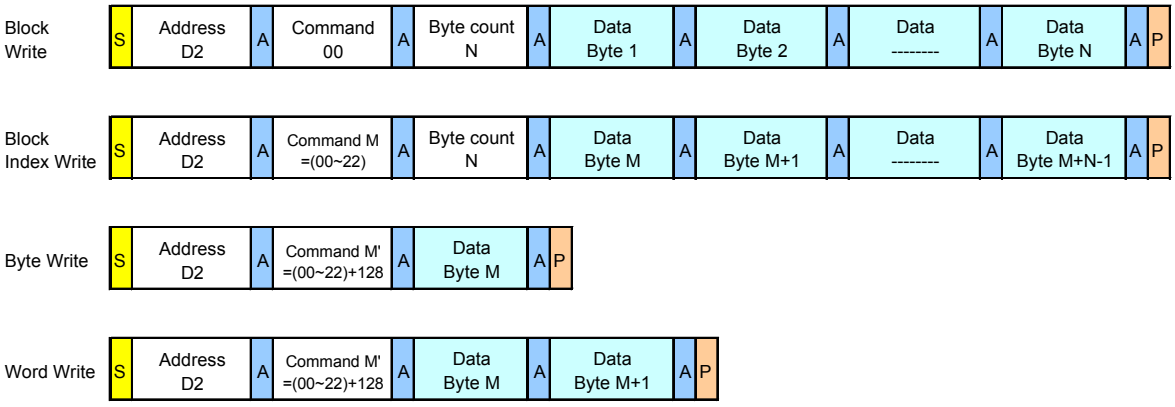
FREQUENCY (MHz) SELECTION TABLE

Bit5	Bit4	Bit3	Bit2	Bit1	CPU	HTT	PCI	SST Amp	VCO
	FS3	FS2	FS1	FS0					
0	0	0	0	0	100.90	67.27	33.63	±0.3% center	403.60
0	0	0	0	1	133.90	66.95	33.48	±0.3% center	535.60
0	0	0	1	0	168.00	67.20	33.60	±0.3% center	672.00
0	0	0	1	1	202.00	67.33	33.67	±0.3% center	404.00
0	0	1	0	0	100.20	66.80	33.40	±0.3% center	400.80
0	0	1	0	1	133.50	66.75	33.38	±0.3% center	534.00
0	0	1	1	0	166.70	66.68	33.34	±0.3% center	666.80
0	0	1	1	1	200.40	66.80	33.40	-0.5% down	400.80
0	1	0	0	0	270.00	67.50	33.75	±0.3% center	540.00
0	1	0	0	1	233.33	66.67	33.33	-0.5% down	466.66
0	1	0	1	0	266.67	66.67	33.33	±0.3% center	533.34
0	1	0	1	1	300.00	75.00	37.50	±0.3% center	600.00
0	1	1	0	0	150.00	60.00	30.00	±0.3% center	600.00
0	1	1	0	1	180.00	60.00	30.00	±0.3% center	360.00
0	1	1	1	0	210.00	70.00	35.00	±0.3% center	420.00
0	1	1	1	1	240.00	60.00	30.00	±0.3% center	480.00
1	0	0	0	0	100.00	66.67	33.33	-0.5% down	400.00
1	0	0	0	1	133.33	66.67	33.33	-0.5% down	533.32
1	0	0	1	0	166.66	66.66	33.33	-0.5% down	666.64
1	0	0	1	1	200.00	66.67	33.33	-0.5% down	400.00
1	0	1	0	0	103.00	68.67	34.33	±0.3% center	412.00
1	0	1	0	1	137.33	38.66	34.33	-0.5% down	549.32
1	0	1	1	0	171.66	68.66	34.33	±0.3% center	686.64
1	0	1	1	1	206.00	68.67	34.33	±0.3% center	412.00
1	1	0	0	0	278.10	69.53	34.76	±0.3% center	556.20
1	1	0	0	1	240.33	68.67	34.33	±0.3% center	480.66
1	1	0	1	0	274.67	68.67	34.33	±0.3% center	549.34
1	1	0	1	1	309.00	77.25	38.63	±0.3% center	618.00
1	1	1	0	0	154.50	61.80	30.90	±0.3% center	618.00
1	1	1	0	1	185.40	61.80	30.90	±0.3% center	370.80
1	1	1	1	0	216.30	72.10	36.05	±0.3% center	432.60
1	1	1	1	1	247.20	61.80	30.90	±0.3% center	494.40

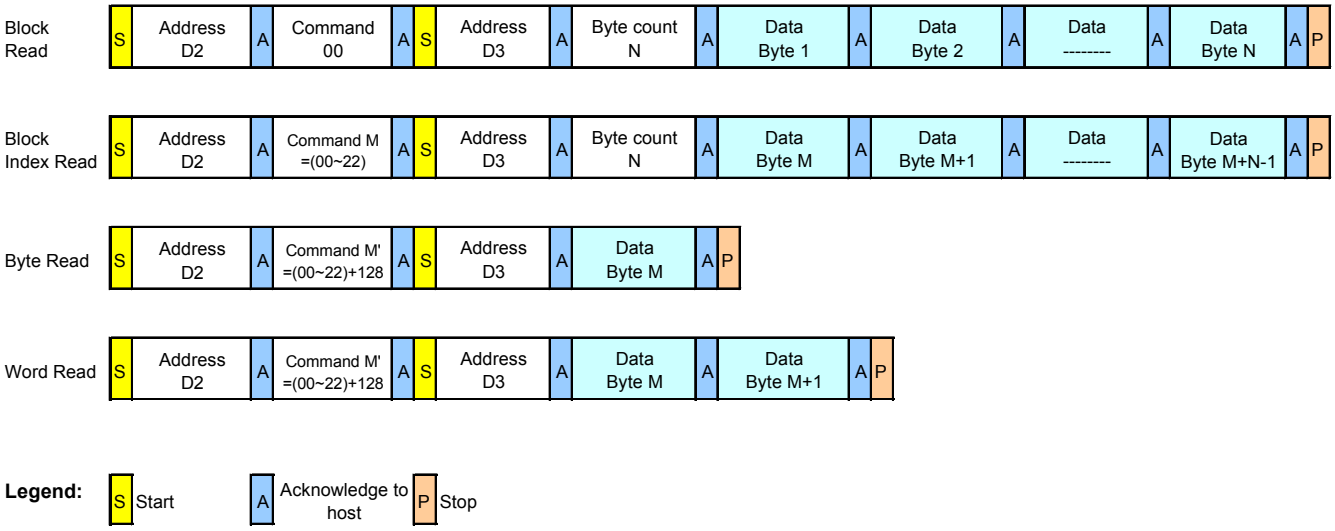
I2C BUS CONFIGURATION SETTING

Address Assignment	A6 A5 A4 A3 A2 A1 A0 R/W 1 1 0 1 0 0 1 _
Slave Receiver/Transmitter	Provides both slave write and read back functionality
Data Transfer Rate	Standard mode at 100kbits/s
Data Protocol	This serial interface is designed to allow multiple protocols to write and read from the controller. It includes Block Read/Write, Block Index Read/Write, Byte Read/Write and Word Read/Write. In general, the bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).

WRITE MODE



READ MODE



Legend: S Start | A Acknowledge to host | P Stop

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7		0	Spread Spectrum modulation amplitude selection. 0 = defined in Frequency Table. 1 = ±0.3% (center) fixed.
Bit 6		0	0 = normal, 1 = Spread Spectrum Enable
Bit 5		Power-up latched FS4 value	FS4
Bit 4	31	Power-up latched FS[0:3] value	FS3
Bit 3	45		FS2
Bit 2	48		FS1
Bit 1	1		FS0
Bit 0	-	0	Frequency selection bit 1=Via I2C, 0=Via External jumper

2. BYTE 1: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	PCICLK8/HTTCLK1 (1=Active, 0=Inactive)
Bit 6	-	1	PCICLK7/HTTCLK0 (1=Active, 0=Inactive)
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

3. BYTE 2: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	36,37	1	CPU[C/T]_1 (1=Active, 0=Inactive)
Bit 6	40,41	1	CPU[C/T]_0 (1=Active, 0=Inactive)
Bit 5	45	1	REF2 (1=Active, 0=Inactive)
Bit 4	48	1	REF1 (1=Active, 0=Inactive)
Bit 3	1	1	REF0 (1=Active, 0=Inactive)
Bit 2	28	1	24_48MHz (1=Active, 0=Inactive)
Bit 1	31	1	48MHz (1=Active, 0=Inactive)
Bit 0	8	1	PCICLK9/HTTCLK2

4. BYTE 3: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	12	1	PCI11 (1=Active 0=Inactive)
Bit 6	11	1	PCI10 (1=Active 0=Inactive)
Bit 5	23	1	PCI5 (1=Active 0=Inactive)
Bit 4	21	1	PCI4 (1=Active 0=Inactive)
Bit 3	18	1	PCI3 (1=Active 0=Inactive)
Bit 2	17	1	PCI2 (1=Active 0=Inactive)
Bit 1	14	1	PCI1 (1=Active 0=Inactive)
Bit 0	16	1	PCI0 (1=Active 0=Inactive)

5. BYTE 4: Output Control Register

Bit	Pin#	Default	Description
Bit 7		1	PCI_F (1=Active 0=Inactive)
Bit 6		1	PCICLK6 (1=Active 0=Inactive)
Bit 5		1	24_48SEL pin control, 1=24MHz, 0=48MHz.
Bit 4		1	Inverted Power-up latched FS3 value
Bit 3		1	Inverted Power-up latched FS2 value
Bit 2		1	Inverted Power-up latched FS1 value
Bit 1		1	Inverted Power-up latched FS0 value
Bit 0		1	PCICLK10/HTTCLK3 (1=Active 0=Inactive)

6. BYTE 5: Vendor ID and Revision ID Register

Bit	Pin#	Default	Description
Bit 7		0	Vendor ID Bit 3 (read only)
Bit 6		0	Vendor ID Bit 2 (read only)
Bit 5		1	Vendor ID Bit 1 (read only)
Bit 4		1	Vendor ID Bit 0 (read only)
Bit 3		0	Revision ID Bit 3 (read only)
Bit 2		0	Revision ID Bit 2 (read only)
Bit 1		0	Revision ID Bit 1 (read only)
Bit 0		0	Revision ID Bit 0 (read only)

7. BYTE 6: Linear Programming Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Linear programming sign bit (0 is “+”, 1 is “–”)
Bit 6	-	0	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0	Linear programming magnitude bit 5
Bit 4	-	0	Linear programming magnitude bit 4
Bit 3	-	0	Linear programming magnitude bit 3
Bit 2	-	0	Linear programming magnitude bit 2
Bit 1	-	0	Linear programming magnitude bit 1
Bit 0	-	0	Linear programming magnitude bit 0 (LSB)

8. BYTE 7: WATCHDOG Fall Back Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Watchdog Timer Unit Bit[7:6]: 00 = 250 ms, 01 = 500ms, 10 = 1s, 11 = 4s
Bit 6	-	0	
Bit 5	-	0	Initialization setting for Linear Programming Byte after Watch dog reset. 0= Byte 7 initialized to 0 after WD-Reset generated. 1= Byte 7 unchanged after WD-Reset generated.
Bit 4	-	0	Reserved
Bit 3	-	0	WDT Fall-back Frequency selection for FS3
Bit 2	-	0	WDT Fall-back Frequency selection for FS2
Bit 1	-	0	WDT Fall-back Frequency selection for FS1
Bit 0	-	0	WDT Fall-back Frequency selection for FS0

9. BYTE 8: WATCHDOG TIMER Register (1=Enable, 0=Disable)

Bit	Name	Default	Description
Bit 7	WDT ENB	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable
Bit 6	-	0	0=Watch Dog falls back to hardware jumper setting frequency 1=Watch Dog falls back to fall back frequency setting in Byte 8.
Bit 5	WDT<5>	0	Watchdog Time Interval Bit 5 (MSB)
Bit 4	WDT<4>	0	Watchdog Time Interval Bit 4
Bit 3	WDT<3>	0	Watchdog Time Interval Bit 3
Bit 2	WDT<2>	0	Watchdog Time Interval Bit 2
Bit 1	WDT<1>	0	Watchdog Time Interval Bit 1
Bit 0	WDT<0>	0	Watchdog Time Interval Bit 0 (LSB)

10. BYTE 9: Programming Mode Counter Register (1=Enable, 0=Disable)

Bit	Name	Default	Description
Bit 7	AccuSkew Enable	0	AccuSkew Setting for ±5% process independent accuracy. 1=enable, 0=disable.
Bit 6	-	0	Initialization setting for Skew Control and Buffer drive strength registers after Watch dog reset. 0= Byte 11~16 initialized to 0 after WD-Reset generated. 1= Byte 11~16 unchanged after WD-Reset generated.
Bit 5	WDT Status	0	Watch Dog Timer Status info (read only)
Bit 4			
Bit 3	SST Profile	0	0=linear, 1=non-linear
Bit 2	Accu-SST Enable	0	Accu-SST programming Enable: 1=via I2C Byte12, 0=via ROM setting.
Bit 1	Skew Enable	0	Enable Skew programming (byte 11~13). 1=enable, 0=disable.
Bit 0	VCO-N Enable	0	Enable VCO-N Counter programming (byte 20~21) 1=programming through setting I2C byte 20~21 0=programming through Frequency ROM setting.

11. BYTE 10: Spread Spectrum Modulation Amplitude Programming Register:

Bit	Name	Default	Description
Bit 7	-	1	Spread Spectrum mode selection. 1=Center Spread, 0=Down Spread.
Bit 6	SST6	1	1. Center Spread: SST<6:0> = Modulation rate * N / 7 2. Down Spread: SST<6:0> = Modulation rate * N /14
Bit 5	SST5	1	
Bit 4	SST4	1	
Bit 3	SST3	1	
Bit 2	SST2	1	
Bit 1	SST1	1	
Bit 0	SST0	1	

TABLE 1: Output Signals SKEW Programming Summary:

Bit<2:0>	Skew Setting I (±80ps/step)		Skew Setting II (±160ps/step)	
111	+320ps	Setting applies to the following outputs: 1. CPU0 2. CPU1	+640ps	Setting applies to the following outputs: 1. HTTCLK 2. All PCI
110	+240ps		+480ps	
101	+160ps		+320ps	
100	+80ps		+160ps	
011	**Default**		**Default**	
010	-80ps		-160ps	
001	-160ps		-320ps	
000	-240ps		-480ps	

12. Byte 11: SKEW Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	Skew CPU0	Bit <2>	0	These three bits will adjust timing of CPU_Host signals (CPUT_0/CPUC_0) either positive or negative delay up to +320ps or –240ps with ±80ps per step.
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	Skew CPU1	Bit <2>	0	These three bits will adjust timing of CPU_chip_sets signals (CPUT_1/CPUC_1) either positive or negative delay up to +320ps or –240ps with ±80ps per step.
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

13. Byte 12: SKEW Control Register

Bit	Name	Default	Description
Bit 7	CPU-PCI/HTT Skew	1	Skew setting between CPU and PCI/HTT clocks Bit[7:6]: 00 = 0.5 ns, 10 = 2 ns (default); 11 = 2.5ns
Bit 6		0	
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	Reserved
Bit 1	-	0	Reserved
Bit 0	-	0	Reserved

14. Byte 13: SKEW Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	-		0	Reserved
Bit 4	-		0	Reserved
Bit 3	-		0	Reserved
Bit 2	Skew PCI	Bit <2>	0	These three bits will adjust timing of all PCI clock signals either positive or negative delay up to +640ps or –480ps with ±160ps per step.
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

TABLE 2: Output Drive Strength Programming Summary:

Bit<2:0>	Setting I		Setting II	
111	+40%	Setting applies to the following outputs 1. HTTCLK[0:4] 2. 48M, 24_48MHz	+50%	Setting applies to the following outputs 1. PCI_F,PCI0 2. PCI[1:7] 3. REF[0:2]
110	+30%		+38%	
101	+20%		+25%	
100	+10%		+13%	
011	**Default**		**Default**	
010	-10%		-13%	
001	-20%		-25%	
000	-30%		-38%	

15. Byte 14: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	HTTCLK Strength	Bit <2>	0	These three bits will program drive strength for ZCLK0 and ZCLK1 output clocks (see Table 2).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	-		0	Reserved
Bit 1	-		0	Reserved
Bit 0	-		0	Reserved

16. Byte 15: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	USB Strength	Bit <2>	0	These three bits will program drive strength for 48MHz and 24_48MHz output clocks (see Table 2).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	PCI_F,PCI0 Strength	Bit <2>	0	These three bits will program drive strength for PCIF[0:1] and PCI0 output clocks (see Table 2).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

17. Byte 16: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	PCI[1:7] Strength	Bit <2>	0	These three bits will program drive strength for PCI[1:5] output clocks (see Table 2).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	REF Strength	Bit <2>	0	These three bits will program drive strength for REF[0:2] output clocks (see Table 2).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

TABLE 3: VCO Divider Programming Summary:

Bit<3:0>	High Speed Divider		Low Speed Divider	
1111	Default ROM Selection	1. CPU0 2. CPU1 3. HTTCLK	Default ROM Selection	1. PCI_F,PCI
1110	N/A		N/A	
1101				
1100				
1011				
1010	/16		/32	
1001	/14		/28	
1000	/12		/24	
0111	/10		/20	
0110	/8		/16	
0101	/7		/14	
0100	/6		/12	
0011	/5		/10	
0010	/4		/8	
0001	/3		/6	
0000	/2		/4	

18. Byte 17: VCO Divider Control Register

Bit	Name		Default	Description
Bit 7	CPU-Host Divider -	Bit <3>	1	These four bits will program VCO divider for CPUT_0 and CPUC_0 clocks (see Table 3).
Bit 6		Bit <2>	1	
Bit 5		Bit <1>	1	
Bit 4		Bit <0>	1	
Bit 3	CPU-CS Divider	Bit <3>	1	These four bits will program VCO divider for CPUC_1 and CPUT_1 clocks (see Table 3).
Bit 2		Bit <2>	1	
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

19. Byte 18: VCO Divider Control Register

Bit	Name		Default	Description
Bit 7	-		1	Reserved
Bit 6	-		1	Reserved
Bit 5	-		1	Reserved
Bit 4	-		1	Reserved
Bit 3	HTT Divider	Bit <3>	1	These four bits will program VCO divider for ZCLK clocks (see Table 3).
Bit 2		Bit <2>	1	
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

20. Byte 19: VCO Divider Control Register

Bit	Name		Default	Description
Bit 7			1	Reserved
Bit 6			1	Reserved
Bit 5			1	Reserved
Bit 4			1	Reserved
Bit 3	PCI Divider	Bit <3>	1	These four bits will program VCO divider for all PCI clocks (see Table 3).
Bit 2		Bit <2>	1	
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

21. BYTE 20: VCO N Counter Register:

Bit	Name	Default	Description
Bit 7	N<15>	1	VCO(MHz)= N<15:0> * 14.318/ 1024
Bit 6	N<14>	1	
Bit 5	N<13>	1	
Bit 4	N<12>	1	
Bit 3	N<11>	1	
Bit 2	N<10>	1	
Bit 1	N<9>	1	
Bit 0	N<8>	1	

22. BYTE 21: VCO N Counter Register

Bit	Name	Default	Description
Bit 7	N<7>	1	VCO(MHz)= N<15:0> * 14.318/ 1024
Bit 6	N<6>	1	
Bit 5	N<5>	1	
Bit 4	N<4>	1	
Bit 3	N<3>	1	
Bit 2	N<2>	1	
Bit 1	N<1>	1	
Bit 0	N<0>	1	

PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL208-101 device incorporates SMART-BYTE ™ technology with a single byte programming via I2C. Detail of PLL208-101's dual mode frequency programming method is described below:

1. **ROM-table Frequency Programming:**

   The pre-defined 32 frequencies found in Frequency table can be accessed through 4 external jumpers.

2. **Micro-step Linear Frequency Programming:**

   CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency changes. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha * M$$

Where:
1. M is magnitude factor defined in I2C Byte 7.bit (0:6)
2. ± (sign bit) of M is defined in I2C Byte7.bit 7
3. α is a constant equal to 0.22.

FREQUENCY PROGRAMMING EXAMPLE:

1. **Procedures to program target CPU frequency to 170 Mhz:**

   A. Locate the closest CPU frequency from Frequency-ROM table: 168
   B. α = 0.22
   C. Solve M (Linear Magnitude factor) in integer:

$$M = (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha$$
$$= (170 - 168) / 0.22$$
$$= 9$$

   D. Program I2C register:

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
Sign	M6	M5	M4	M3	M2	M1	M0

Setting of M = +9 in I2C.BYTE 7

F_{CPU} = 168 + (0.22) * 9 = 169.98 (% of frequency increased vs. ROM Table = 1.83 %)
F_{PCI} = 36 * (1 + 1.83 %) = 36.66

BUILT-IN WATCHDOG TIMER (WDT)

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into "Hang-up" state within a reasonable period of time (or Watchdog time interval). While disabled, the watchdog time interval can be programmed between 0 and 63 seconds with increment of 1 second by setting the value of I2C.Byte8.Bit(5:0). Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL208-101 will start from predefined Fall-back Frequency (the value of I2C Byte6, bits(5:3)). If system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

Example usage:

1. System power-up at CPU= 66.6MHz where external jumpers are used.

2A. Switch to target CPU=100.0MHz frequency with following I2C register setting:

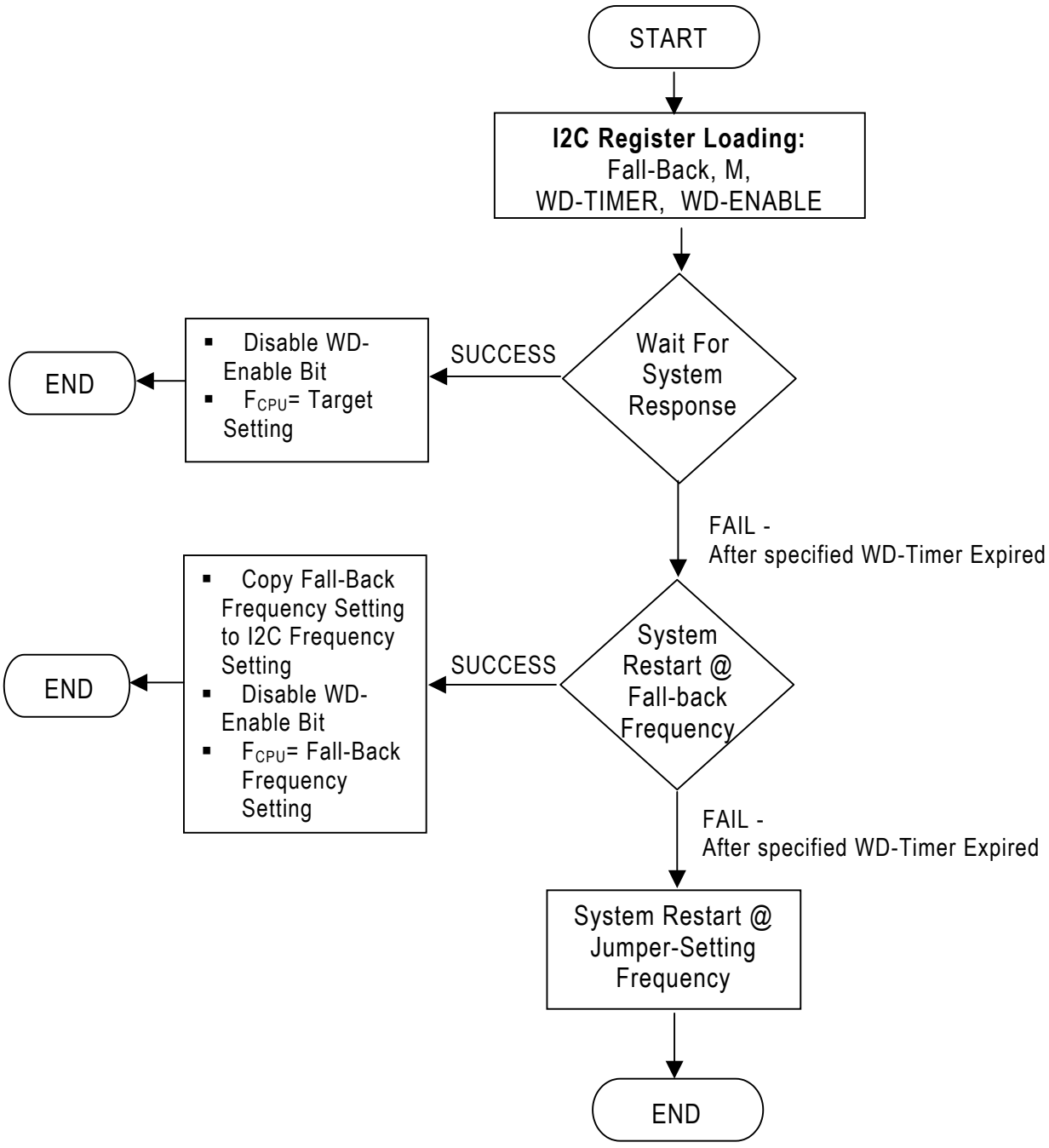
7	6	5	4	3	2	1	0		
0	0	0	0	0	0	0	0	M =0	Setting in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0		
7	6	5	4	3	2	1	0		
1	0	0	0	1	1	1	1	WD-Timer = 15s	Setting in I2C.BYTE8
ENB		T5	T4	T3	T2	T1	T0		
7	6	5	4	3	2	1	0		
0	0	0	0	1	0	0	0	FBSEL	Setting in I2C.BYTE6
FB4	FB3	FB2	FB1	FB0					

The fall-back frequency is set to the same location as that of FSEL since frequency switching between different timing groups will cause system to hang up. After WD timer expired or 15 seconds, the system will restart properly at target 100.0MHz if CPU is capable; otherwise WDT will perform another reset action to restart the system from 66.8 Mhz

2B. Switch to target CPU=103Mhz within the same timing Group

The fall-back frequency is recommended to set at the most safe and comfortable level to ensure a successful reboot such as 100 if system is unable to switch to 103Mhz.

WDT OPERATIONAL FLOW CHART



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC/AC Electrical Specifications

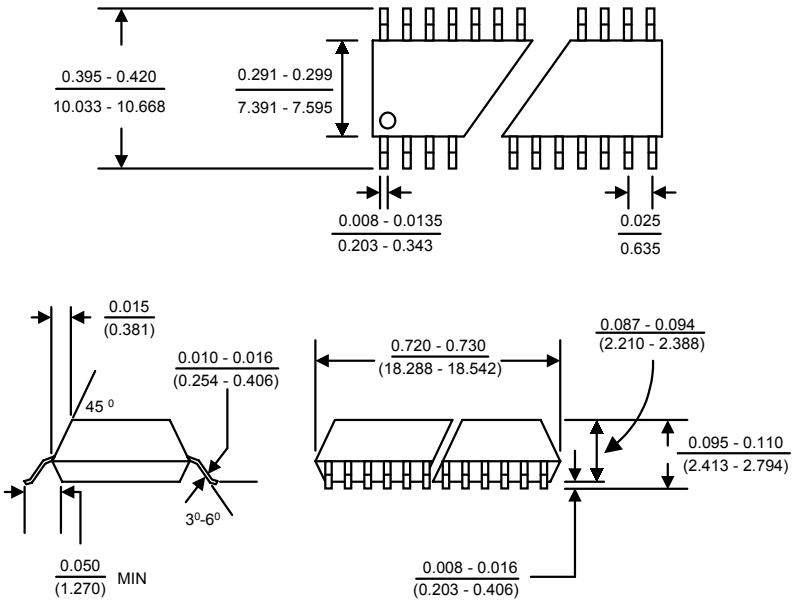
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	uA
Input Low Current	I_{IL1}	V_{IN}=0 with no pull-up resistor	-5			uA
Input Low Current	I_{IL2}	V_{IN}=0 with pull-up resistor	-200			
Supply Current	I_{DD}	C_L=0 pF@66MHz, 3.3V±5%			180	mA
	I_{DDL}	C_L=0 pF@133MHz, 3.3V±5%				
Transition Time	T_{trans}	To 1st crossing of target Freq.			3	ms
Input frequency	F_I	V_{DD} = 3.3V	12	14.318	16	MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	XIN & XOUT pins	27	28	45	pF

2. DC/AC Electrical Specifications (continued)

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU	Measured @ 0.4V ~ 2.0V, C_L=10-20pf, 3.3V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 0.4V ~ 2.4V, C_L=10-20pf			4	
		PCI_F, PCI	Measured @ 0.4V ~ 2.4V, C_L=10-30pf			2	
Output Fall time	T_{OF}	CPU	Measured @ 2.0 ~ 0.4V, C_L=10-20pf, 3.3V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 2.4V ~ 0.4V, C_L=10-20pf			4	
		PCIF, PCI	Measured @ 2.4V ~ 0.4V, C_L=10-30pf			2	
Duty Cycle	D_T	CPU, APIC, REF, 48MHz,24MHz	Measured @ 1.5V C_L=20pf	45	50	55	%
		PCI	Measured @ 1.5V, C_L=20~30pf	40		55	
Clock Skew	T_{SKEW}	CPU	Rising edge @ 1.25V, C_L=20pf			175	ps
		PCI	Rising edge @ 1.5V, C_L=30pf			500	
Jitter(Cycle to Cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		REF	Measured @ 1.5V			500	
		PCI	Measured @ 1.5V			250	
Frequency Stabilization Time	T_{FST}	CPU,PCI_F,PCI, REF, 48MHz,24MHz	Assumes full supply voltage reached within 1ms from power-up. Short cycle exist prior to frequency stabilization.			3	ms
AC output impedance	Z_0	CPU	V_{DD}=3.3V(2.5V)±5%		20		ohm
		PCI	V_{DD}=3.3V±5%		30		
		REF,48MHz,24MHz	V_{DD}=3.3V±5%		40		

PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL208-101 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP