

Power PC Clock Generator with Integrated 0-delay Buffer for Printer

FEATURES

- 1 CPU Clock output with selectable frequencies (33, 50, 66, 83, 100, 133, 150 or 166 MHz).
- 2 ASIC output clocks (at CPU speed)
- 4 PCI output clocks.
- Output buffer enable/disable ability for PCI, BUFOUT, ASIC and CPU.
- Selectable Spread Spectrum (SST) for EMI reduction on ASIC, CPU and PCI.
- Advanced, low power, sub-micron CMOS processes.
- 14.31818MHz fundamental crystal input.
- Low EMI Spread Spectrum Technology is available for the CPU, ASIC and PCI clock.
- Available in 48-Pin SSOP

FREQUENCY TABLES

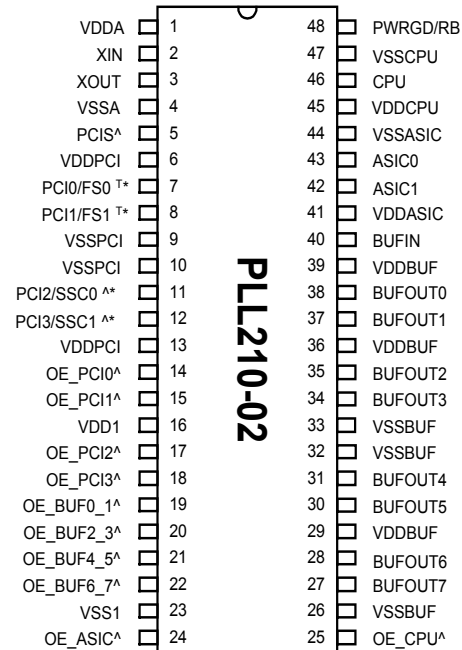
FS1	FS0	CPU	ASIC(0:1)
0	0	33.3 MHz	33.3 MHz
0	M	50.0 MHz	50.0 MHz
0	1	66.6 MHz	66.6 MHz
M	0	83.3 MHz	83.3 MHz
M	M	100.0 MHz	100.0 MHz
M	1	133.3 MHz	133.3 MHz
1	0	150.0 MHz	150.0 MHz
1	M	166.6 MHz	166.6 MHz

PCIS	PCI (1:3)
0	33.3 MHz
1	66.6 MHz

SPREAD SPECTRUM SELECTION TABLE

SSC1	SSC0	Spread Spectrum Modulation
0	0	OFF
0	1	- 0.50% – Downspread
1	0	- 1.00% – Downspread
1	1	- 1.50% – Downspread

PIN ASSIGNMENT



Notes: [^]: Internal pull-up resistor * : Bi-directional pin
T: Tri-level input

KEY SPECIFICATIONS

- CPU Output Jitter < 120ps
- ASIC Output Jitter < 150ps
- PCI Output Jitter < 250ps
- BUFOUT Output Jitter < 250ps
- ASIC-ASIC Skew < 250ps
- PCI-PCI Skew < 250ps
- BUFOUT-BUFOUT Skew < 100ps
- CPU-ASIC-PCI Skew < 250ps
- ASIC-PCI Skew < 250ps

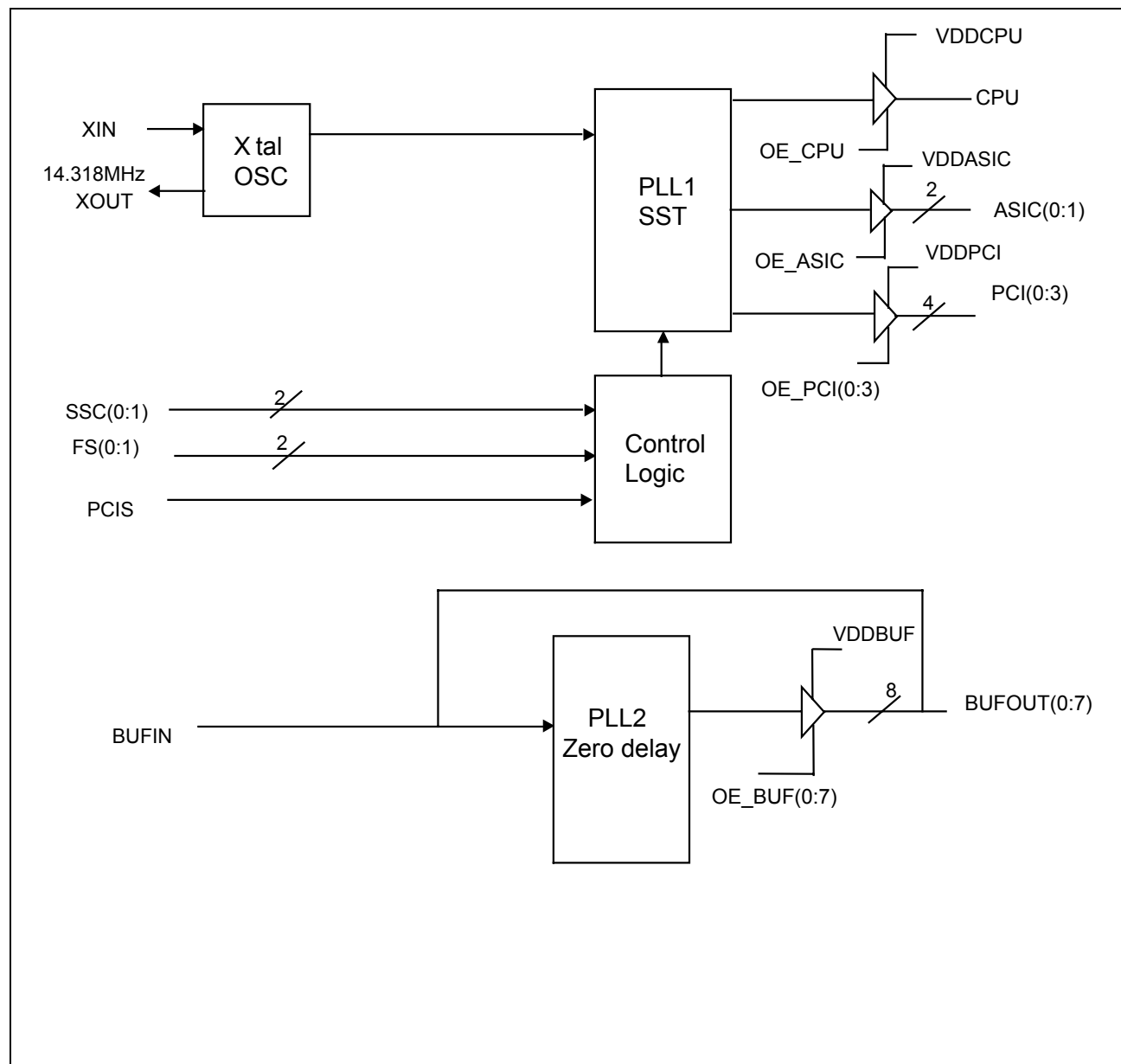
POWER GROUP

- VDDA, VSSA: XIN, XOUT
- VDDPCI, VSSPCI: PCI
- VDD1, VSS1: OE
- VDDBUF, VSSBUF: BUFOUT (0:7)
- VDDASIC, VSSASIC: ASIC (0:1)
- VDDCPU, VSSCPU: CPU

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Note: When CPU=133.3 MHz, it implements 130.9 MHz to meet Power PC clock AC Timing Specification; when CPU=150.0 MHz, it implements 148.1 MHz to meet Power PC clock AC Timing Specification; when CPU=166.6 MHz, it implements 162.6 MHz to meet Power PC clock AC Timing Specification.

BLOCK DIAGRAM



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PIN DESCRIPTIONS

Name	Number	Type	Description
VDD	1,6,13,16,29,36,39,41,45	P	Power supply
VSS	4,9,10,23,26,32,33,44,47	P	Ground
XIN/XOUT	2,3	B	Crystal input to be connected to a 14.31818MHz fundamental crystal (CL = 20pF, parallel resonant mode). Load capacitors have been integrated on the chip. No external load capacitor is required.
SSC (0:1)	11,12	I	Bi-level input for SST control (see Spread Spectrum selection table on p.4). '0' = 10kΩ pull down, '1' (default, internal pull up) = Not connected.
OE_CPU	25	I	Output enable pin for CPU output clock, '1' (default, internal pull up) = enable, '0' = disable
OE_ASIC	24	I	Output enable pin for ASIC output clock, '1' (default, internal pull up) = enable, '0' = disable
OE_PCI(0:3)	14,15,17,18,	I	Output enable pin for PCI output clocks, '1' (default, internal pull up) = enable, '0' = disable
OE_BUF(0:7)	19,20,21,22,	I	Output enable pin for BUFFER output clocks, '1' (default, internal pull up) = enable, '0' = disable
PCIS	5	I	The value of PCIS is latched in and used to select the PCI clock output (see frequency table on p.1). When PCIS = '0', PCI clock will be 33MHz, and 66MHz if PCIS = '1'. (default, internal pull up)
FS(0:1)	7,8	B	Tri-level frequency selection input pin, '0' = 10kΩ pull down, '1' = 10kΩ pull up, M (default) = not connected
BUFIN	40	I	Zero delay buffer clock input pin
BUFOUT(0:7)	27,28,30,31,34,35,37,38	O	Zero delay buffer output pin
PCI (0:3)	7,8,11,12	O	PCI clocks signal output pin
ASIC (0:1)	42,43	O	ASIC clocks signal output pins, will have the same frequency as CPU. (see frequency table on p.1).
PWRGD/RB	48	I	At power-up, this pin works as PWRGD. Before power supply stabilized, the input of PWRGD should be low, PLL loop and all output is disabled. After power supply stabilized, PWRGD change to high, FS(0:1), SSC(0:1) are latched and PLL loop is enabled, later on, the output buffers is enabled as well. After power-up, this pin works as Reset pin, when low, all the circuit will be reset.
CPU	46	O	CPU clock signal output pin. The CPU clock frequency is selected as per the frequency table on page 1, depending on the value of FS(0:1)

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FUNCTIONAL DESCRIPTION

Tri-level and two-level inputs

In order to reduce pin usage, the P210-02 uses tri-level input pins. These pins allow 3 levels for input selection: namely, 0 = Connect to GND, 1 = Connect to VDD, M = Do not connect. Thus, unlike the two-level selection pins, the tri-level input pins are in the "M" (mid) state when not connected. In order to connect a tri-level pin to a logical "zero", the pin must be connected to GND. Likewise, in order to connect to a logical "one", the pin must be connected to VDD.

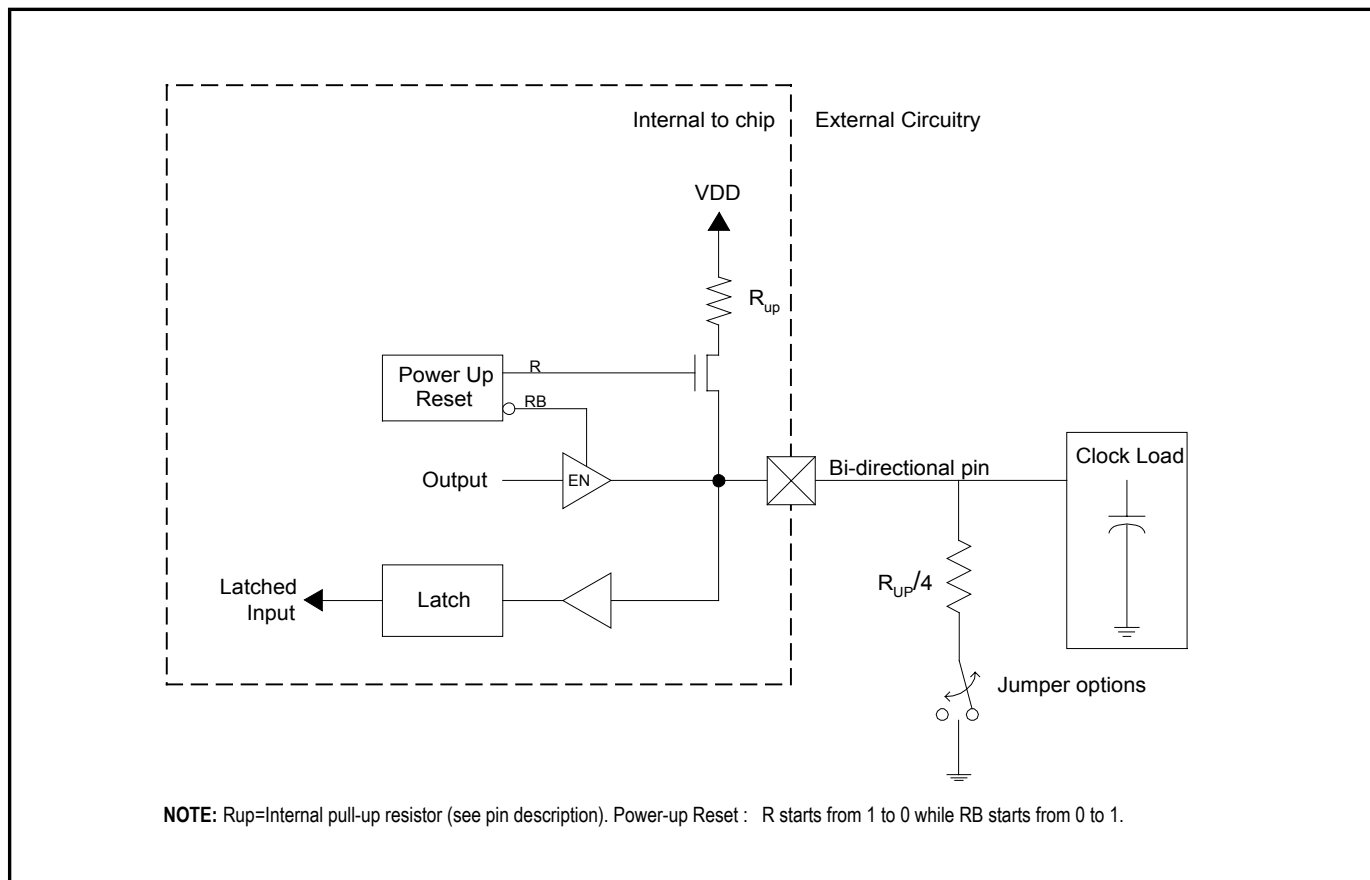
Connecting a bi-directional pin

The P210-01 also uses bi-directional pins. The same pin serves as input upon power-up, and as output as soon as the inputs have been latched. The value of the input is latched-in upon power-up. Depending on the pin (see pin description), the input can be tri-level or a standard two-level. Unlike unidirectional pins, bi-directional pins cannot be connected directly to GND or VDD in order to set the input to "0" or "1", since the pin also needs to serve as output. In the case of two level input pins, an internal pull-up resistor is present. This allows a default value to be set when no external pull down resistor is connected between the pin and GND (by definition, a tri-level input has a the default value of "M" (mid) if it is not connected). In order to connect a bi-directional pin to a non-default value, the input must be connected to GND or VDD through an external pull-down/pull-up resistor. **Note:** *when the output load presents a low impedance in comparison to the internal pull-up resistor, the internal pull-up resistor may not be sufficient to pull the input up to a logical "one", and an external pull-up resistor may be required.*

For bi-directional inputs, the external loading resistor between the pin and GND has to be sufficiently small (compared to the internal pull-up resistor) so that the pin voltage be pulled below 0.8V (logical "zero"). In order to avoid loading effects when the pin serves as output, the value of the external pull-down resistor should however be kept as large as possible. In general, it is recommended to use an external resistor of around one sixth to one quarter of the internal pull-up resistor (see Application Diagram). **Note:** *when the output is used to drive a load presenting an small resistance between the output pin and VDD, this resistance is in essence connected in parallel to the internal pull-up resistor. In such a case, the external pull-down resistor may have to be dimensioned smaller to guarantee that the pin voltage will be low enough achieve the desired logical "zero". This is particularly true when driving 74FXX TTL components.*

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APPLICATION DIAGRAM: BI-DIRECTIONAL PINS WITH INTERNAL PULL-UP



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Electrical Specifications

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	7	V
Input Voltage Range	V_I	-0.5	$V_{CC}+0.5$	V
Output Voltage Range	V_O	-0.5	$V_{CC}+0.5$	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		0	70	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

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2. AC Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency			14.31818		MHz
SST Modulation Sweep Rate			28		kHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
PLL Stability Time	Start when power supply reach 2.5V			4	ms
Reset Time	From reset signal applied to output buffer disabled	1	1		μs
Duty Cycle	At VDD/2	45	50	55	%
Max. Output Skew CPU and ASIC and PCI	Equal loading (20 pF) Equal frequency & drive strength Equal Power Supply		150	250	ps
Max. Output Skew ASIC and ASIC	Equal loading (20 pF) Equal frequency & drive strength Equal Power Supply		150	250	ps
Max. Output Skew BUFOUT and BUFOUT	Equal loading (20 pF) Equal frequency & drive strength Equal Power Supply			100	ps
Max. Output Skew ASIC and PCI	Equal loading (20 pF) Equal frequency & drive strength Equal Power Supply		150	250	ps
Max. Output Skew PCI and PCI	Equal loading (20 pF) Equal frequency & drive strength Equal Power Supply		150	250	ps
CPU Max. Cycle to Cycle Jitter	Long term + short term			120	ps
ASIC Max. Cycle to Cycle Jitter	Long term + short term			150	ps
PCI Max. Cycle to Cycle Jitter	Long term + short term			250	ps
BUFIN SSC Modulation Frequency		30		50	kHz
BUFIN SSC Clock Input Frequency Deviation		0.00		-1	%
BUFIN PLL Loop Bandwidth		2			MHz

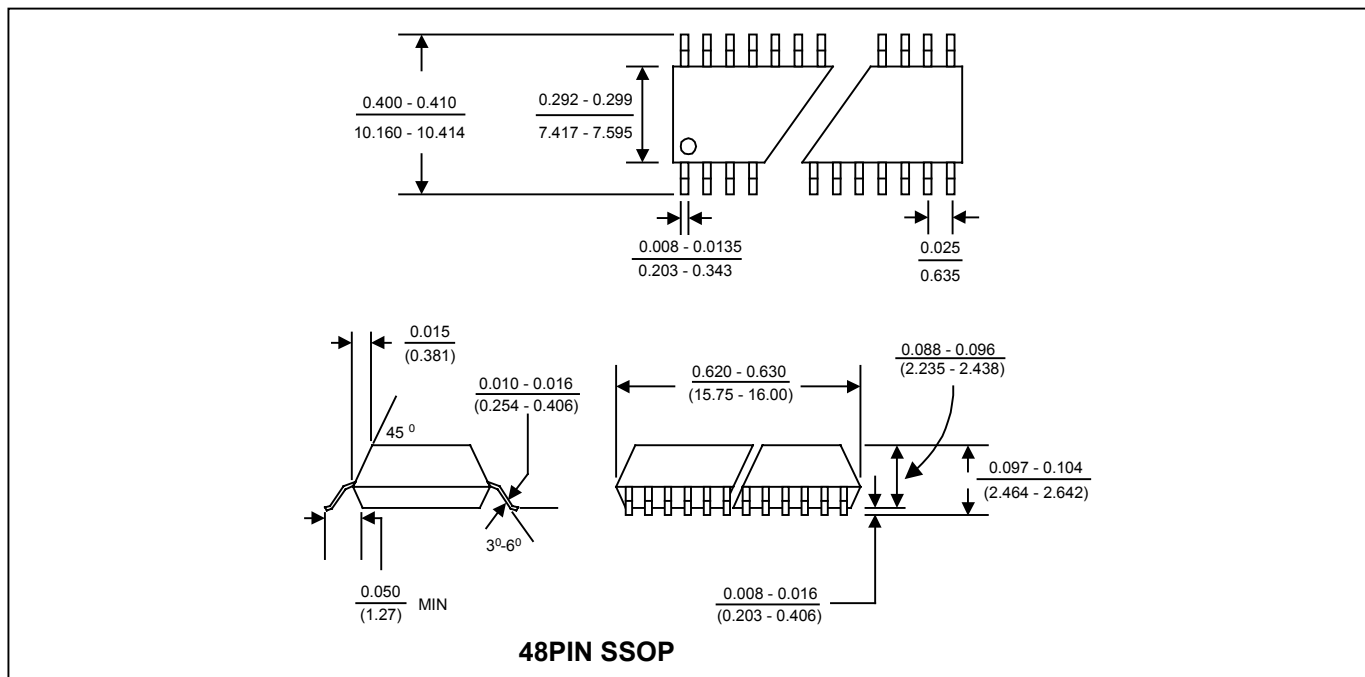
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3. DC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	VDDA VDDPCI VDDBUF VDD1	3.3V Nominal voltage	2.97		3.63	V
	VDDASIC VDDCPU	2.5V Nominal voltage	2.25		2.75	V
		3.3V Nominal voltage	2.97		3.63	
Input High Voltage	V _{IH}			VDD/2		V
Input Low Voltage	V _{IL}			VDD/2	VDD/2 - 1	V
Input High Voltage	V _{IH}	For all Tri-level input	VDD-0.5			V
Input Low Voltage	V _{IL}	For all Tri-level input			0.5	V
Input High Voltage	V _{IH}	For all normal input	2			V
Input Low Voltage	V _{IL}	For all normal input			0.8	V
Output High Voltage	V _{OH}	I _{OH} = -25mA VDD = 3.3V	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V _{OH}	I _{OH} = -8mA	VDD-0.4			V
Nominal Output Current	I _{out}		25			mA
Operating Supply Current	I _{DD}	No Load		35		mA
Short-circuit Current	I _s			±100		mA

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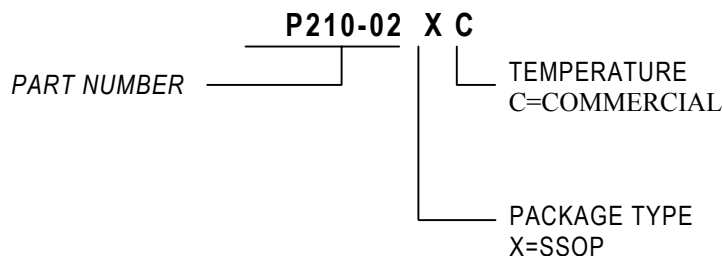
PACKAGE INFORMATION



ORDERING INFORMATION

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
P210-02XC	P210-02XC	SSOP-Tube
P210-02XC-R	P210-02XC	SSOP - Tape and Reel

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