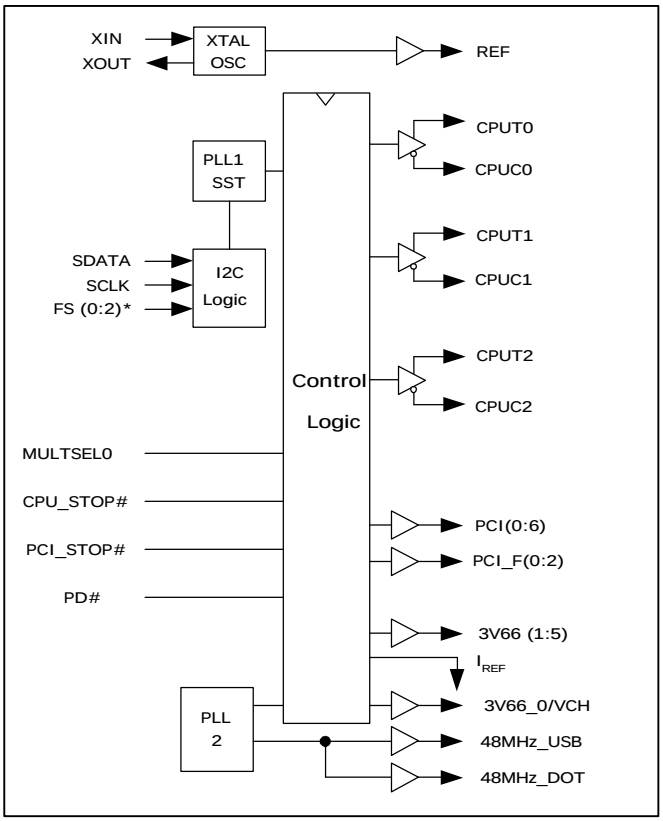
PLL207-151

Frequency Generator with 200MHz Differential CPU Clocks

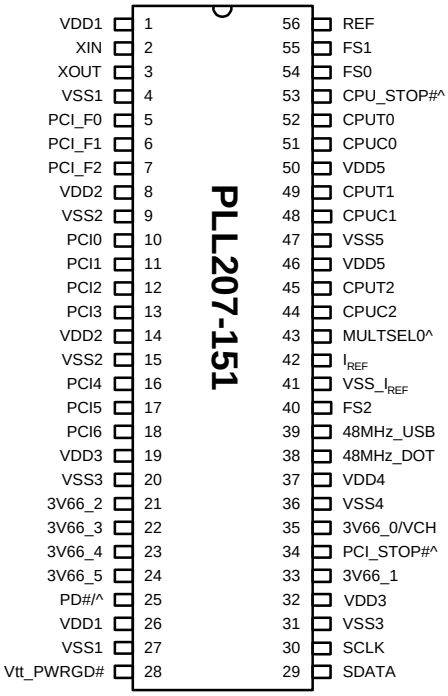
FEATURES

- Supports 3 pair of differential CPU clocks for INTEL Brookdale chipsets.
- Programmable Spread Spectrum Modulation from ±0.1% to ±1.5% with minimum step size of ±0.012%. Selectable either center or down.
- Selectable Spread Spectrum modulation profile.
- AccuSkew™, Programmable Precision skew tuning channel with maximum ±5% precision over the variation of temperature, process and voltage. Finest step starts with 80ps.
- AccuDrive™ Programmable Output Buffer drive strength with minimum 6mA per step.
- 7 PCI, 3 PCI_F, 1 USB, 1 DOT, 1 REF, 5 3V66
- One 3V66/VCH (3.3V) at 66.66MHz or 48MHz.
- Power management control to stop CPU, PCI.
- Support 2-wire I2C serial bus interface.
- Single byte micro-step linear Frequency programming via I2C with smooth switching.
- Available in 300 mil 56 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: ^: Pull up (100kΩ), #: Active low,
*: Bi-directional latched at power-up

POWER GROUP

- VDD1, VSS1: REF, XIN, XOUT, PLL ANALOG
- VDD2, VSS2: PCI
- VDD3, VSS3: 3V66
- VDD4, VSS4: 48MHz
- VDD5, VSS5: CPUT & CPUC

KEY SPECIFICATIONS

- CPU Output Jitter < 200ps
- 3V66 Output Jitter < 250ps
- CPU Output Skew < 150 ps

PIN DESCRIPTIONS

Name	Number	Type	Description
VDD	1,8,14,19,26, 32,37,46,50	P	3.3V Power Supply.
XIN	2	I	14.318Mhz crystal input to be connected to one end of the crystal.
XOUT	3	O	14.318Mhz crystal output.
PCI_F(0:2)	5,6,7	O	PCI clock optionally not affected by PCI_STOP (see I2C Byte 3). PCI_F will all be left free running if I2C Byte 3 bit [3:5] = 0, but will be stopped if I2C Byte 3 bit [3:5] = 1. They have 20 ohms on-chip series resistor.
PCI(0:6)	10,11,12,13, 16,17,18	O	PCI clock outputs. They have 20 ohms on-chip series resistor.
3V66(1:5)	21,22,23,24, 33	O	66MHz reference clock from internal VCO. It has a 20 ohms on-chip series resistor.
PD#	25	I	Power Down Control input. When low, Power Down will disable all clock outputs including internal VCO and crystal clock. This pin has a 100kΩ internal pull-up.
Vtt_PWRGD#	28	I	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS (0:2) and MULTSEL0 inputs are valid and ready to be sampled (active low).
SDATA	29	B	Serial data inputs for serial interface port.
SCLK	30	I	
PCI_STOP#	34	I	Halts PCI clocks when low (except PCI_F which are free running). This pin has a 100kΩ internal pull-up.
3V66_0/VCH	35	O	3.3V output selectable through I2C to be 66MHz from internal VCO or 48MHz (non-Speed Spectrum Controlled). It has a 20 ohms on-chip series resistor.
48MHz_DOT	38	O	48MHz output for DOT. It has a 20 ohms on-chip series resistor.
48MHz_USB	39	O	48MHz output for USB. It has a 20 ohms on-chip series resistor.
FS2	40	I	Frequency select pins.
I_{REF}	42	O	This pin establishes the reference current for the CPU pairs, it requires a fixed precision resistor tied to ground in order to establish the appropriate current.
MULTSEL0	43	I	This input is selecting the current multiplier for CPU outputs. This pin has a 100kΩ internal pull-up.
CPUC(0:2)	44,48,51	O	Complementary clock of differential pair of CPU outputs.
CPUT(0:2)	45,49,52	O	True clock of differential pair of CPU outputs.
CPU_STOP	53	I	Halts CPU clocks when input low. This pin has a 100kΩ internal pull-up.

PIN DESCRIPTIONS (CONTINUED)

Name	Number	Type	Description
FS(0:1)	54,55	I	Frequency select pins.
REF	56	O	14.318MHz reference clock. It has a 20 ohms on-chip series resistor.
VSS_I_{REF}	41	P	Current reference programming input for CPU buffers. This pin is returned to device VSS.
VSS	4,9,15,20,27, 31,36,47	P	0.0V Power Supply.

FEQUENCY (MHz) SELECTION TABLE

FS2	FS1	FS0	CPU	3V66	PCI_F, PCI	Spread Spectrum modulation rate
0	0	0	66.66	66.66	33.3	0 to –0.5% down spread
0	0	1	100	66.66	33.3	0 to –0.5% down spread
0	1	0	200	66.66	33.3	0 to –0.5% down spread
0	1	1	133.3	66.66	33.3	0 to –0.5% down spread
1	0	0	66.66	66.66	33.3	0 to –0.75% down spread
1	0	1	100	66.66	33.3	0 to –0.75% down spread
1	1	0	200	66.66	33.3	0 to –0.75% down spread
1	1	1	133.3	66.66	33.3	0 to –0.75% down spread
Mid	0	0	Tristate	Tristate	Tristate	N/A
Mid	0	1	TCLK/2	TCLK/4	TCLK/8	N/A
Mid	1	0	Reserved	Reserved	Reserved	N/A
Mid	1	1	Reserved	Reserved	Reserved	N/A

POWER MANAGEMENT CONIGURATION

PD#	CPU_STOP#	PCI_STOP#	CPUT	CPUC	3V66	PCI_F	PCI	USB/DOT	PLL/OSC
0	X	X	IREF*2	FLOAT	LOW	LOW	LOW	LOW	OFF
1	0	0	IREF*2	FLOAT	ON	ON	ON	ON	ON
1	0	1	IREF*2	FLOAT	ON	ON	ON	ON	ON
1	1	0	ON	ON	ON	ON	ON	ON	ON
1	1	1	ON	ON	ON	ON	ON	ON	ON

HOST SWING SELECT FUNCTIONS

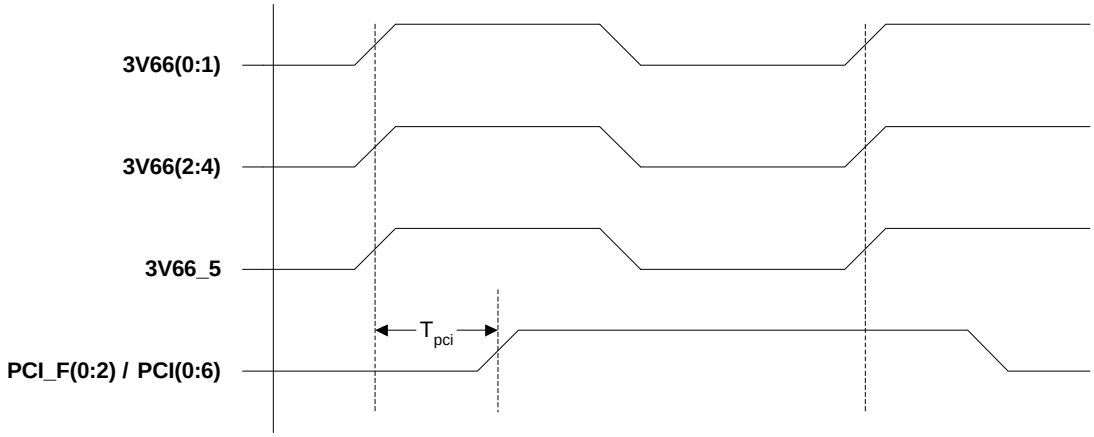
MULT_SEL0	Board target trace (Z)	Reference R (Rr); IREF = VDD/(3*Rr)	Output Current	Voh @ Z
0	50 Ω	Rr = 221Ω (1%); IREF = 5.00mA	Ioh = 4 x IREF	1.0V @ 50
1	50 Ω	Rr = 475Ω (1%); IREF = 2.32mA	Ioh = 6 x IREF	0.7V @ 50

MAXIMUM ALLOWED CURRENT

Conditions	Max. 3.3 supply consumption VDD = 3.465V All static inputs = VDD or GND
Powerdown Mode (PD# = 0)	25mA @ Iref = 2.32 mA, 45mA @ Iref = 5.0mA
Full Active	280 mA

TIMING DIAGRAMS & PHASE RELATIONSHIP

Figure: **3V66 & PCI Phase Relationship (Un-Buffered Mode)**



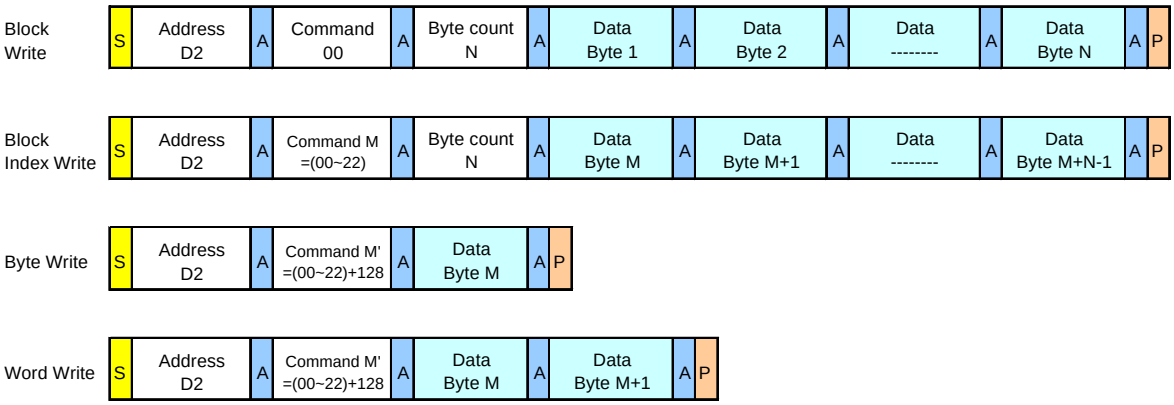
Group Skews at Common Transition Edges: (Un-Buffered Mode)

Group	Symbols	Description	Min	Max	Units
3V66	3V66	3V66(0:5) pin-to-pin skew	0	500	ps
PCI	PCI	PCI_F(0:2) and PCI (0:6) pin-to-pin skew	0	500	ps
3V66 to PCI	T PCI	3V66(0:5) leads 33MHz PCI	1.5	3.5	ns

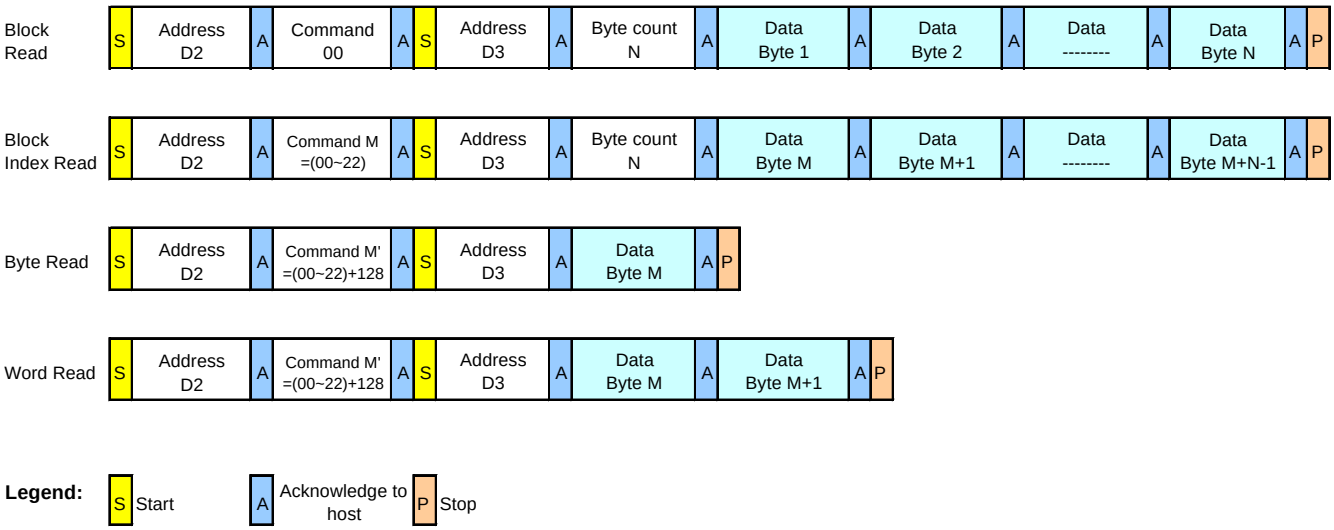
I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and read back functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	This serial interface is designed to allow multiple protocols to write and read from the controller. It includes Block Read/Write, Block Index Read/Write, Byte Read/Write and Word Read/Write. In general, the bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).							

WRITE MODE



READ MODE



Legend: S Start | A Acknowledge to host | P Stop

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	0 = OFF, 1 = Spread Spectrum Enable
Bit 6	-	0	CPU PD mode: 0=CPU drive when PD, 1=non drive
Bit 5	-	0	VCH Select 66Mhz/48Mhz. 0=66Mhz, 1=48Mhz
Bit 4	-	X	Reflects the value of CPU_STOP#.
Bit 3	34	X	Reflects the value of PCI_STOP#.
Bit 2	40	X	Power-up latched FS2 value (Read only)
Bit 1	55	X	Power-up latched FS1 value (Read only)
Bit 0	54	X	Power-up latched FS0 value (Read only)

2. BYTE 1: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	43	X	Reflects current MULTSEL0 value (Read only)
Bit 6	-	0	CPU STP mode: 0=CPU drive when CPU STP, 1=non drive, CPU=STPD
Bit 5	-	0	Allow control of CPUCLKT2/C2 with assertion of CPU_STOP# 0=not free running, 1=free running
Bit 4	-	0	Allow control of CPUCLKT1/C1 with assertion of CPU_STOP# 0=not free running, 1=free running
Bit 3	-	0	Allow control of CPUCLKT0/C0 with assertion of CPU_STOP# 0=not free running, 1=free running
Bit 2	45,44	1	Enables/disables CPUT2, CPUC2. When disabled, defaults to CPUT2 = 1 CPUC2 = 0.
Bit 1	49,48	1	Enables/disables CPUT1, CPUC1. When disabled, defaults to CPUT1 = 1 CPUC1 = 0.
Bit 0	52,51	1	Enables/disables CPUT0, CPUC0. When disabled, defaults to CPUT0 = 1 CPUC0 = 0.

3. BYTE 2: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Reserved
Bit 6	18	1	PCI6 (1=Active 0=Inactive)
Bit 5	17	1	PCI5 (1=Active 0=Inactive)
Bit 4	16	1	PCI4 (1=Active 0=Inactive)
Bit 3	13	1	PCI3 (1=Active 0=Inactive)
Bit 2	12	1	PCI2 (1=Active 0=Inactive)
Bit 1	11	1	PCI1 (1=Active 0=Inactive)
Bit 0	10	1	PCI0 (1=Active 0=Inactive)

4. BYTE 3: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	38	1	48MHz_DOT (1=Active 0=Inactive)
Bit 6	39	1	48MHz_USB (1=Active 0=Inactive)
Bit 5	7	0	Allows control of PCI_F2 output after assertion of PCI_STOP#. 0 = Free running, 1 = Not free running.
Bit 4	6	0	Allows control of PCI_F1 output after assertion of PCI_STOP#. 0 = Free running, 1 = Not free running.
Bit 3	5	0	Allows control of PCI_F0 output after assertion of PCI_STOP#. 0 = Free running, 1 = Not free running.
Bit 2	7	1	PCI_F2 (1=Active 0=Inactive)
Bit 1	6	1	PCI_F1 (1=Active 0=Inactive)
Bit 0	5	1	PCI_F0 (1=Active 0=Inactive)

5. BYTE 4: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	SST Profile	1	0= linear, 1= non-linear
Bit 6	Accu-SST	1	Accu-SST programming Enable: 0= via I2C Byte 7, 1= via ROM setting
Bit 5	33	1	3V66_1 (1=Active 0=Inactive)
Bit 4	35	1	3V66_0/VCH (1=Active 0=Inactive)
Bit 3	24	1	3V66_5 (1=Active 0=Inactive)
Bit 2	23	1	3V66_4 (1=Active 0=Inactive)
Bit 1	22	1	3V66_3 (1=Active 0=Inactive)
Bit 0	21	1	3V66_2 (1=Active 0=Inactive)

6. BYTE 5: Linear Programming Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Linear programming sign bit (0 is "+", 1 is "–")
Bit 6	-	0	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0	Linear programming magnitude bit 5
Bit 4	-	0	Linear programming magnitude bit 4
Bit 3	-	0	Linear programming magnitude bit 3
Bit 2	-	0	Linear programming magnitude bit 2
Bit 1	-	0	Linear programming magnitude bit 1
Bit 0	-	0	Linear programming magnitude bit 0 (LSB)

7. BYTE 6: Vendor ID and Revision ID Register

Bit	Pin#	Default	Description
Bit 7	-	0	Revision ID Bit 3 (read only)
Bit 6	-	0	Revision ID Bit 2 (read only)
Bit 5	-	0	Revision ID Bit 1 (read only)
Bit 4	-	0	Revision ID Bit 0 (read only)
Bit 3	-	0	Vendor ID Bit 3 (read only)
Bit 2	-	0	Vendor ID Bit 2 (read only)
Bit 1	-	1	Vendor ID Bit 1 (read only)
Bit 0	-	1	Vendor ID Bit 0 (read only)

8. BYTE 7: Accu-Spread Spectrum Modulation Amplitude Programming Register:

Bit	NAME	Default	Description
Bit 7	-	1	Spread Spectrum mode selection. 1=Center Spread, 0= Down Spread
Bit 6	SST6	1	1. Center Spread: SST<6:0> = Modulation rate * N /7 2. Down Spread: SST<6:0> = Modulation rate * N /14
Bit 5	SST5	1	
Bit 4	SST4	1	
Bit 3	SST3	1	
Bit 2	SST2	1	
Bit 1	SST1	1	
Bit 0	SST0	1	

9. BYTE 8: SKEW Control Register (1=Enable, 0=Disable)

Bit	Name	Default	Description	
Bit 7	SKEW ENABLE	0	Enable Accu-Skew programming. 1=enable, 0=disable	
Bit 6	-	0	Skew calibration: 1=enable, 0=disable	
Bit 5	SKEW CPU0	0	**Bit [5:3]** 111 +320ps 110 +240ps 101 +160ps 100 +80ps **011 Default** 010 –80ps 001 –160ps 000 –240ps	These three bits will adjust timing of CPU0 signals (CPUT0/CPUC0) either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
Bit 4		1		
Bit 3		1		
Bit 2	SKEW CPU1	0	**Bit [2:0]** 111 +320ps 110 +240ps 101 +160ps 100 +80ps **011 Default** 010 –80ps 001 –160ps 000 –240ps	These three bits will adjust timing of CPU1 signals (CPUT1/CPUC1) either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
Bit 1		1		
Bit 0		1		

10. BYTE 9: SKEW Control Register (1=Enable, 0=Disable)

Bit	Name	Default	Description	
Bit 7	-	0	Reserved	
Bit 6	-	0	Reserved	
Bit 5	SKEW CPU2	0	**Bit [5:3]** 111 +320ps 110 +240ps 101 +160ps 100 +80ps **011 Default** 010 –80ps 001 –160ps 000 –240ps	These three bits will adjust timing of CPU2 signals (CPUT2/CPUC2) either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
Bit 4		1		
Bit 3		1		
Bit 2	SKEW 3V66	0	**Bit [2:0]** 111 +640ps 110 +480ps 101 +320ps 100 +160ps **011 Default** 010 –160ps 001 –320ps 000 –480ps	These three bits will adjust timing of 3V66 signals (3V66[0:5]) either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
Bit 1		1		
Bit 0		1		

11. BYTE 10: Control Register (1=Enable, 0=Disable)

Bit	Name	Default	Description	
Bit 7	-	0	Reserved	
Bit 6	-	0	Reserved	
Bit 5	SKEW PCI	0	**Bit [5:3]** 111 +640ps 110 +480ps 101 +320ps 100 +160ps **011 Default** 010 –160ps 001 –320ps 000 –480ps	These three bits will adjust timing of all PCI signals (PCI_F[0:2], PCI[0:6]) either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
Bit 4		1		
Bit 3		1		
Bit 2	PCI_F Strength	0	**Bit [2:0]** 111 +50% 110 +38% 101 +25% 100 +13% **011 Default** 010 –13% 001 –25% 000 –38%	These three bits will program drive strength for PCI_F[0:2] output clocks either increase or decrease from –38% to +50%.
Bit 1		1		
Bit 0		1		

12. BYTE 11: Buffer Strength Control Register (1=Enable, 0=Disable)

Bit	Name	Default	Description	
Bit 7	-	0	Reserved	
Bit 6	-	0	Reserved	
Bit 5	PCI Strength	0	**Bit [2:0]** 111 +50% 110 +38% 101 +25% 100 +13% **011 Default** 010 –13% 001 –25% 000 –38%	These three bits will program drive strength for PCI[0:6] output clocks either increase or decrease from –38% to +50%.
Bit 4		1		
Bit 3		1		
Bit 2	3V66 Strength	0	**Bit [2:0]** 111 +40% 110 +30% 101 +20% 100 +10% **011 Default** 010 –10% 001 –20% 000 –30%	These three bits will program drive strength for 3V66[0:5] output clocks either increase or decrease from –30% to +40%.
Bit 1		1		
Bit 0		1		

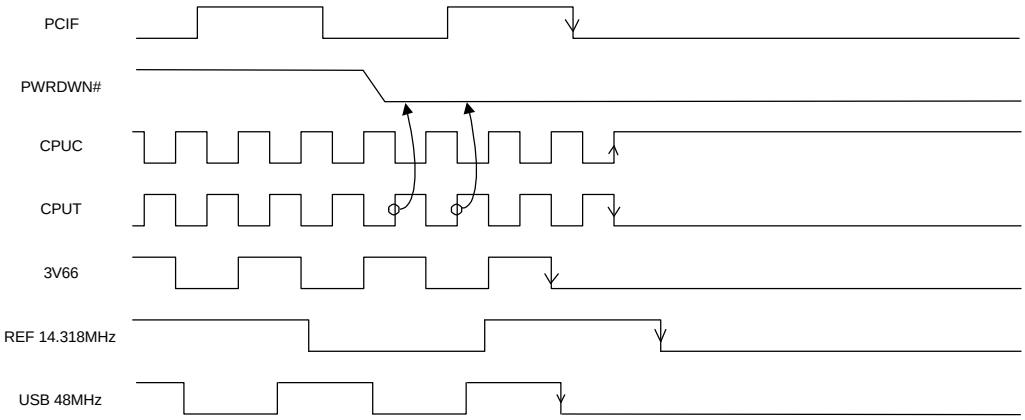
13. BYTE 12: Buffer Strength Control Register (1=Enable, 0=Disable)

Bit	Name	Default	Description	
Bit 7	-	0	Reserved	
Bit 6	-	0	Reserved	
Bit 5	USB Strength	0	**Bit [2:0]** 111 +40% 110 +30% 101 +20% 100 +10% **011 Default** 010 –10% 001 –20% 000 –30%	These three bits will program drive strength for 48MHz_USB, 48MHz_DOT output clocks either increase or decrease from –30% to +40%.
Bit 4		1		
Bit 3		1		
Bit 2	REF Strength	0	**Bit [2:0]** 111 +50% 110 +38% 101 +25% 100 +13% **011 Default** 010 –13% 001 –25% 000 –38%	These three bits will program drive strength for REF output clocks either increase or decrease from –38% to +50%.
Bit 1		1		
Bit 0		1		

PD# ASSERTION (Transition from Logic "1" to Logic "0")

1. When Power-Down (PD#) is sampled low by two consecutive rising edges of CPUT clock, then all clock outputs must be held low on their next high to low transition (except CPUC which must be driven high with a value of 2 x IREF).
2. After the clocks have all been stopped, the internal PLL stages and the Crystal oscillator will all be driven to a low power stopped condition.

Figure: **PD# assertion (Transition from Logic '1' to Logic '0')**



PD# DE-ASSERTION (Transition from Topic "0" to Topic "1")

1. Power-Down (PD#) pin is taken from Low to High transition to return to normal running operation.
2. The Crystal Oscillator and the two PLL stages are released from PD to start-up to normal operation.
3. The CPU PLL clocks (differential CPU outputs and the driven 3V66_(0:5) clocks are then operating.
4. After the PCI clocks are released.
5. Following the 48 MHz (DOT and USB clocks) and the REF (14.318MHz) clocks are released.

Figure: **PD# de-assertion (Transition from Logic '0' to Logic '1')**

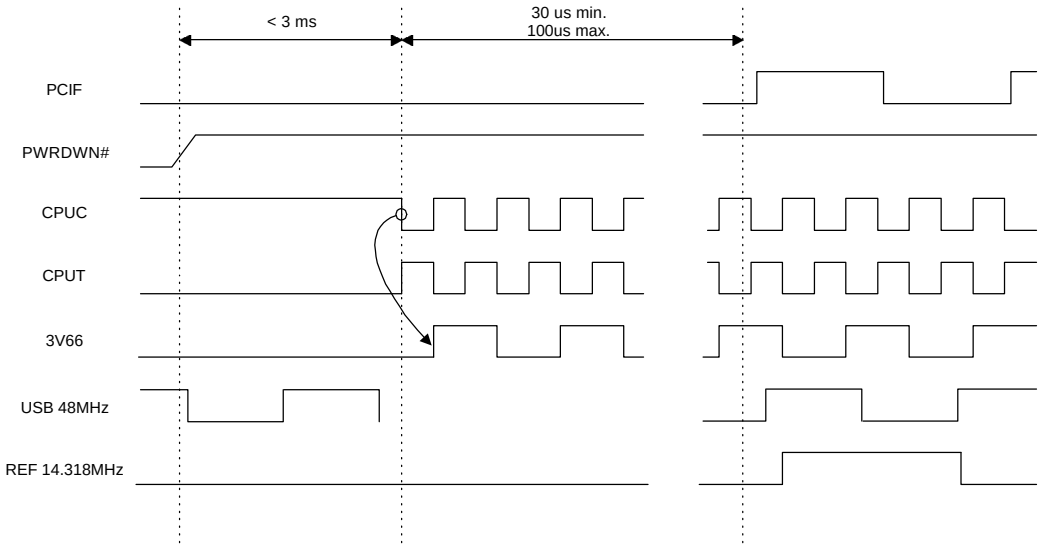


Figure: **Assertion CPU_Stop# Waveforms**

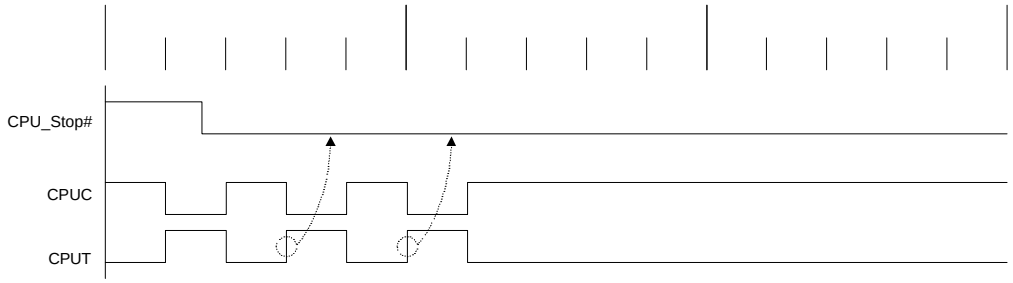
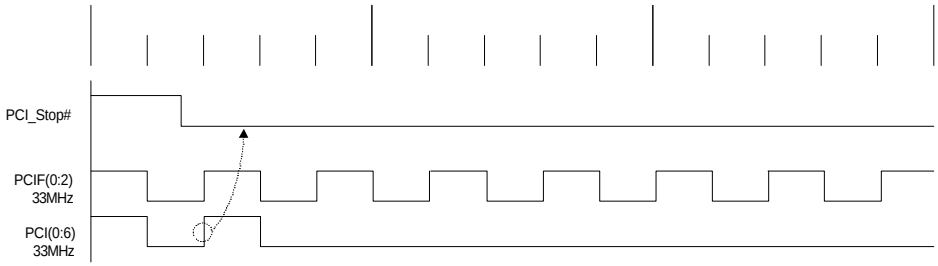


Figure: **Assertion PCI_Stop# Waveforms**



Note: PCIF left free-running if so selected by I2C.

PROGRAMMING OF CPU FREQUENCY USING SMART-BYTE:

To simplify traditional loop counter setting, the PLL207-151 device incorporates SMART-BYTE ™ technology with a single byte programming via I2C. Detail of PLL207-151's dual mode frequency programming method is described below:

1. **ROM-table Frequency Programming:**

   The pre-defined 8 frequencies found in Frequency table can be accessed through 2 external jumpers.

2. **Micro-step Linear Frequency Programming:**

   CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency changes. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha * M$$

Where:
1. M is magnitude factor defined in I2C Byte 5.bit (0:6)
2. ± (sign bit) of M is defined in I2C Byte5.bit 7
3. α is a constant equal to 0.9/(CPUDivider) ranging from 0.11~0.45.

FREQUENCY PROGRAMMING EXAMPLE:

1. **Procedures to program target CPU frequency to 110 Mhz:**

   A. Locate the closest CPU frequency from Frequency-ROM table: 108
   B. α = 0.22
   C. Solve M (Linear Magnitude factor) in integer:

$$M = (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha$$
$$= (110 - 108) / 0.22$$
$$= 9$$

   D. Program I2C register:

7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	1
Sign	M6	M5	M4	M3	M2	M1	M0

Setting of M = +9 in I2C.BYTE57

F_{CPU} = 108 + (0.22) * 9 = 109.98 (% of frequency increased vs. ROM Table = 1.83 %)
F_{PCI} = 36 * (1 + 1.83 %) = 36.66

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	4.6	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input Leakage Current	I_{IL}	0 < V_{in} < VDD	-5		5	uA
Output High Voltage	V_{OH}	I_{oh} = -1 mA	2.4			V
Output Low Voltage	V_{OL}	I_{ol} = 1 mA			0.4	V
Input pin Capacitance	C_{in}				5	pF
Output pin Capacitance	C_{out}				6	pF

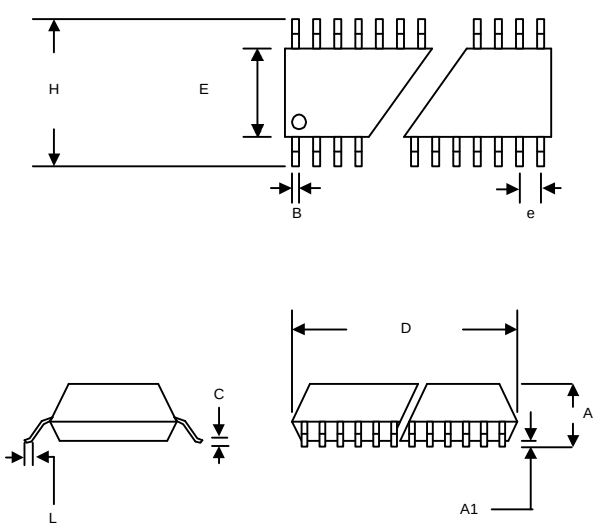
3. AC Electrical Specifications

PARAMETERS	SYMBOL	OUTPUTS	CONDITION	MIN.	TYP.	MAX.	UNITS
Rise Time	T_r	CPU	@1.0V	300		600	ps
		3V66, 66MHz, PCI	Measured @ 0.4V ~ 2.4V, C_L=20pf, 3.3V±5%	0.5		2.0	ns
Fall Time	T_f	CPU	@1.0V	300		600	ps
		3V66, 66MHz, PCI	Measured @ 0.4V ~ 2.4V, C_L=20pf, 3.3V±5%	0.5		2.0	ns

3. AC Electrical Specifications (Continued)

PARAMETERS	SYMBOL	OUTPUTS	CONDITION	MIN.	TYP.	MAX.	UNITS
Cycle to Cycle jitter	$T_{cyc-cyc}$	CPU	@1.5V			200	ps
		3V66, 66MHz	@1.5V			250	
		PCI	@1.5V			250	
		48MHz, DOT, USB	@1.5V			350	
Skew	T_{skew}	CPU to CPU	V_T = 50%			150	ps
		3V66 to 3V66	Un-buffered mode @1.5V			500	
		PCI and PCI_F				500	
Duty Cycle	D_T	CPU, PCI, REF, 48MHz, 3V66	V_T = 50%	45	51	55	%
Rising edge Rate	R_r	48MHz_USB, DOT, REF	Measured @ 0.4V ~ 2.4V	1.0		2.0	
		3V66, 66MHz, PCI	Measured @ 0.4V ~ 2.4V	1.0		4.0	V/ns
Falling edge Rate	R_f	48MHz_USB, DOT, REF	Measured @ 0.4V ~ 2.4V	1.0		2.0	
		3V66, 66MHz, PCI	Measured @ 0.4V ~ 2.4V	1.0		4.0	
Long Term jitter	$T_{L-jitter}$	48MHz_USB	125us period jitter (8kHz modulation Amplitude)			6.0	ns
		48MHz_DOT	10us period jitter (100kHz modulation Amplitude)			2.0	
Output enable delay	Tpzl,Tpzh	All outputs		1.0		10.0	ns
Output disable delay	Tplz,Tpzh	All outputs		1.0		10.0	
Stabilization time	Ts	All outputs				3	ms

PACKAGE INFORMATION



56PIN SSOP

Package	SSOP (QSOP) 300mil			
Pins#	56			
Unit	mm		inches	
	min	max	min	max
A	2.41	2.79	0.095	0.110
A1	0.203	0.406	0.008	0.016
B	0.203	0.343	0.008	0.0135
C	0.127	0.254	0.005	0.010
D	18.29	18.54	0.720	0.730
E	7.39	7.60	0.291	0.299
H	10.03	10.67	0.395	0.420
e	0.635BSC		0.025BSC	
L	0.508	1.016	0.020	0.040

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL207-151 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP