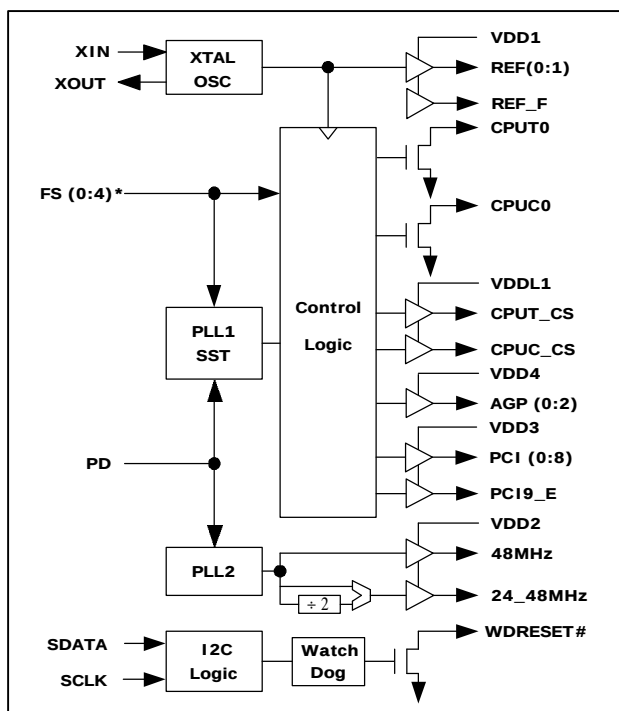


Programmable Clock Generator for VIA KT-266 Chipset

FEATURES

- Generates all clock frequencies for VIA KT266 chipset.
- Support one pair of differential CPU clocks, one pair of differential push-pull CPU clocks, 3 AGP and 10 PCI.
- Enhanced PCI Output Drive selectable by I2C.
- One 48MHz clock and 24_48MHz clock via I2C.
- Three 14.318MHz reference clocks.
- Power management control to stop CPU, PCI, REF, 24_48MHz, 48MHz and AGP clocks.
- Supports 2-wire I2C serial bus interface with readback.
- Single byte micro-step linear Frequency Programming via I2C with glitch free smooth switching.
- Built-in programmable watchdog timer up to 63 seconds with 1-second interval. It will generate a low reset output when timer expired.
- Spread Spectrum $\pm 0.25\%$ center, $\pm 0.5\%$ center, $\pm 0.75\%$ center, and 0 to -0.5% downspread.
- 50% duty cycle with low jitter.
- Available in 300 mil 48 Pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION

VDD1	1	48	REF0/FS0*^
GND	2	47	REF1/FS1*^
XIN	3	46	REF_F
XOUT	4	45	N/C
VDD2	5	44	AGP_STOP#^
48MHz/FS2*^	6	43	GND
24_48MHz/FS3* ^	7	42	CPU0
GND	8	41	CPUC0
FS4*^/PCI_F	9	40	VDDL1
SEL24_48#/PCI0	10	39	CPUT_CS
PCI1	11	38	CPUC_CS
GND	12	37	GND
PCI2	13	36	CPU_STOP#^
PCI3	14	35	PCI_STOP#^
VDD3	15	34	PD#^
PCI4	16	33	VDDL2
PCI5	17	32	GND
PCI6	18	31	SDATA
GND	19	30	SCLK
PCI7	20	29	GND
PCI8	21	28	AGP2
PCI9_E/SELPCI9_E*^	22	27	AGP1
VDD3	23	26	AGP0
WDRESET#^	24	25	VDD4

Note: ^: 100k internal Pull up v: 100k internal Pull down
#: Active low *: Bi-directional up latched at power-up

POWER GROUP

- VDD1: REF(0:1), REF_F, XIN, XOUT
- VDD2: 48MHz or 24_48MHz
- VDD3: PCI(0:8), PCI9_E
- VDD4: AGP(0:2)
- VDDL1: CPUT0, CPUC0, CPUT_CS, CPUC_CS
- VDDL2: PLL Core

KEY SPECIFICATIONS

- CPU Cycle to Cycle jitter: 250ps.
- PCI Cycle to Cycle jitter: 500ps.
- PCI to PCI skew: 500ps.
- CPU to CPU skew: 175ps.
- AGP to AGP skew: 250ps.

Programmable Clock Generator for VIA KT-266 Chipset

PIN DESCRIPTION

Name	Number	Type	Description
VDD1	1	P	Power supply for REF(0:1), REF_F and crystal oscillator.
VDD2	5	P	Power supply for 48MHz or 24_48MHz.
VDD3	15,23	P	Power supply for PCI(0:8), PCI9_E.
VDD4	25	P	Power supply for AGP(0:2).
VDDL1	40	P	Power supply for CPUT0, CPUC0, CPUT_CS and CPUC_CS.
VDDL2	33	P	Power supply for PLL CORE.
GND	2,8,12,19,29, 32,37,43	P	Ground.
XIN	3	I	14.318MHz crystal input to be connected to one end of the crystal.
XOUT	4	O	14.318MHz crystal output.
PD#	34	I	PD is Asynchronous active low input used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped.
PCI_STOP#	35	I	When input is Low, it will stop PCI(0:8) and PCI9_E. The enable of the watchdog timer masks the PCI_STOP action.
CPU_STOP	36	I	When input is Low, it will disable CPUT0, CPUC0, CPUT_CS and CPUC_CS.
AGP_STOP	44	I	When input is Low, it will stop AGP(0:2).
N/C	45		Not connected
PCI(0:8)	10,11,13,14, 16,17,18,20,21	O	PCI clocks with frequencies defined by Frequency Table. These pins will be LOW when PCI_STOP is LOW.
SEL24_48#/PCI0	10	B	PCI clock output. This pin also serves as the select 24MHz (when High) or 48MHz (when Low) for pin7.
PCI9_E/SELPCI9_E	22	B	At power up, this pin is an input pin and will determine the operating frequency of PCI9_E output. After input sampling, this pin will generate PCI output clock. If SELPCI9_E=1, PCI9_E will arrive 2 ns earlier than other PCI clocks, if SELPCI9_E=0, PCI9_E will be normal PCI output like other PCI clock outputs.

Programmable Clock Generator for VIA KT-266 Chipset

PIN DESCRIPTIONS (continued)

Name	Number	Type	Description
FS4*/PCI_F	9	B	Free running PCI clock. This pin also serves as the select strap to determine device operating frequency.
CPUT0	42	O	True clock of differential pair open drain CPU outputs. This output will be disabled when CPU_STOP is low.
CPUC0	41	O	Complementary clock of differential pair open drain CPU outputs. This output will be disabled when CPU_STOP is low.
CPUT_CS, CPUC_CS	39,38	O	Differential CPU clock outputs for the chipset. They are push-pull outputs. These outputs will be disabled when CPU_STOP is low.
AGP(0:2)	26,27,28	O	AGP clocks outputs defined as 2x PCI.
SDATA	31	B	Serial data input for serial interface port.
SCLK	30	I	
REF0/FS0* REF1/FS1* 48MHz/FS2* 24_48MHz/FS3* FS4*/PCI_F	48,47,6,7,9	B	At power up, these pins are input pins. After input sampling, these pins will generate output clocks. FS(0:4) have internal pull-up resistor.
WDRESET#	24	I	This pin is an open drain output. Will be Low at watchdog timer expiration.
REF(0:1),REF_F	48,47,46	O	3.3V 14.318MHz clock output.

Programmable Clock Generator for VIA KT-266 Chipset

POWER MANAGEMENT

CPU_STOP	PCI_STOP	CPUT_CS	CPUC_CS	CPUT0	CPUC0	PCI	PCI_F	XTAL,VCO
1	1	Running	Running	Running	Running	Running	Running	Running
0	1	Stopped Low	Stopped High	Stopped High	Stopped Low	Running	Running	Running
1	0	Running	Running	Running	Running	Stopped Low	Running	Running

FREQUENCY (MHz) SELECTION TABLE

FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	Spread Spectrum
0	0	0	0	0	156	78	39	± 0.25%
0	0	0	0	1	154	77	38.5	± 0.25%
0	0	0	1	0	152	76	38	± 0.25%
0	0	0	1	1	147	73.5	36.8	± 0.25%
0	0	1	0	0	144	72	36	± 0.25%
0	0	1	0	1	142	71	35.5	± 0.25%
0	0	1	1	0	138	69	34.5	± 0.25%
0	0	1	1	1	136	68	34	± 0.25%
0	1	0	0	0	124	62	31	± 0.25%
0	1	0	0	1	122	61	30.5	± 0.25%
0	1	0	1	0	117	78	39	± 0.25%
0	1	0	1	1	115	76.7	38.3	± 0.25%
0	1	1	0	0	113	75.3	37.7	± 0.25%
0	1	1	0	1	108	72	36	± 0.25%
0	1	1	1	0	105	70	35	± 0.25%
0	1	1	1	1	102	68	34	± 0.25%
1	0	0	0	0	233.3	77.78	38.88	± 0.25%
1	0	0	0	1	220	73.3	36.6	± 0.5%
1	0	0	1	0	210	70	35	± 0.75%
1	0	0	1	1	200	66.6	33.3	± 0.25%
1	0	1	0	0	190	76	38	± 0.25%
1	0	1	0	1	180	72	36	± 0.25%
1	0	1	1	0	170	68	34	± 0.25%
1	0	1	1	1	150	75	37.5	± 0.25%
1	1	0	0	0	140	70	35	± 0.25%
1	1	0	0	1	120	60	30	± 0.25%
1	1	0	1	0	110	73.3	36.67	± 0.25%
1	1	0	1	1	66.6	66.6	33.3	± 0.25%
1	1	1	0	0	200	66.6	33.3	± 0.25%
1	1	1	0	1	166.6	66.64	33.32	± 0.25%
1	1	1	1	0	100	66.67	33.33	± 0.5%
1	1	1	1	1	133.33	66.67	33.33	± 0.75%

Programmable Clock Generator for VIA KT-266 Chipset
FREQUENCY (MHz) SELECTION TABLE BY GROUP TIMING

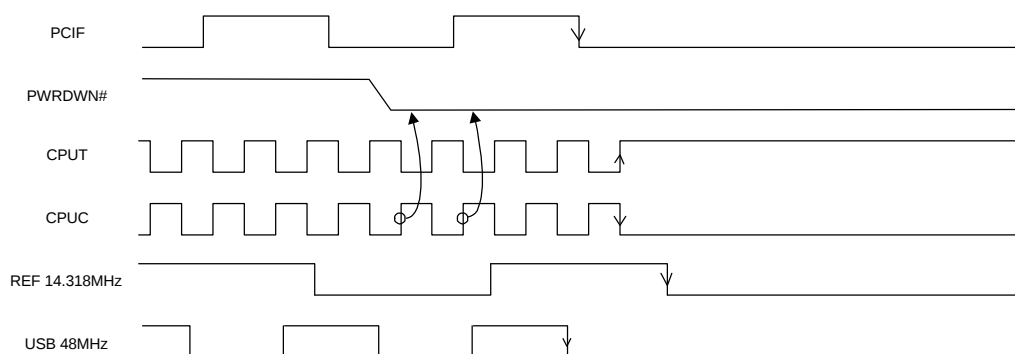
Divider Ratio (CPU:AGP)	FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI
A (1 : 1)	1	1	0	1	1	66.6	66.6	33.3
B (1.5 : 1)	1	1	1	1	0	100	66.67	33.33
	0	1	1	1	1	102	68	34
	0	1	1	1	0	105	70	35
	0	1	1	0	1	108	72	36
	1	1	0	1	0	110	73.3	36.67
	0	1	1	0	0	113	75.3	37.7
	0	1	0	1	1	115	76.7	38.3
	0	1	0	1	0	117	78	39
B (2 : 1)	1	1	0	0	1	120	60	30
	0	1	0	0	1	122	61	30.5
	0	1	0	0	0	124	62	31
	1	1	1	1	1	133.33	66.67	33.33
	0	0	1	1	1	136	68	34
	0	0	1	1	0	138	69	34.5
	1	1	0	0	0	140	70	35
	0	0	1	0	1	142	71	35.5
	0	0	1	0	0	144	72	36
	0	0	0	1	1	147	73.5	36.8
	1	0	1	1	1	150	75	37.5
	0	0	0	1	0	152	76	38
	0	0	0	0	1	154	77	38.5
	0	0	0	0	0	156	78	39
C (2.5 : 1)	1	1	1	0	1	166.6	66.64	33.32
	1	0	1	1	0	170	68	34
	1	0	1	0	1	180	72	36
	1	0	1	0	0	190	76	38
D (3 : 1)	1	1	1	0	0	200	66.6	33.3
	1	0	0	1	1	200	66.6	33.3
	1	0	0	1	0	210	70	35
	1	0	0	0	1	220	73.3	36.6
	1	0	0	0	0	233.3	77.78	38.88

Programmable Clock Generator for VIA KT-266 Chipset

PD# ASSERTION (Transition from Logic "1" to Logic "0")

1. When Power-Down (PD#) is sampled low by two consecutive rising edges of CPUC clock, then all clock outputs must be held low on their next high to low transition (except CPUT which must be driven high with a value of 2 x IREF).
2. After the clocks have all been stopped, the internal PLL stages and the Crystal oscillator will all be driven to a low power stopped condition.

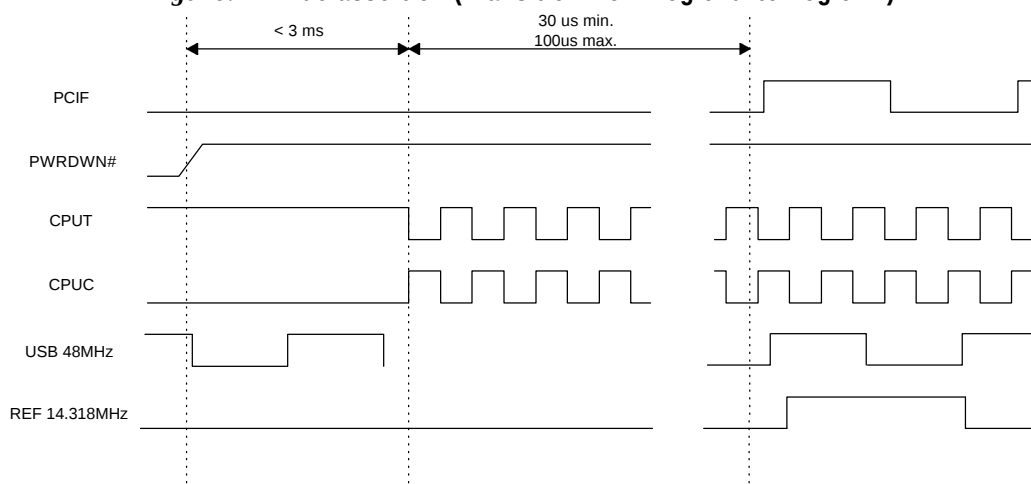
Figure: PD# assertion (Transition from Logic '1' to Logic '0')



PD# DE-ASSERTION (Transition from Logic "0" to Logic "1")

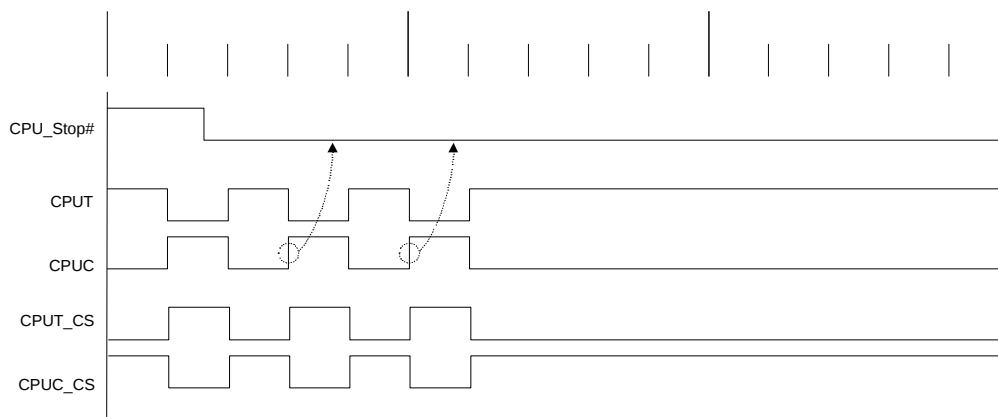
1. Power-Down (PD#) pin is taken from Low to High transition to return to normal running operation.
2. The Crystal Oscillator and the two PLL stages are released from PD to start-up to normal operation.
3. The CPU PLL clocks (differential CPU outputs) are then operating.
4. After the PCI clocks are released.
5. Following the 48 MHz (DOT and USB clocks) and the REF (14.318MHz) clocks are released.

Figure: PD# de-assertion (Transition from Logic '0' to Logic '1')



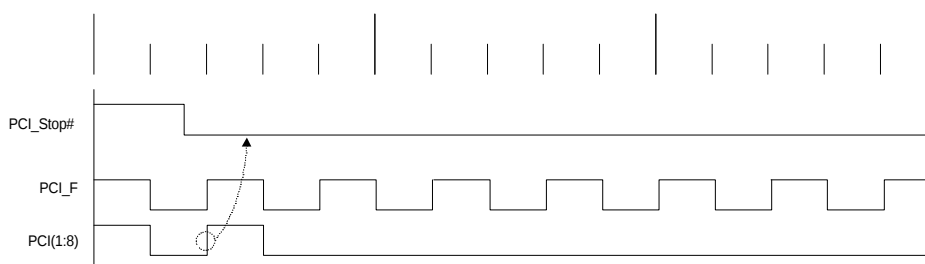
Programmable Clock Generator for VIA KT-266 Chipset

Figure: Assertion CPU_Stop# Waveforms



Note: CPU_STOP# assertion will stop all CPU outputs.

Figure: Assertion PCI_Stop# Waveforms



Note: PCI_F left free-running after PCI_STOP# assertion.

Programmable Clock Generator for VIA KT-266 Chipset

I2C BUS CONFIGURATION SETTING

Address Assignment	A6 1	A5 1	A4 0	A3 1	A2 0	A1 0	A0 1	R/W —
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbts/s							
Serial Bits Reading	The serial bits will be read or sent by the clock driver in the following order Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in Write Mode: the Command Byte and Byte Count Byte must be sent by the master but ignored by the slave, in Read Mode: the Byte Count Byte will be read by the master then all other Data Byte.							

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	0 = OFF, 1 = Spread Spectrum Enable
Bit 6	-	0	Frequency selection control bit 1=Via I2C, 0=Via External jumper
Bit 5	-	0	0 = Normal, 1 = Tristate Mode for all outputs
Bit 4	9	0	FS4 (see Frequency selection Table)
Bit 3	7	0	FS3 (see Frequency selection Table)
Bit 2	6	0	FS2 (see Frequency selection Table)
Bit 1	47	0	FS1 (see Frequency selection Table)
Bit 0	48	0	FS0 (see Frequency selection Table)

Programmable Clock Generator for VIA KT-266 Chipset

2. BYTE 1: CPU Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS2 value (Read only)
Bit 6	-	X	Inverted Power-up latched FS1 value (Read only)
Bit 5	-	1	1 = Normal, 0 = PCI Drive Enhanced 25%
Bit 4	-	X	Inverted Power-up latched FS0 value (Read only)
Bit 3	39,38	1	CPUT_CS, CPUC_CS (Active/Inactive). When disabled, defaults to CPUT_CS = 0 CPUC_CS = 1
Bit 2	42,41	1	CPUT0, CPUC0 (Active/Inactive). When disabled, defaults to CPUT0 = 1 CPUC0 = 0
Bit 1	22	1	PCI9_E (Active/Inactive)
Bit 0	21	1	PCI8 (Active/Inactive)

3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	20	1	PCI7 (Active/Inactive)
Bit 6	18	1	PCI6 (Active/Inactive)
Bit 5	17	1	PCI5 (Active/Inactive)
Bit 4	16	1	PCI4 (Active/Inactive)
Bit 3	14	1	PCI3 (Active/Inactive)
Bit 2	13	1	PCI2 (Active/Inactive)
Bit 1	11	1	PCI1 (Active/Inactive)
Bit 0	10	1	PCI0 (Active/Inactive)

4. BYTE 3: AGP Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS3 value (Read only)
Bit 6	7	1	Reserved
Bit 5	6	1	48MHz (Active/Inactive)
Bit 4	7	1	24_48MHz (Active/Inactive)
Bit 3	9	1	PCI_F (Active/Inactive)
Bit 2	28	1	AGP2 (Active/Inactive)
Bit 1	27	1	AGP1 (Active/Inactive)
Bit 0	26	1	AGP0 (Active/Inactive)

Programmable Clock Generator for VIA KT-266 Chipset

5. BYTE 4: Linear Programming Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Linear programming sign bit (0 is "+", 1 is "-")
Bit 6	-	0	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0	Linear programming magnitude bit 5
Bit 4	-	0	Linear programming magnitude bit 4
Bit 3	-	0	Linear programming magnitude bit 3
Bit 2	-	0	Linear programming magnitude bit 2
Bit 1	-	0	Linear programming magnitude bit 1
Bit 0	-	0	Linear programming magnitude bit 0 (LSB)

6. BYTE 5: Peripheral Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS4 value (Read only)
Bit 6	-	1	Reserved (Active/Inactive)
Bit 5	44	1	AGP_STOP (Active/Inactive)
Bit 4	45	1	REF_STOP (Active/Inactive)
Bit 3	46	1	REF_F (Active/Inactive)
Bit 2	-	1	Reserved
Bit 1	47	1	REF1 (Active/Inactive)
Bit 0	48	1	REF0 (Active/Inactive)

7. BYTE 6: Reserved Register (For external DDR buffer)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Programmable Clock Generator for VIA KT-266 Chipset

8. BYTE 7: Reserved Register (For external DDR buffer)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

9. BYTE 8: Watchdog Timer / Revision ID and Vendor ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable
Bit 6	-	0	Revision ID Bit 2*
Bit 5	-	0	Watchdog Time Interval Bit 5 (MSB) Revision ID Bit 1*
Bit 4	-	0	Watchdog Time Interval Bit 4 Revision ID Bit 0*
Bit 3	-	0	Watchdog Time Interval Bit 3 Vendor ID Bit 3*
Bit 2	-	0	Watchdog Time Interval Bit 2 Vendor ID Bit 2*
Bit 1	-	1	Watchdog Time Interval Bit 1 Vendor ID Bit 1*
Bit 0	-	1	Watchdog Time Interval Bit 0 (LSB) Vendor ID Bit 0*

Note: *: Default value at power-up. Don't write into this register, writing into this register can cause malfunction.

Programmable Clock Generator for VIA KT-266 Chipset

PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL205-16 device incorporates SMART-BYTE™ technology with a single byte programming via I2C to better optimize clock jitter and spread spectrum performance. Detail of PLL205-16's dual mode frequency programming method is described below:

1. ROM-table Frequency Programming:

The pre-defined 32 frequencies found in Frequency table can be accessed either through 5 external jumpers or by setting internal I2C register in BYTE0.

2. Fine-step Linear Frequency Programming:

CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around current selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency change. The formula is as follow:

$$F_{CPU} = F_{CPU-ROM-table} \pm \alpha (=0.22) * M$$

- Where:
1. M is magnitude factor defined in I2C Byte4.bit (0:6)
 2. $\pm$ (sign bit) of M is defined in I2C Byte4.bit 7
 3. α is a constant
 $\alpha = 0.22$

FREQUENCY PROGRAMMING EXAMPLE:

1. Procedures to program target CPU frequency to 130.0 Mhz in Group B timing:

- A. Locate the closest CPU frequency from Frequency from Frequency-ROM table: 124.0
- B. $\alpha = 0.22$
- C. Solve M (Linear Magnitude factor) in integer:

$$\begin{aligned} M &= (F_{CPU} - F_{CPU-ROMTABLE}) / \alpha \\ &= (130 - 124) / 0.22 \\ &= 27 \end{aligned}$$

- D. Program I2C register:

7	6	5	4	3	2	1	0	
0	1	0	0	1	0	0	0	Setting of I2C.BYTE0

CTR FS4 FS3 FS2 FS1 FS0

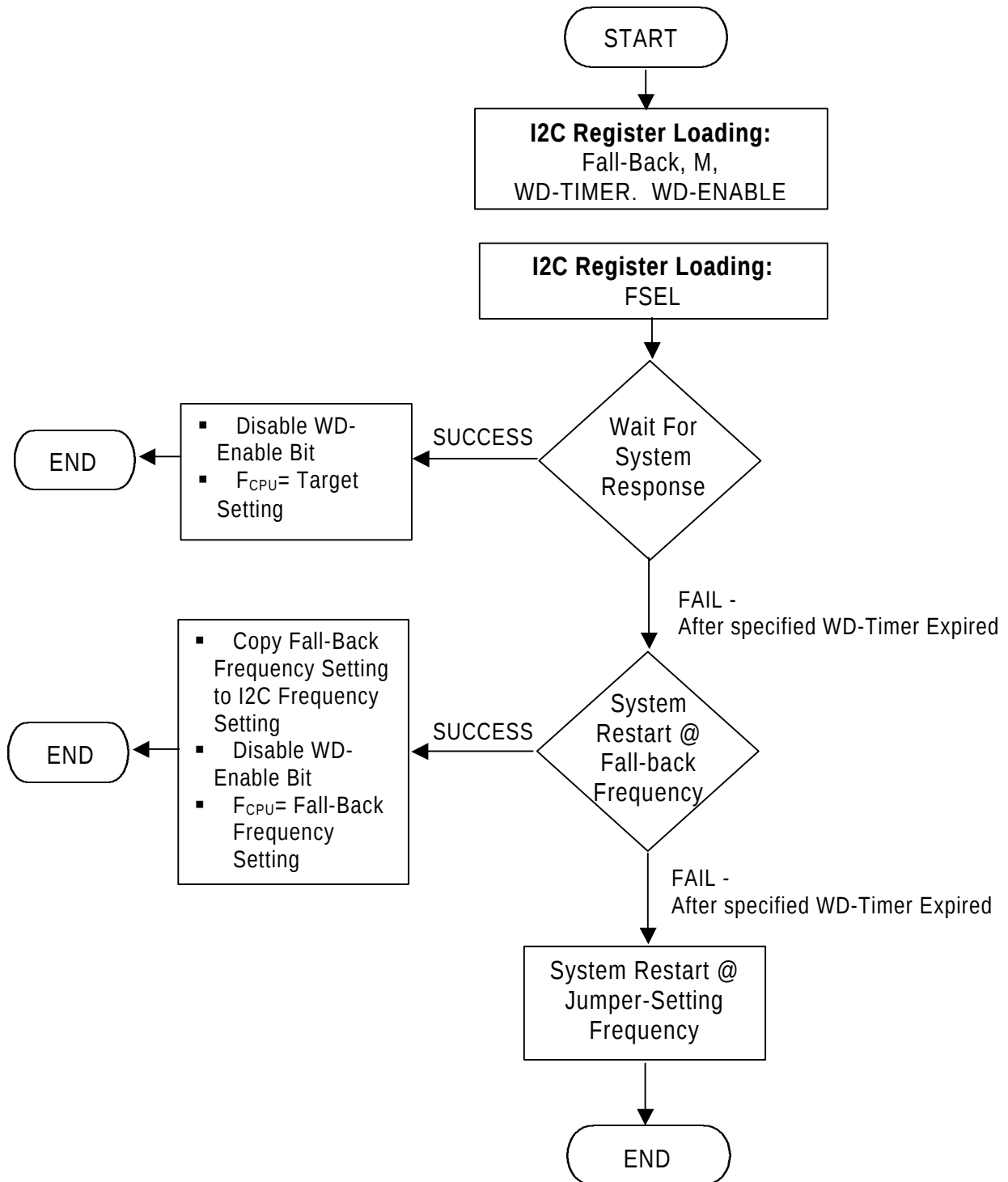
7	6	5	4	3	2	1	0	
0	0	0	1	1	0	1	1	Setting of M = +27 in I2C.BYTE4

Sign M6 M5 M4 M3 M2 M1 M0

$$\begin{aligned} F_{CPU} &= 124.0 + (0.22) * 27 = 129.94 \quad (\% \text{ of frequency increased} = 4.79\%) \\ F_{AGP} &= 62 * (1 + 4.79\%) = 64.97 \\ F_{PCI} &= 31 * (1 + 4.79\%) = 32.48 \end{aligned}$$

Programmable Clock Generator for VIA KT-266 Chipset

WDT OPERATIONAL FLOW CHART



Programmable Clock Generator for VIA KT-266 Chipset

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	$V_{SS}-0.5$	7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC/AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2		$V_{DD}+0.3$	V
Input Low Voltage	V_{IL}	All inputs except XIN	$V_{SS}-0.3$		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	uA
Input Low Current	I_{IL1}	$V_{IN}=0$ with no pull-up resistor	-5			uA
Input Low Current	I_{IL2}	$V_{IN}=0$ with pull-up resistor	-200			
Supply Current	I_{DD}	$C_L=0$ pF@66MHz, 3.3V±5%			180	mA
	I_{DDL}	$C_L=0$ pF@133MHz, 3.3V±5%				
	I_{DD}	$C_L=0$ pF@66MHz, 2.5V±5%			72	
	I_{DDL}	$C_L=0$ pF@133MHz, 2.5V±5%			100	
Transition Time	T_{trans}	To 1 st crossing of target Freq.			3	ms
Pull-up resistor	R_{PU}	Pin 6,21,35,36,44,45,47,48		120		kohm
Pull-down resistor	R_{dw}	Pin 7		120		kohm
Input frequency	F_I	$V_{DD} = 3.3V$	12	14.318	16	MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	XIN & XOUT pins	27	28	45	pF

Programmable Clock Generator for VIA KT-266 Chipset

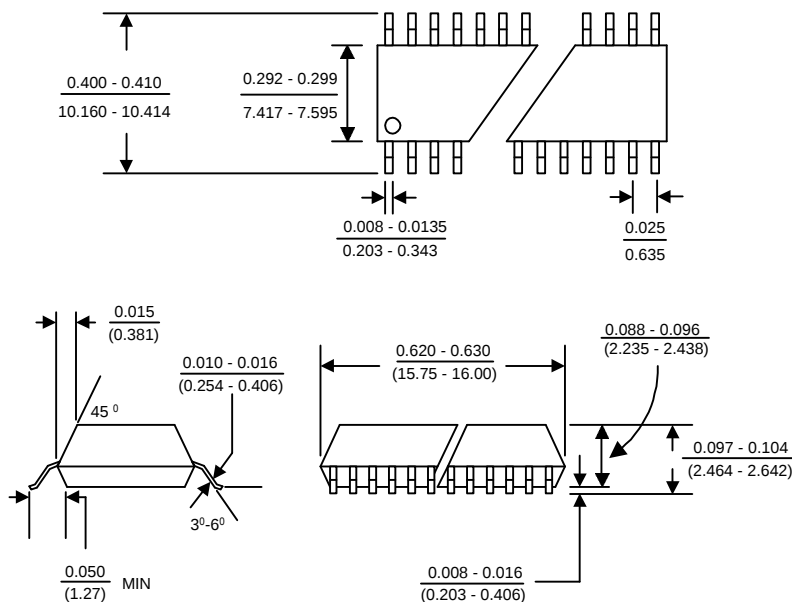
2. DC/AC Electrical Specifications (continued)

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A = 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T _{OR}	CPU	Measured @ 0.4V ~ 2.0V, C _L =10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 0.4V ~ 2.4V, C _L =10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 0.4V ~ 2.4V, C _L =10-30pf			2	
Output Fall time	T _{OF}	CPU	Measured @ 2.0 ~ 0.4V, C _L =10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 2.4V ~ 0.4V, C _L =10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 2.4V ~ 0.4V, C _L =10-30pf			2	
Duty Cycle	D _T	CPU,APIC,REF, 48MHz,24MHz	Measured @ 1.5V C _L =20pf	45	50	55	%
		PCI, AGP	Measured @ 1.5V, C _L =20~30pf	40		55	
Clock Skew	T _{SKEW}	CPU	Rising edge @ 1.25V, C _L =20pf			175	ps
		PCI	Rising edge @ 1.5V, C _L =30pf			500	
		AGP	Rising edge @ 1.5V, C _L =30pf			250	
Jitter(Cycle to Cycle)	J _{cyc-cyc}	CPU	Measured @ 1.25V			250	ps
		PCI, AGP	Measured @ 1.5V			500	
Frequency Stabilization Time	T _{FST}	CPU,PCI_F,PCI, APIC,AGP,REF, 48MHz,24MHz	Assumes full supply voltage reached within 1ms from power-up. Short cycle exist prior to frequency stabilization.			3	ms
AC output impedance	Z ₀	CPU	V _{DD} =3.3V(2.5V)±5%		20		ohm
		PCI,AGP	V _{DD} =3.3V±5%		30		
		REF,48MHz,24MHz	V _{DD} =3.3V±5%		40		

Programmable Clock Generator for VIA KT-266 Chipset

PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:

Device number, Package type and Operating temperature range

PLL205-16 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRIAL
PACKAGE TYPE
X=SSOP

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.