PhaseLink Corporation

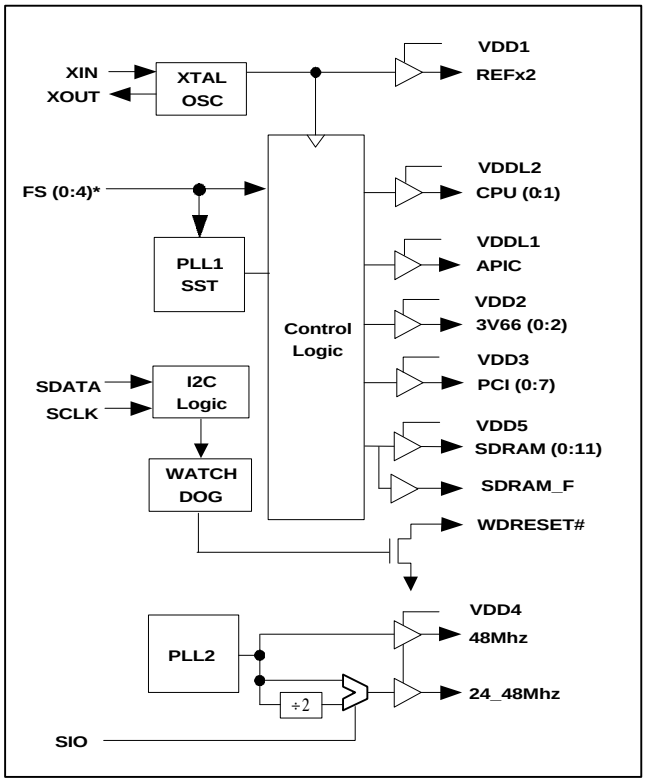
PLL203-61

Programmable Clock Generator for 815 with 133MHz FSB

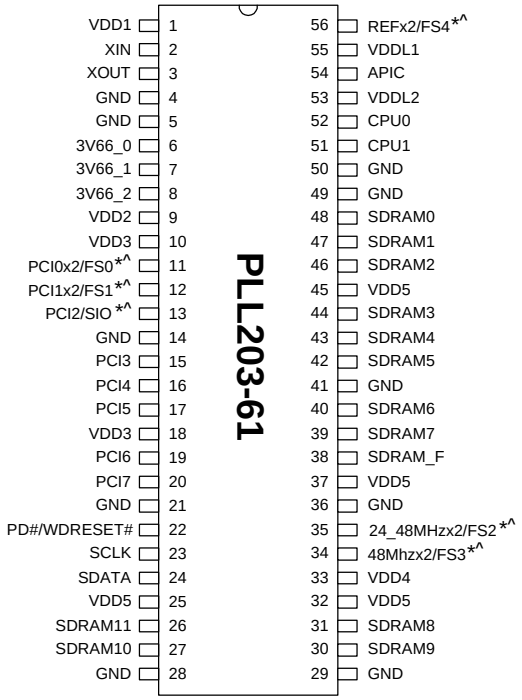
FEATURES

- Generates all clock frequencies for INTEL 815 Chip sets.
- Supports 2 CPU clocks, 13 high-speed SDRAM clocks for 3-DIMM applications and 8 PCI clocks.
- Three 3V66MHz clocks and one 2.5v APIC clock.
- One 24MHz clock and one 48MHz clock.
- One double strength 14.318MHz reference clock.
- Support 2-wire I2C serial bus with built-in Vendor ID, Device ID and Revision ID.
- Single byte micro-step linear Frequency programming via I2C with glitch free and smooth switching.
- Built-in programmable watchdog timer up to 63 seconds with 1-second interval. It will generate a LOW reset output when timer expired.
- Spread Spectrum ± 0.25% center spread.
- 50% duty cycle with low jitter.
- Available in 300 mil 56 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: ^: Pull up, #: Active low, *: Bi-directional latched at power-up

POWER GROUP

- VDD1: REF, XIN, XOUT, PLL CORE
- VDD2: 3V66(0:2) VDD3: PCI(0:7)
- VDD4: 48MHz or 24_48MHz
- VDD5: SDRAM(0:11)& SDRAM_F
- VDDL1: APIC VDDL2: CPU(0:1)

KEY SPECIFICATIONS

- Cycle to Cycle jitter:
  1) 250ps: CPU, SDRAM
  2) 500ps: APIC, 48Mhz, 3V66, PCI
- Pin to Pin Skew:
  1) 250ps: CPU, 3V66
  2) 500ps: SDRAM, APIC, PCI, 48Mhz
- Clock Offset (@CPU=100Mhz):
  1) 4.5~5.5ns: CPU-SDRAM, CPU-3V66
  2) 1.5~3.5ns: 3V66-PCI
  3) -0.5~0.5ns: SDRAM-3V66, PCI-APIC

PIN DESCRIPTIONS

Name	Number	Type	Description
REFX2/FS4	56	B	Reference 14.318Mhz Clock with 2x Drive strength. This pin latches in FS4 value at power-up. (See Frequency Selection table on page 3).
XIN	2	I	14.318 Mhz crystal input to be connected to one end of the crystal.
XOUT	3	O	14.318 Mhz crystal output.
3V66(0:2)	6,7,8	O	66MHz clock output. (See Frequency Selection table on page3).
SDRAM(0:11), SDRAM_F	48,47,46,44, 43,42,40,39, 31,30,27,26,38	O	3.3V SDRAM Clocks with frequencies defined in Frequency Selection table. SDRAM_F is free running clock output.
PCI0X2/FS0, PCI1X2/FS1	11,12	B	PCI clock output with 2X drive strength. These pins latch FS(0:1) value at power-up. (See Frequency Selection table on page 3). These pins have internal pull up resistors.
PCI(3:7)	15,16, 17,19,20	O	PCI bus clock output. (See Frequency Selection table on page 3)
PCI2/SIO	13	B	At power-up, SIO function will be activated. When SIO is Low, the output frequency of pin35 is 48MHz. When High, Pin35 is 24MHz. After input data latched, this pin is PCI clock output. Has internal pull up resistor.
48MHzX2/FS3	34	B	48MHz Clock output with 2X drive strength. This pin latches FS3 value at power-up. (See Frequency selection table on page3). This pin has internal pull up resistor.
24_48MHzx2/FS2	35	B	24 or 48MHz Clock output with 2X drive strength. This pin latches FS2 value at power-up. (See Frequency selection table on page3). This pin has internal pull up resistor.
SDATA	24	B	Serial data inputs for serial interface port.
SCLK	23	I	
PD# / WDRESET#	22	B	Power Down Control input. When low, it will disable all clock outputs including internal VCO and crystal clock. The enable of the watchdog timer masks the PD action.
CPU(0:1)	52,51	O	2.5V CPU Clocks with frequencies defined in Frequency Selection table on page3.
APIC	54	O	2.5V APIC Clock output running Synchronous with PCI/2 clock output.
VDD1	1	P	Power supply for REF, crystal oscillator, PLL Core.
VDD2	9	P	Power supply for 3V66(0:2).
VDD3	10,18	P	Power supply for PCI (0:7).
VDD4	33	P	Power supply for 48MHz or 24MHz.
VDD5	25,32,37,45	P	Power supply for SDRAM (0:11), SDRAM_F.
VDDL1	55	P	Power supply for APIC 2.5V.
VDDL2	53	P	Power supply for CPU (0:1) 2.5V.
GND	4,5,14,21,28, 29,36,41,49,50	P	Ground.

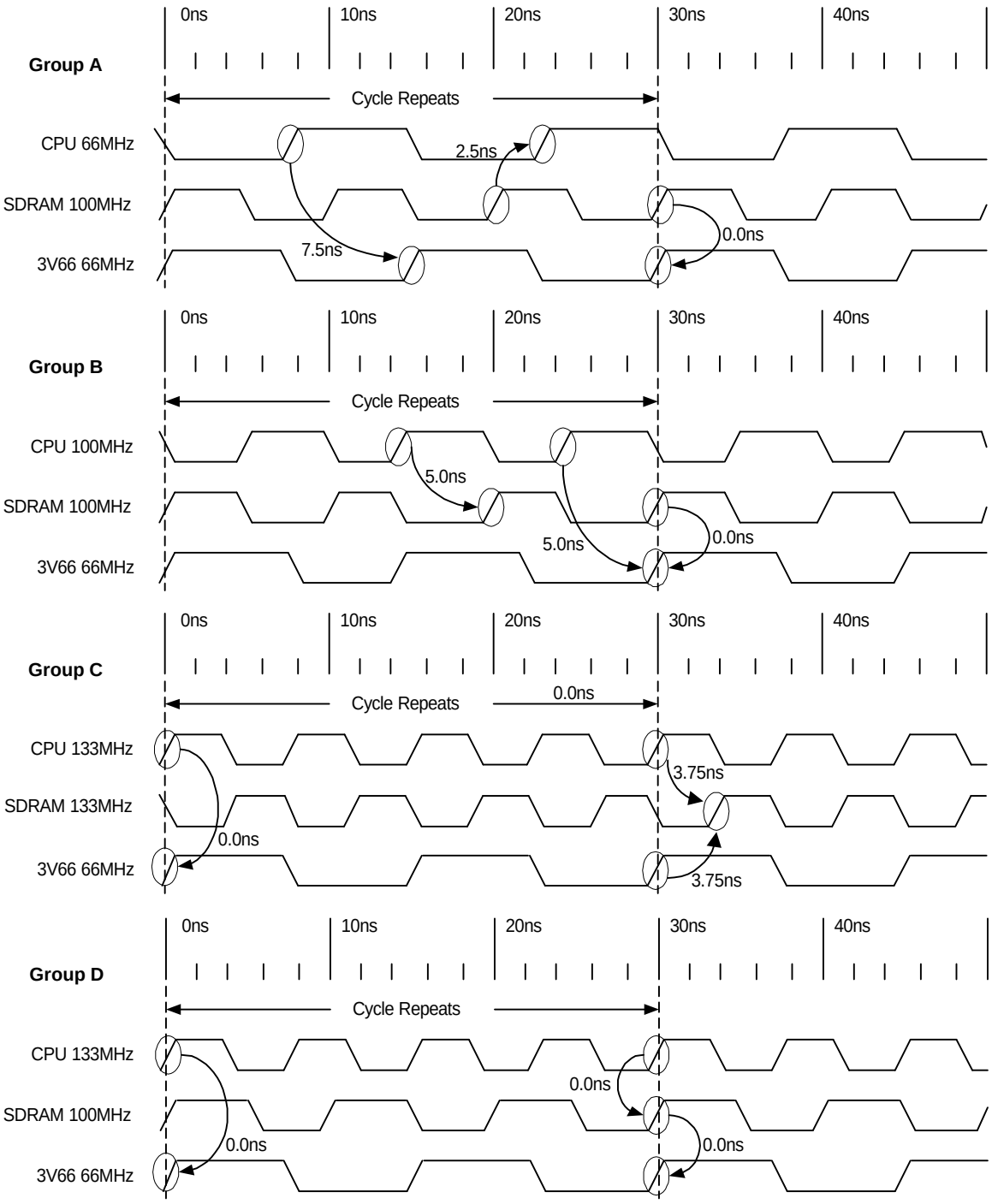
FREQUENCY (MHz) SELECTION TABLE

FS4	FS3	FS2	FS1	FS0	CPU	SDRAM	3V66	PCI	APIC
0	0	0	0	0	55.0	82.5	55.0	27.5	13.8
0	0	0	0	1	60.0	90.0	60.0	30.0	15.0
0	0	0	1	0	66.8	100.2	66.8	33.4	16.7
0	0	0	1	1	68.3	102.5	68.3	34.0	17.1
0	0	1	0	0	70.0	105.0	70.0	35.0	17.5
0	0	1	0	1	72.0	108.0	72.0	36.0	18.0
0	0	1	1	0	75.0	112.5	75.0	37.5	18.8
0	0	1	1	1	77.0	115.5	77.0	38.5	19.3
0	1	0	0	0	83.3	83.3	55.5	27.8	13.9
0	1	0	0	1	90.0	90.0	60.0	30.0	15.0
0	1	0	1	0	100.3	100.3	66.9	33.4	16.7
0	1	0	1	1	103.0	103.0	68.7	34.3	17.2
0	1	1	0	0	112.5	112.5	75.0	37.5	18.8
0	1	1	0	1	115.0	115.0	76.7	38.3	19.2
0	1	1	1	0	120.0	120.0	80.0	40.0	20.0
0	1	1	1	1	125.0	125.0	83.3	41.7	20.8
1	0	0	0	0	128.0	128.0	64.0	32.0	16.0
1	0	0	0	1	130.0	130.0	65.0	32.5	16.3
1	0	0	1	0	133.7	133.7	66.9	33.4	16.7
1	0	0	1	1	137.0	137.0	68.5	34.3	17.1
1	0	1	0	0	140.0	140.0	70.0	35.0	17.5
1	0	1	0	1	145.0	145.0	72.5	36.3	18.1
1	0	1	1	0	150.0	150.0	75.0	37.5	18.8
1	0	1	1	1	153.3	153.3	76.7	38.3	19.2
1	1	0	0	0	125.0	93.8	62.5	31.3	15.6
1	1	0	0	1	130.0	97.5	65.0	32.5	16.3
1	1	0	1	0	133.7	100.3	66.9	33.4	16.7
1	1	0	1	1	137.0	102.8	68.5	34.3	17.1
1	1	1	0	0	140.0	105.0	70.0	35.0	17.5
1	1	1	0	1	145.0	108.8	72.5	36.3	18.1
1	1	1	1	0	150.0	112.5	75.0	37.5	18.8
1	1	1	1	1	153.3	115.0	76.7	38.3	19.2

FREQUENCY (MHz) SELECTION TABLE BY GROUP TIMING

Group Timing (CPU:SDRAM:3V66)	FS4	FS3	FS2	FS1	FS0	CPU	SDRAM	3V66	PCI	APIC
A (66:100:66)	0	0	0	0	0	55.0	82.5	55.0	27.5	13.8
	0	0	0	0	1	60.0	90.0	60.0	30.0	15.0
	0	0	0	1	0	66.8	100.2	66.8	33.4	16.7
	0	0	0	1	1	68.3	102.5	68.3	34.0	17.1
	0	0	1	0	0	70.0	105.0	70.0	35.0	17.5
	0	0	1	0	1	72.0	108.0	72.0	36.0	18.0
	0	0	1	1	0	75.0	112.5	75.0	37.5	18.8
	0	0	1	1	1	77.0	115.5	77.0	38.5	19.3
B (100:100:66)	0	1	0	0	0	83.3	83.3	55.5	27.8	13.9
	0	1	0	0	1	90.0	90.0	60.0	30.0	15.0
	0	1	0	1	0	100.3	100.3	66.9	33.4	16.7
	0	1	0	1	1	103.0	103.0	68.7	34.3	17.2
	0	1	1	0	0	112.5	112.5	75.0	37.5	18.8
	0	1	1	0	1	115.0	115.0	76.7	38.3	19.2
	0	1	1	1	0	120.0	120.0	80.0	40.0	20.0
	0	1	1	1	1	125.0	125.0	83.3	41.7	20.8
C (133:133:66)	1	0	0	0	0	128.0	128.0	64.0	32.0	16.0
	1	0	0	0	1	130.0	130.0	65.0	32.5	16.3
	1	0	0	1	0	133.7	133.7	66.9	33.4	16.7
	1	0	0	1	1	137.0	137.0	68.5	34.3	17.1
	1	0	1	0	0	140.0	140.0	70.0	35.0	17.5
	1	0	1	0	1	145.0	145.0	72.5	36.3	18.1
	1	0	1	1	0	150.0	150.0	75.0	37.5	18.8
	1	0	1	1	1	153.3	153.3	76.7	38.3	19.2
D (133:100:66)	1	1	0	0	0	125.0	93.8	62.5	31.3	15.6
	1	1	0	0	1	130.0	97.5	65.0	32.5	16.3
	1	1	0	1	0	133.7	100.3	66.9	33.4	16.7
	1	1	0	1	1	137.0	102.8	68.5	34.3	17.1
	1	1	1	0	0	140.0	105.0	70.0	35.0	17.5
	1	1	1	0	1	145.0	108.8	72.5	36.3	18.1
	1	1	1	1	0	150.0	112.5	75.0	37.5	18.8
	1	1	1	1	1	153.3	115.0	76.7	38.3	19.2

GROUP OFFSET TIMING RELATIONSHIP



I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Serial Bits Reading	The serial bits will be read or sent by the clock driver in the following order Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in **Write Mode:** the **Command Byte** and **Byte Count Byte must be sent by the master** but ignored by the slave, in **Read Mode:** the **Byte Count Byte** will be **read by the master** then all other **Data Byte**. **Byte Count Byte** default at power-up is = (0x09).							

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	34	0	FS3 (see Frequency selection Table)
Bit 6	35	0	FS2 (see Frequency selection Table)
Bit 5	12	0	FS1 (see Frequency selection Table)
Bit 4	11	0	FS0 (see Frequency selection Table)
Bit 3	-	0	Frequency selection control bit 1=Via I2C, 0=Via External jumper
Bit 2	56	0	FS4 (see Frequency selection Table)
Bit 1	-	1	0 = Normal 1 = ±0.25% Center Spread
Bit 0	-	0	0 = Normal 1 = Tristate all outputs

2. BYTE 1: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS3 value (Read only)
Bit 6	-	X	Inverted Power-up latched FS0 value (Read only)
Bit 5	-	X	Inverted Power-up latched FS2 value (Read only)
Bit 4	35	1	24MHz (Active/Inactive)
Bit 3	-	X	Inverted Power-up latched SIO value (Read only)
Bit 2	34	1	48MHzX2 (Active/Inactive)
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

3. BYTE 2: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	39	1	SDRAM7 (Active/Inactive)
Bit 6	40	1	SDRAM6 (Active/Inactive)
Bit 5	42	1	SDRAM5 (Active/Inactive)
Bit 4	43	1	SDRAM4 (Active/Inactive)
Bit 3	44	1	SDRAM3 (Active/Inactive)
Bit 2	46	1	SDRAM2 (Active/Inactive)
Bit 1	47	1	SDRAM1 (Active/Inactive)
Bit 0	48	1	SDRAM0 (Active/Inactive)

4. BYTE 3: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	20	1	PCI7 (Active/Inactive)
Bit 6	19	1	PCI6 (Active/Inactive)
Bit 5	17	1	PCI5 (Active/Inactive)
Bit 4	16	1	PCI4 (Active/Inactive)
Bit 3	15	1	PCI3 (Active/Inactive)
Bit 2	13	1	PCI2 (Active/Inactive)
Bit 1	12	1	PCI1 (Active/Inactive)
Bit 0	11	1	PCI0 (Active/Inactive)

5. BYTE 4: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	6	1	3V66_0 (Active/Inactive)
Bit 6	7	1	3V66_1 (Active/Inactive)
Bit 5	8	1	3V66_2 (Active/Inactive)
Bit 4	-	X	Inverted Power-up latched FS4 value (Read only)
Bit 3	54	1	APIC (Active/Inactive)
Bit 2	-	X	Inverted Power-up latched FS1 value (Read only)
Bit 1	51	1	CPU1 (Active/Inactive)
Bit 0	52	1	CPU0 (Active/Inactive)

6. BYTE 5: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	26	1	SDRAM11 (Active/Inactive)
Bit 2	27	1	SDRAM10 (Active/Inactive)
Bit 1	30	1	SDRAM9 (Active/Inactive)
Bit 0	31	1	SDRAM8 (Active/Inactive)

7. BYTE 6: Fall-Back Frequency / Revision / Vendor ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description	
Bit 7	-	0	Revision ID Bit 3*	
Bit 6	-	0	Revision ID Bit 2*	
Bit 5	-	0	Revision ID Bit 1*	
Bit 4	-	0	WDT Fall-back Frequency selection for FS4	Revision ID Bit 0*
Bit 3	-	0	WDT Fall-back Frequency selection for FS3	Vendor ID Bit 3*
Bit 2	-	0	WDT Fall-back Frequency selection for FS2	Vendor ID Bit 2*
Bit 1	-	1	WDT Fall-back Frequency selection for FS1	Vendor ID Bit 1*
Bit 0	-	1	WDT Fall-back Frequency selection for FS0	Vendor ID Bit 0*

Note: ***:** Default value at power-up

8. BYTE 7: Linear Programming (M) Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0*	Linear programming sign bit (0 is "+", 1 is "–")
Bit 6	-	0*	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0*	Linear programming magnitude bit 5
Bit 4	-	0*	Linear programming magnitude bit 4
Bit 3	-	0*	Linear programming magnitude bit 3
Bit 2	-	0*	Linear programming magnitude bit 2
Bit 1	-	0*	Linear programming magnitude bit 1
Bit 0	-	0*	Linear programming magnitude bit 0 (LSB)

Note: This register will be initialized to 0 following WATCHDOG RESET.

9. BYTE 8: WATCHDOG TIMER / Device ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description	
Bit 7	-	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable	
Bit 6	-	0	Device ID Bit 6*	
Bit 5	-	0	Watchdog Time Interval Bit 5 (MSB)	Device ID Bit 5*
Bit 4	-	0	Watchdog Time Interval Bit 4	Device ID Bit 4*
Bit 3	-	0	Watchdog Time Interval Bit 3	Device ID Bit 3*
Bit 2	-	1	Watchdog Time Interval Bit 2	Device ID Bit 2*
Bit 1	-	0	Watchdog Time Interval Bit 1	Device ID Bit 1*
Bit 0	-	1	Watchdog Time Interval Bit 0 (LSB)	Device ID Bit 0*

Note: *: Default value at power-up

PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL203-61 device incorporates SMART-BYTE ™ technology with a single byte programming via I2C to better optimize clock jitter and spread spectrum performance. Detail of PLL203-61's dual mode frequency programming method is described below:

1. ROM-table Frequency Programming:

The pre-defined 32 frequencies found in Frequency table can be accessed either through 5 external jumpers or by setting internal I2C register in BYTE0.

2. Micro-step Linear Frequency Programming:

CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency change. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha\ (=0.22 \text{ or } 0.15) * M$$

Where:
1. M is magnitude factor defined in I2C Byte 7.bit(0:6)
2. ± (sign bit) of M is defined in I2C Byte7.bit 7
3. α is a constant but related to CPU's three Timing groups definition
   α = 0.22 (for Group B,C) or α = 0.15 (for Group A,D)

FREQUENCY PROGRAMMING EXAMPLE:

1. Procedures to program target CPU frequency to 123.0 Mhz in Group B timing:

A. Locate the closest CPU frequency from Frequency-ROM table: 120.0

B. α = 0.22 for Group B

C. Solve M (Linear Magnitude factor) in integer:

$$M = (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha$$
$$= (123 - 120) / 0.22$$
$$= 14$$

D. Program I2C register:

7	6	5	4	3	2	1	0	
1	1	1	0	1	0	0	0	Setting of I2C.BYTE0
FS3	FS2	FS1	FS0	CTR	FS4			

7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	Setting of M = +14 in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0	

F_{CPU} = 120.0 + (0.22) * 14 = 123.08 (% of frequency increased = 2.6 %)
F_{SDRAM} = 120.0 * (1+2.6%) = 123.08
F_{3V66} = 80.0 * (1+2.6%) = 82.04
F_{PCI} = 40.0 * (1+2.6%) = 41.02

BUILT-IN WATCHDOG TIMER (WDT)

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into "Hang-up" state within a reasonable period of time (or Watchdog time interval). The watchdog time interval can be programmed between 0 and 63 seconds with increment of 1 second by setting the value of I2C.Byte8.Bit(5:0). Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL203-61 will start from predefined Fall-back Frequency (the value of I2C Byte6,bits(0:4)). If system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

Example usage:

1. System power-up at CPU= 66.8MHz (Group A) where external jumpers are used.

2A. Switch to target CPU=100.3MHz frequency (Group B) with following I2C register setting:

7	6	5	4	3	2	1	0	
1	0	1	0	**1**	0	0	0	FSEL Setting in I2C.BYTE0
FS3	FS2	FS1	FS0	CTR	FS4			

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	M =0 Setting in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0	

7	6	5	4	3	2	1	0	
1	0	0	0	1	1	1	1	WD-Timer = 15s Setting in I2C.BYTE8
ENB		T5	T4	T3	T2	T1	T0	

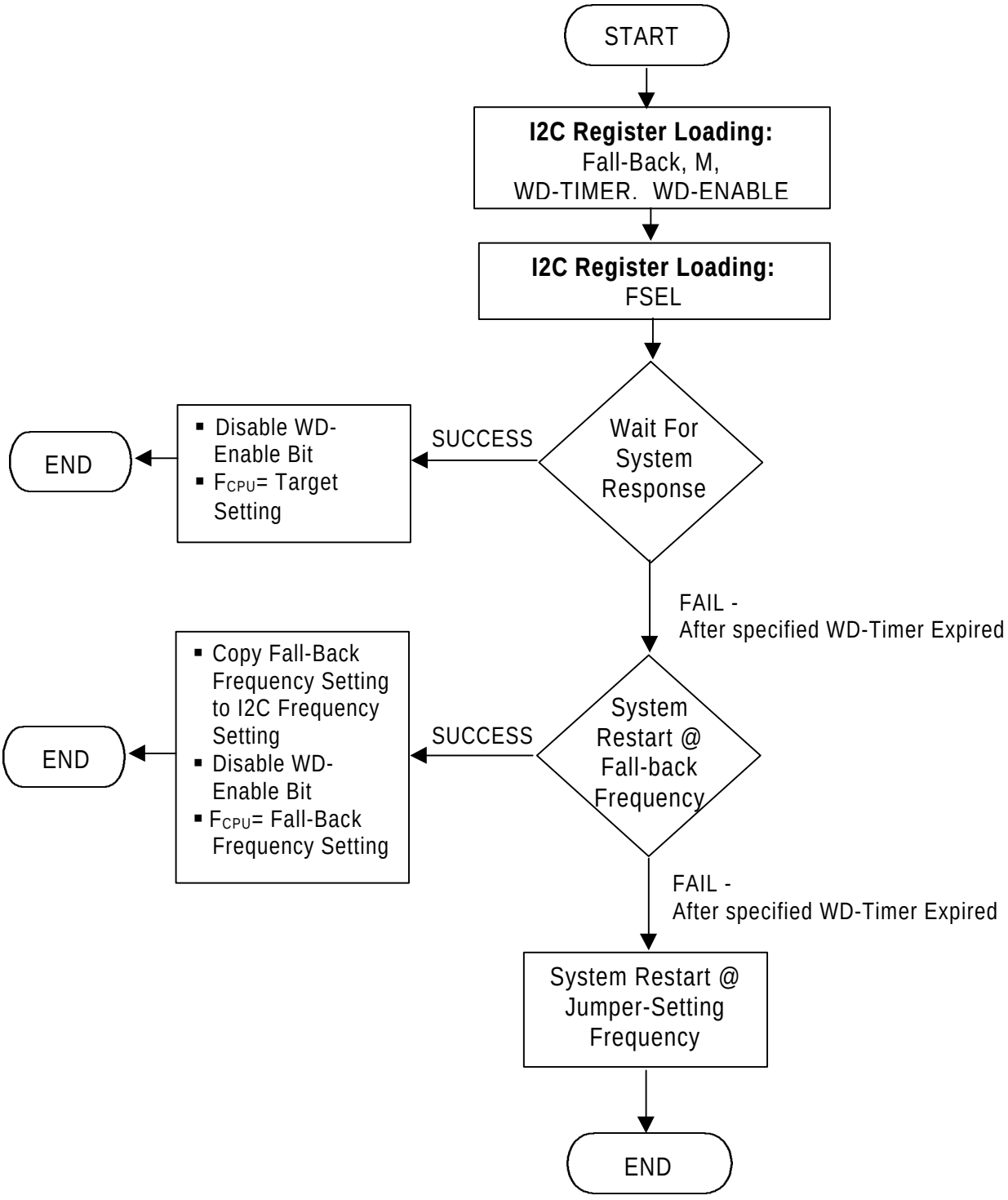
7	6	5	4	3	2	1	0	
0	0	0	0	1	0	1	0	FBSEL Setting in I2C.BYTE6
			FB4	FB3	FB2	FB1	FB0	

The fall-back frequency is set to the same location as that of FSEL since frequency switching between different timing groups will cause system to hang up. After WD timer expired or 15 seconds, the system will restart properly at target 100.3MHz if CPU is capable; otherwise WDT will perform another reset action to restart the system from 66.8 Mhz

2B. Switch to target CPU=78Mhz within the same timing Group

The fall-back frequency is recommended to set at the most safe and comfortable level to ensure a successful reboot such as 70 or 72.0 if system is unable to switch to 78Mhz.

WDT OPERATIONAL FLOW CHART



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		125	°C
ESD Voltage		2		KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC/DC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reference input clock rise time	T_{IR}	From 0.8V to 2V				ns
Reference input clock fall time	T_{IF}	From 2V to 0.8V				ns
Dynamic Current	I_{DY}	CPU at 66Mhz no load		60	110	mA
Static Current	I_S			25	50	uA
Input High Voltage	V_{IH}	All Inputs except XIN	2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}–0.3		0.8	V
Input Frequency	F_{XIN}			14.318		Mhz
Input Capacitance	C_{IN}	Logic Inputs			5	PF
	C_{OUT}	Output pin Capacitance			6	
	C_{XIN}		27		45	
Pull up resistor	R_{PU}	Pin 11,12,13,23,24,34,35,56		120		Kohm
Pull down resistor	R_{PD}			120		Kohm

2. Output Buffer Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

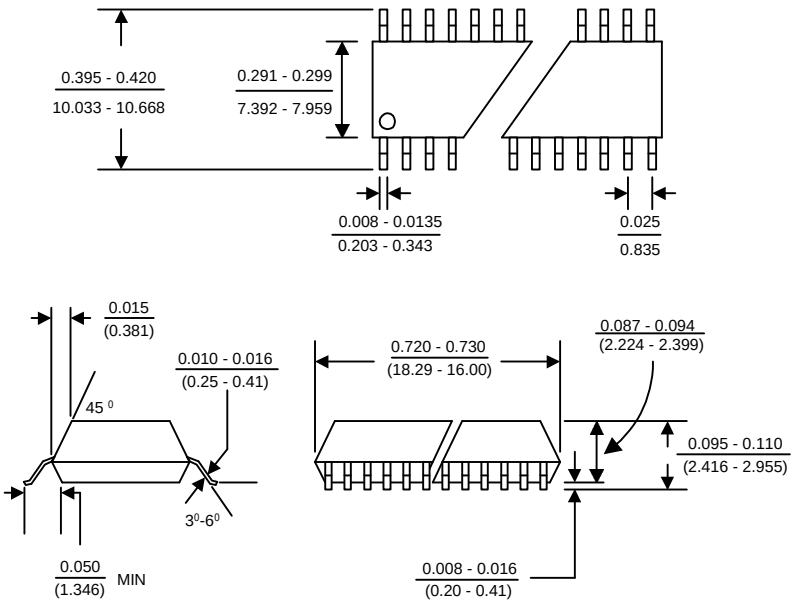
PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU,APIC	Measured @ 0.4V ~ 2.0V, C_L=10-20pf, 2.5V±0.5%	0.4		1.6	ns
		REF,48MHZ, 24_48MHZ	Measured @ 0.4V ~ 2.4V, C_L=10-20pf		1.8	4	ns
		SDRAM,3V66	Measured @ 0.4V ~ 2.4V, C_L=10-30pf	0.4		1.6	ns
		PCI		0.5		2	
Output Fall time	T_{OF}	CPU,APIC	Measured @ 2.0V ~ 0.4V, C_L=10-20pf, 2.5V±0.5%	0.4		1.6	ns
		REF,48MHZ, 24_48MHZ	Measured @ 2.4V ~ 0.4V, C_L=10-20pf		1.7	4	ns
		SDRAM,3V66	Measured @ 2.4V ~ 0.4V, C_L=10-30pf	0.4		1.6	ns
		PCI		0.5		2	
Duty Cycle	D_T	CPU,APIC	Measured @ 1.25V C_L=20pf, V_{DD}=2.5V	45	50	55	%
		REF,48MHZ, SDRAM, PCI,3V66	Measured @ 1.5V, C_L=20~30pf, V_{DD}=3.3V				
Clock Skew (pin-pin)	T_{PSKEW}	CPU	2.5V, Measured @ 1.25V			175	ps
		APIC				250	
		3V66	Measured @ 1.5V			175	
		SDRAM				250	
		PCI, 48MHZ				500	
Clock Skew	T_{SKEW}	CPU-SDRAM	CPU @ 66MhZ	2	2.5	3.0	ns
			CPU @ 100Mhz	4.5	5.0	5.5	
			CPU @ 133Mhz	-0.5	0	0.5	
		CPU-3V66	CPU @ 66MhZ	7	7.5	8	
			CPU @ 100Mhz	4.5	5.0	5.5	
			CPU @ 133Mhz	-0.5	0	0.5	
		SDRAM-3V66	CPU @ any frequency	-0.5	0	0.5	
		3V66-PCI		1.5	2.5	3.5	
		PCI-APIC		-1	0	1	

2. Output Buffer Electrical Specifications, continued

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Impedance	Z_O	CPU	V_{DD}=2.5V±0.5%	13.5		45	ohms
		APIC		9		30	
		REF,48MHZ	V_{DD}=3.3V±0.5%	20		60	
		SDRAM		10		24	
		PCI,3V66		12		55	
Output High Current	I_{OH}	CPU	V_{OUT} = 1.0V ~ 2.375V	-27		27	mA
		APIC	V_{OUT} = 1.0V ~ 2.375V	-36		-21	
		REF,48MHZ	V_{OUT} = 1.0V ~ 3.135V	-29		-23	
		SDRAM	V_{OUT} = 2.0V ~ 3.135V	-54		-46	
		PCI,3V66	V_{OUT} = 1.0V ~ 3.135V	-33		-33	
Output Low Current	I_{OL}	CPU	V_{OUT} = 1.2V ~ 0.3V	27		30	mA
		APIC	V_{OUT} = 1.2V ~ 0.3V	36		31	
		REF,48MHZ	V_{OUT} = 1.95V ~ 0.4V	29		27	
		SDRAM	V_{OUT} = 1.0V ~ 0.4V	54		53	
		PCI,3V66	V_{OUT} = 1.95V ~ 0.4V	30		38	
Jitter (cycle to cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		APIC				500	
		SDRAM	Measured @ 1.5V			250	
		48MHZ,PCI,3V66				500	
		REF				1000	

PACKAGE INFORMATION



56PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL203-61 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP