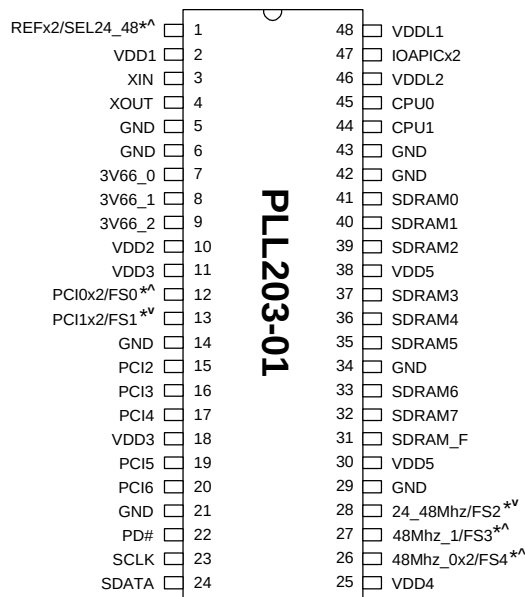


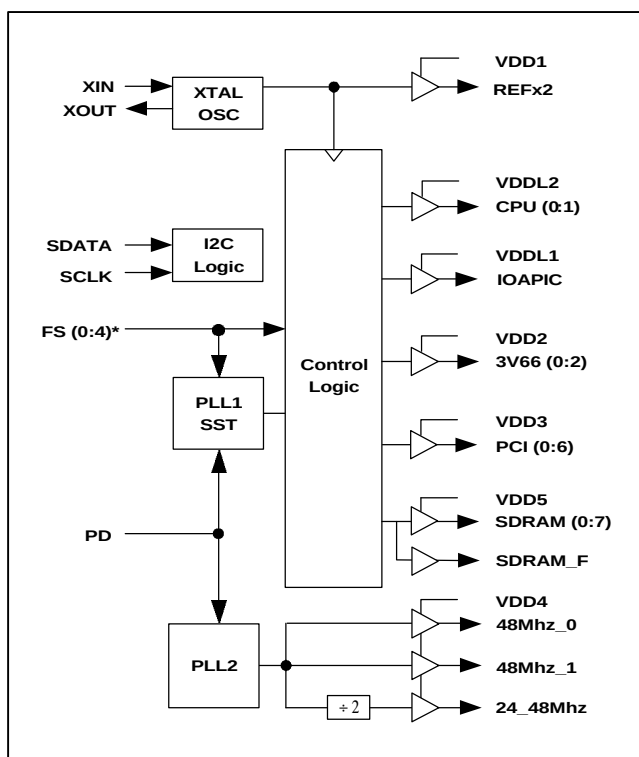
## Motherboard Clock Generator for 815 with 133MHz FSB

### PIN CONFIGURATION

- Generates all clock frequencies for INTEL 815 Chip sets.
- Supports 2 CPU clocks, 9 high-speed SDRAM clocks for 2-DIMM applications and 7 PCI clocks.
- Three 3.3V 3V66MHz clocks.
- One 24/48MHz clock and two 48MHz clocks.
- One double-strength 2.5V IOAPIC clock.
- One double-strength 14.318MHz reference clock.
- Support 2-wire I2C serial bus interface with built-in Vendor ID, Device ID and Revision ID.
- Single byte micro-step linear Frequency programming via I2C with glitch free and smooth switching.
- Spread Spectrum  $\pm 0.25\%$  center spread, 0 to 0.5% downspread.
- 50% duty cycle with low jitter.
- Available in 300 mil 48 pin SSOP.



### BLOCK DIAGRAM



Note: v: pull down, <sup>^</sup>: Pull up, #: Active low,  
\*: Bi-directional latched at power-up

### POWER GROUP

- VDD1: REF, XIN, XOUT, PLL CORE
- VDD2: 3V66(0:2) VDD3: PCI(0:6)
- VDD4: 48MHz\_0, 48MHz\_1 & 24\_48MHz
- VDD5: SDRAM(0:7)& SDRAM\_F
- VDDL1: IOAPIC VDDL2: CPU(0:1)

### KEY SPECIFICATIONS

- Cycle to Cycle jitter:
  - 250ps: CPU, SDRAM
  - 500ps: APIC, 48Mhz, 3V66, PCI
- Pin to Pin Skew:
  - 250ps: CPU, 3V66
  - 500ps: SDRAM, APIC, PCI, 48Mhz
- Clock Offset (@CPU=100Mhz):
  - 4.5~5.5ns: CPU-SDRAM, CPU-3V66
  - 1.5~3.5ns: 3V66-PCI
  - 0.5~0.5ns: SDRAM-3V66, PCI-APIC

**Motherboard Clock Generator for 815 with 133MHz FSB**
**PIN DESCRIPTIONS**

| Name                      | Number                         | Type | Description                                                                                                                                                                                      |
|---------------------------|--------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REFx2/SEL24_48            | 1                              | B    | At power up, this pin will select 24MHz (when high) or 48MHz (when low) for pin 28 output. After input sampling, this pin is double strength REF output. This pin has internal pull-up resistor. |
| XIN                       | 3                              | I    | 14.318Mhz crystal input to be connected to one end of the crystal.                                                                                                                               |
| XOUT                      | 4                              | O    | 14.318Mhz crystal output.                                                                                                                                                                        |
| 3V66(0:2)                 | 7,8,9                          | O    | 66MHz clock output. (See Frequency Selection table on page3).                                                                                                                                    |
| SDRAM(0:7),<br>SDRAM_F    | 41,40,39,37,<br>36,35,33,32,31 | O    | 3.3V SDRAM Clocks with frequencies defined in Frequency Selection table. SDRAM_F is free running clock output.                                                                                   |
| PCI0x2/FS0,<br>PCI1x2/FS1 | 12,13                          | B    | PCI clock output. These pins latch FS(0:1) value at power-on. (See Frequency Selection table on page 3). FS0 has internal pull up resistor, while FS1 has internal pull down resistor.           |
| PCI(2:6)                  | 15,16,17,19,20                 | O    | PCI bus clock output. (See Frequency Selection table on page 3)                                                                                                                                  |
| 48MHz_0x2/FS4             | 26                             | B    | Double strength 48MHz clock output. This pin latches FS4 value at power-on. (See Frequency selection table on page3). This pin has internal pull up resistor.                                    |
| 48MHz_1/FS3               | 27                             | B    | 48MHz clock output. This pin latches FS3 value at power-on. (See Frequency selection table on page3). This pin has internal pull up resistor.                                                    |
| 24_48MHz/FS2              | 28                             | B    | At power up, this pin is input pin and will determine the CPU clock frequency. It has internal pull down resistor.                                                                               |
| SDATA                     | 24                             | B    | Serial data inputs for serial interface port (I2C).                                                                                                                                              |
| SCLK                      | 23                             | I    |                                                                                                                                                                                                  |
| PD#                       | 22                             | I    | Power Down Control input. When low, it will disable all clock outputs including internal VCO and crystal clock.                                                                                  |
| CPU(0:1)                  | 45,44                          | O    | 2.5V CPU Clocks with frequencies defined in Frequency Selection table on page3.                                                                                                                  |
| IOAPICx2                  | 47                             | O    | 2.5V double strength IOAPIC clock output.                                                                                                                                                        |
| VDD1                      | 2                              | P    | Power supply for REF, crystal oscillator, PLL Core.                                                                                                                                              |
| VDD2                      | 10                             | P    | Power supply for 3V66(0:2).                                                                                                                                                                      |
| VDD3                      | 11,18                          | P    | Power supply for PCI (0:6).                                                                                                                                                                      |
| VDD4                      | 25                             | P    | Power supply for 48MHz or 24_48MHz.                                                                                                                                                              |
| VDD5                      | 30,38                          | P    | Power supply for SDRAM (0:7), SDRAM_F.                                                                                                                                                           |
| VDDL1                     | 48                             | P    | Power supply for IOAPIC 2.5V.                                                                                                                                                                    |
| VDDL2                     | 46                             | P    | Power supply for CPU (0:1) 2.5V.                                                                                                                                                                 |
| GND                       | 5,6,14,21,29,<br>34,42,43      | P    | Ground.                                                                                                                                                                                          |

**Motherboard Clock Generator for 815 with 133MHz FSB**
**FREQUENCY (MHz) SELECTION TABLE**

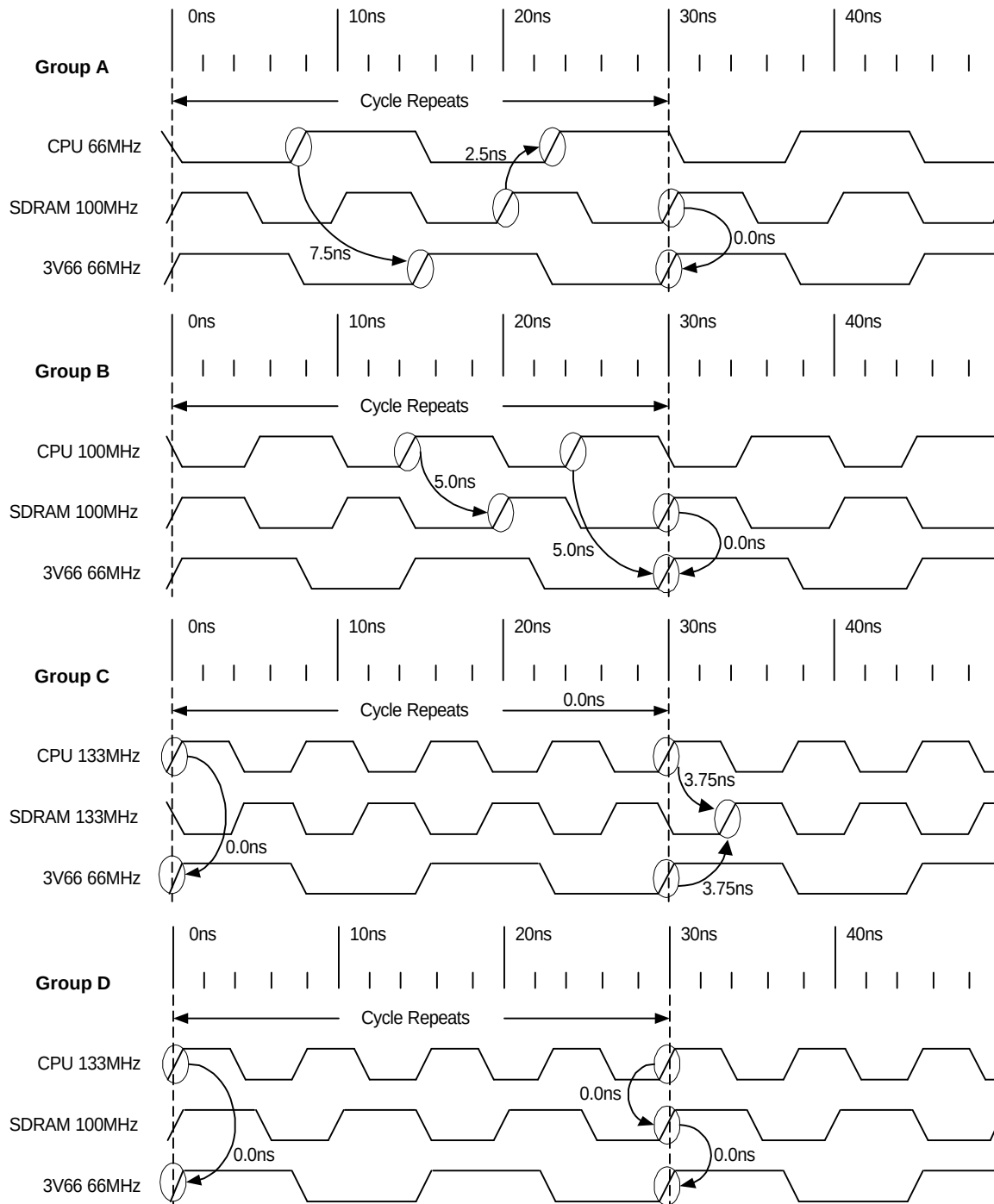
| I2C<br>Byte0<br>Bit2 | FS3 | FS2 | FS1 | FS0 | CPU   | SDRAM | 3V66  | PCI  | IOAPIC | Spread<br>Spectrum<br>Modulation |
|----------------------|-----|-----|-----|-----|-------|-------|-------|------|--------|----------------------------------|
| 0<br>default         | 0   | 0   | 0   | 0   | 66.6  | 100.0 | 66.6  | 33.3 | 16.6   | 0 to -0.5%                       |
|                      | 0   | 0   | 0   | 1   | 66.8  | 100.3 | 66.8  | 33.4 | 16.7   | ±0.25%                           |
|                      | 0   | 0   | 1   | 0   | 68.6  | 103.0 | 68.6  | 34.3 | 17.1   | ±0.25%                           |
|                      | 0   | 0   | 1   | 1   | 71.3  | 107.0 | 71.3  | 35.6 | 17.8   | ±0.25%                           |
|                      | 0   | 1   | 0   | 0   | 100.0 | 100.0 | 66.6  | 33.3 | 16.6   | 0 to -0.5%                       |
|                      | 0   | 1   | 0   | 1   | 100.3 | 100.3 | 66.8  | 33.4 | 16.7   | ±0.25%                           |
|                      | 0   | 1   | 1   | 0   | 103.0 | 103.0 | 68.6  | 34.3 | 17.1   | ±0.25%                           |
|                      | 0   | 1   | 1   | 1   | 107.0 | 107.0 | 71.3  | 35.6 | 17.8   | ±0.25%                           |
|                      | 1   | 0   | 0   | 0   | 133.3 | 133.3 | 66.6  | 33.3 | 16.6   | 0 to -0.5%                       |
|                      | 1   | 0   | 0   | 1   | 133.7 | 133.7 | 66.8  | 33.4 | 16.7   | ±0.25%                           |
|                      | 1   | 0   | 1   | 0   | 137.3 | 137.3 | 68.6  | 34.3 | 17.1   | ±0.25%                           |
|                      | 1   | 0   | 1   | 1   | 120.0 | 120.0 | 60.0  | 30.0 | 15.0   | ±0.25%                           |
|                      | 1   | 1   | 0   | 0   | 133.3 | 100.0 | 66.6  | 33.3 | 16.6   | 0 to -0.5%                       |
|                      | 1   | 1   | 0   | 1   | 133.7 | 100.3 | 66.8  | 33.4 | 16.7   | ±0.25%                           |
|                      | 1   | 1   | 1   | 0   | 137.3 | 103.0 | 68.6  | 34.3 | 17.1   | ±0.25%                           |
|                      | 1   | 1   | 1   | 1   | 120.0 | 90.0  | 60.0  | 30.0 | 15.0   | ±0.25%                           |
| 1                    | 0   | 0   | 0   | 0   | 136.0 | 136.0 | 68.0  | 34.0 | 17.0   | ±0.25%                           |
|                      | 0   | 0   | 0   | 1   | 140.0 | 140.0 | 70.0  | 35.0 | 17.5   | ±0.25%                           |
|                      | 0   | 0   | 1   | 0   | 142.6 | 142.6 | 71.3  | 35.6 | 17.8   | ±0.25%                           |
|                      | 0   | 0   | 1   | 1   | 145.3 | 145.3 | 72.6  | 36.3 | 18.1   | ±0.25%                           |
|                      | 0   | 1   | 0   | 0   | 136.0 | 102.0 | 68.0  | 34.0 | 17.0   | ±0.25%                           |
|                      | 0   | 1   | 0   | 1   | 140.0 | 105.0 | 70.0  | 35.0 | 17.5   | ±0.25%                           |
|                      | 0   | 1   | 1   | 0   | 142.6 | 107.0 | 71.3  | 35.6 | 17.8   | ±0.25%                           |
|                      | 0   | 1   | 1   | 1   | 145.3 | 109.0 | 72.6  | 36.3 | 18.1   | ±0.25%                           |
|                      | 1   | 0   | 0   | 0   | 146.6 | 146.6 | 73.3  | 36.6 | 18.3   | ±0.25%                           |
|                      | 1   | 0   | 0   | 1   | 153.3 | 153.3 | 76.6  | 38.3 | 19.1   | ±0.25%                           |
|                      | 1   | 0   | 1   | 0   | 160.0 | 160.0 | 80.0  | 40.0 | 20.0   | ±0.25%                           |
|                      | 1   | 0   | 1   | 1   | 166.6 | 166.6 | 83.3  | 41.6 | 20.8   | ±0.25%                           |
|                      | 1   | 1   | 0   | 0   | 146.6 | 110.0 | 73.3  | 36.6 | 18.3   | ±0.25%                           |
|                      | 1   | 1   | 0   | 1   | 160.0 | 120.0 | 80.0  | 40.0 | 20.0   | ±0.25%                           |
|                      | 1   | 1   | 1   | 0   | 166.6 | 125.0 | 83.3  | 41.6 | 20.8   | ±0.25%                           |
|                      | 1   | 1   | 1   | 1   | 200.0 | 200.0 | 100.0 | 50.0 | 25.0   | ±0.25%                           |

**Motherboard Clock Generator for 815 with 133MHz FSB**
**FREQUENCY (MHz) SELECTION TABLE BY GROUP TIMING**

| Group Timing<br>(CPU:SDRAM:3V66) | FS4 | FS3 | FS2 | FS1 | FS0 | CPU   | SDRAM | 3V66  | PCI  | IOAPIC |
|----------------------------------|-----|-----|-----|-----|-----|-------|-------|-------|------|--------|
| A<br>(66:100:66)                 | 0   | 0   | 0   | 0   | 0   | 66.6  | 100.0 | 66.6  | 33.3 | 16.6   |
|                                  | 0   | 0   | 0   | 0   | 1   | 66.8  | 100.3 | 66.8  | 33.4 | 16.7   |
|                                  | 0   | 0   | 0   | 1   | 0   | 68.6  | 103.0 | 68.6  | 34.3 | 17.1   |
|                                  | 0   | 0   | 0   | 1   | 1   | 71.3  | 107.0 | 71.3  | 35.6 | 17.8   |
| B<br>(100:100:66)                | 0   | 0   | 1   | 0   | 0   | 100.0 | 100.0 | 66.6  | 33.3 | 16.6   |
|                                  | 0   | 0   | 1   | 0   | 1   | 100.3 | 100.3 | 66.8  | 33.4 | 16.7   |
|                                  | 0   | 0   | 1   | 1   | 0   | 103.0 | 103.0 | 68.6  | 34.3 | 17.1   |
|                                  | 0   | 0   | 1   | 1   | 1   | 107.0 | 107.0 | 71.3  | 35.6 | 17.8   |
| C<br>(133:133:66)                | 0   | 1   | 0   | 1   | 1   | 120.0 | 120.0 | 60.0  | 30.0 | 15.0   |
|                                  | 0   | 1   | 0   | 0   | 0   | 133.3 | 133.3 | 66.6  | 33.3 | 16.6   |
|                                  | 0   | 1   | 0   | 0   | 1   | 133.7 | 133.7 | 66.8  | 33.4 | 16.7   |
|                                  | 1   | 0   | 0   | 0   | 0   | 136.0 | 136.0 | 68.0  | 34.0 | 17.0   |
|                                  | 0   | 1   | 0   | 1   | 0   | 137.3 | 137.3 | 68.6  | 34.3 | 17.1   |
|                                  | 1   | 0   | 0   | 0   | 1   | 140.0 | 140.0 | 70.0  | 35.0 | 17.5   |
|                                  | 1   | 0   | 0   | 1   | 0   | 142.6 | 142.6 | 71.3  | 35.6 | 17.8   |
|                                  | 1   | 0   | 0   | 1   | 1   | 145.3 | 145.3 | 72.6  | 36.3 | 18.7   |
|                                  | 1   | 1   | 0   | 0   | 0   | 146.6 | 146.6 | 73.3  | 36.6 | 18.3   |
|                                  | 1   | 1   | 0   | 0   | 1   | 153.3 | 153.3 | 76.6  | 38.3 | 19.1   |
|                                  | 1   | 1   | 0   | 1   | 0   | 160.0 | 160.0 | 80.0  | 40.0 | 20.0   |
|                                  | 1   | 1   | 0   | 1   | 1   | 166.6 | 166.6 | 83.3  | 41.6 | 20.8   |
|                                  | 1   | 1   | 1   | 1   | 1   | 200.0 | 200.0 | 100.0 | 50.0 | 25.0   |
| D<br>(133:100:66)                | 0   | 1   | 1   | 1   | 1   | 120.0 | 90.0  | 60.0  | 30.0 | 15.0   |
|                                  | 0   | 1   | 1   | 0   | 0   | 133.3 | 100.0 | 66.6  | 33.3 | 16.6   |
|                                  | 0   | 1   | 1   | 0   | 1   | 133.7 | 100.3 | 66.8  | 33.4 | 16.7   |
|                                  | 0   | 1   | 1   | 1   | 0   | 137.3 | 103.0 | 68.6  | 34.3 | 17.1   |
|                                  | 1   | 0   | 1   | 0   | 0   | 136.0 | 102.0 | 68.0  | 34.0 | 17.0   |
|                                  | 1   | 0   | 1   | 0   | 1   | 140.0 | 105.0 | 70.0  | 35.0 | 17.5   |
|                                  | 1   | 0   | 1   | 1   | 0   | 142.6 | 107.0 | 71.3  | 35.6 | 17.8   |
|                                  | 1   | 0   | 1   | 1   | 1   | 145.3 | 109.0 | 72.6  | 36.3 | 18.1   |
|                                  | 1   | 1   | 1   | 0   | 0   | 146.6 | 110.0 | 73.3  | 36.6 | 18.3   |
|                                  | 1   | 1   | 1   | 0   | 1   | 160.0 | 120.0 | 80.0  | 40.0 | 20.0   |
|                                  | 1   | 1   | 1   | 1   | 0   | 166.6 | 125.0 | 83.3  | 41.6 | 20.8   |

**Motherboard Clock Generator for 815 with 133MHz FSB**

**GROUP OFFSET TIMING RELATIONSHIP**



**Motherboard Clock Generator for 815 with 133MHz FSB**
**I2C BUS CONFIGURATION SETTING**

|                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |         |         |         |         |         |         |          |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------|---------|---------|---------|---------|----------|
| Address Assignment         | A6<br>1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | A5<br>1 | A4<br>0 | A3<br>1 | A2<br>0 | A1<br>0 | A0<br>1 | R/W<br>— |
| Slave Receiver/Transmitter | Provides both slave write and readback functionality                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |         |         |         |         |         |         |          |
| Data Transfer Rate         | Standard mode at 100kbts/s                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |         |         |         |         |         |          |
| Serial Bits Reading        | The serial bits will be read or sent by the clock driver in the following order<br>Byte 0 Bits 7, 6, 5, 4, 3, 2, 1, 0<br>Byte 1 Bits 7, 6, 5, 4, 3, 2, 1, 0<br>-<br>Byte N Bits 7, 6, 5, 4, 3, 2, 1, 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |         |         |         |         |         |         |          |
| Data Protocol              | This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).<br><br>Following the acknowledge of this address byte, in <b>Write Mode:</b> the <b>Command Byte</b> and <b>Byte Count Byte</b> must be sent by the master but ignored by the slave, in <b>Read Mode:</b> the <b>Byte Count Byte</b> will be read by the master then all other <b>Data Byte</b> . <b>Byte Count Byte</b> default at power-up is = (0x09). |         |         |         |         |         |         |          |

**I2C CONTROL REGISTERS**
**1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description                                                      |
|-------|------|---------|------------------------------------------------------------------|
| Bit 7 | 26   | 0       | FS3 ( see Frequency selection Table )                            |
| Bit 6 | 28   | 0       | FS2 ( see Frequency selection Table )                            |
| Bit 5 | 13   | 0       | FS1 ( see Frequency selection Table )                            |
| Bit 4 | 12   | 0       | FS0 ( see Frequency selection Table )                            |
| Bit 3 | -    | 0       | Frequency selection control bit 1=Via I2C, 0=Via External jumper |
| Bit 2 | -    | 0       | FS4 ( see Frequency selection Table )                            |
| Bit 1 | -    | 1       | 0 = Normal 1 = Spread Spectrum Enable                            |
| Bit 0 | -    | 0       | 0 = Normal 1 = Tristate all outputs                              |

**Motherboard Clock Generator for 815 with 133MHz FSB**

**2. BYTE 1: SDRAM Clock Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description                                     |
|-------|------|---------|-------------------------------------------------|
| Bit 7 | -    | X       | Inverted Power-on latched FS2 value (Read only) |
| Bit 6 | -    | X       | Inverted Power-on latched FS1 value (Read only) |
| Bit 5 | 31   | 1       | SDRAM_F (Active/Inactive)                       |
| Bit 4 | 32   | 1       | SDRAM7 (Active/Inactive)                        |
| Bit 3 | 33   | 1       | SDRAM6 (Active/Inactive)                        |
| Bit 2 | 35   | 1       | SDRAM5 (Active/Inactive)                        |
| Bit 1 | 36   | 1       | SDRAM4 (Active/Inactive)                        |
| Bit 0 | 37   | 1       | SDRAM3 (Active/Inactive)                        |

**3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description                                     |
|-------|------|---------|-------------------------------------------------|
| Bit 7 | -    | X       | Inverted Power-on latched FS0 value (Read only) |
| Bit 6 | 20   | 1       | PCI6 (Active/Inactive)                          |
| Bit 5 | 19   | 1       | PCI5 (Active/Inactive)                          |
| Bit 4 | 17   | 1       | PCI4 (Active/Inactive)                          |
| Bit 3 | 16   | 1       | PCI3 (Active/Inactive)                          |
| Bit 2 | 15   | 1       | PCI2 (Active/Inactive)                          |
| Bit 1 | 13   | 1       | PCI1 (Active/Inactive)                          |
| Bit 0 | 12   | 1       | PCI0 (Active/Inactive)                          |

**4. BYTE 3: 3V66 Clock Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description                                     |
|-------|------|---------|-------------------------------------------------|
| Bit 7 | -    | X       | Inverted Power-on latched FS4 value (Read only) |
| Bit 6 | -    | 1       | Reserved                                        |
| Bit 5 | -    | 1       | Reserved                                        |
| Bit 4 | -    | X       | Inverted Power-on latched FS3 value (Read only) |
| Bit 3 | -    | 1       | Reserved                                        |
| Bit 2 | 7    | 1       | 3V66_0                                          |
| Bit 1 | 8    | 1       | 3V66_1                                          |
| Bit 0 | 9    | 1       | 3V66_2                                          |

**Motherboard Clock Generator for 815 with 133MHz FSB**
**5. BYTE 4: Control Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description |
|-------|------|---------|-------------|
| Bit 7 | -    | 1       | Reserved    |
| Bit 6 | -    | 1       | Reserved    |
| Bit 5 | -    | 1       | Reserved    |
| Bit 4 | -    | 1       | Reserved    |
| Bit 3 | -    | 1       | Reserved    |
| Bit 2 | 26   | 1       | 48MHz_0     |
| Bit 1 | 27   | 1       | 48MHz_1     |
| Bit 0 | 28   | 1       | 24_48MHz    |

**6. BYTE 5: Control Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description                                          |
|-------|------|---------|------------------------------------------------------|
| Bit 7 | -    | X       | Inverted Power-on latched SEL24_48 value (Read only) |
| Bit 6 | 1    | 1       | REF                                                  |
| Bit 5 | 47   | 1       | IOAPIC                                               |
| Bit 4 | 44   | 1       | CPU1                                                 |
| Bit 3 | 45   | 1       | CPU0                                                 |
| Bit 2 | 39   | 1       | SDRAM2                                               |
| Bit 1 | 40   | 1       | SDRAM1                                               |
| Bit 0 | 41   | 1       | SDRAM0                                               |

**7. BYTE 6: Revision ID and Vendor ID Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description        |
|-------|------|---------|--------------------|
| Bit 7 | -    | 0       | Revision ID Bit 3* |
| Bit 6 | -    | 0       | Revision ID Bit 2* |
| Bit 5 | -    | 0       | Revision ID Bit 1* |
| Bit 4 | -    | 0       | Revision ID Bit 0* |
| Bit 3 | -    | 0       | Vendor ID Bit 3*   |
| Bit 2 | -    | 0       | Vendor ID Bit 2*   |
| Bit 1 | -    | 1       | Vendor ID Bit 1*   |
| Bit 0 | -    | 1       | Vendor ID Bit 0*   |

**Note:** \*: Default value at power-up



**Motherboard Clock Generator for 815 with 133MHz FSB**

**8. BYTE 7: Linear Programming (M) Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description                                     |
|-------|------|---------|-------------------------------------------------|
| Bit 7 | -    | 0       | Linear programming sign bit ( 0 is + , 1 is - ) |
| Bit 6 | -    | 0       | Linear programming magnitude bit 6              |
| Bit 5 | -    | 0       | Linear programming magnitude bit 5              |
| Bit 4 | -    | 0       | Linear programming magnitude bit 4              |
| Bit 3 | -    | 0       | Linear programming magnitude bit 3              |
| Bit 2 | -    | 0       | Linear programming magnitude bit 2              |
| Bit 1 | -    | 0       | Linear programming magnitude bit 1              |
| Bit 0 | -    | 0       | Linear programming magnitude bit 0              |

**9. BYTE 8: Device ID Register (1=Enable, 0=Disable)**

| Bit   | Pin# | Default | Description      |
|-------|------|---------|------------------|
| Bit 7 | -    | 0       | Reserved         |
| Bit 6 | -    | 0       | Device ID Bit 6* |
| Bit 5 | -    | 0       | Device ID Bit 5* |
| Bit 4 | -    | 0       | Device ID Bit 4* |
| Bit 3 | -    | 1       | Device ID Bit 3* |
| Bit 2 | -    | 0       | Device ID Bit 2* |
| Bit 1 | -    | 1       | Device ID Bit 1* |
| Bit 0 | -    | 0       | Device ID Bit 0* |

**Note:** \*: Default value at power-up

**Motherboard Clock Generator for 815 with 133MHz FSB**

**PROGRAMMING OF CPU FREQUENCY**

To simplify traditional loop counter setting, the PLL203-01 device incorporates SMART-BYTE technology with a single byte programming via I2C to better optimize clock jitter and spread spectrum performance. Detail of PLL203-01's dual mode frequency programming method is described below:

**1. ROM-table Frequency Programming:**

The pre-defined 32 frequencies found in Frequency table can be accessed either through 5 external jumpers or by setting internal I2C register in BYTE0.

**2. Fine-step Linear Frequency Programming:**

CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around current selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency change. The formula is as follow:

$$F_{CPU} = F_{CPU-ROM-table} \pm \alpha (=0.22 \text{ or } 0.15) * M$$

- Where:
1. M is magnitude factor defined in I2C Byte 7.bit(0:6)
  2.  $\pm$  (sign bit) of M is defined in I2C Byte7.bit 7
  3.  $\alpha$  is a constant but related to CPU's three Timing groups definition  
 $\alpha = 0.22$  (for Group B,C) or  $\alpha = 0.15$  (for Group A,D)

**FREQUENCY PROGRAMMING EXAMPLE:**

**1. Procedures to program target CPU frequency to 123.0 Mhz in Group B timing:**

- A. Locate the closest CPU frequency from Frequency from Frequency-ROM table: 120.0
- B.  $\alpha = 0.22$  for Group B
- C. Solve M (Linear Magnitude factor) in integer:

$$\begin{aligned} M &= (F_{CPU} - F_{CPU-ROMTABLE}) / \alpha \\ &= (123 - 120) / 0.22 \\ &= 14 \end{aligned}$$

- D. Program I2C register:

|   |   |   |   |   |   |   |   |                      |
|---|---|---|---|---|---|---|---|----------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                      |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Setting of I2C.BYTE0 |

FS3 FS2 FS1 FS0 CTR FS4

|      |    |    |    |    |    |    |    |                                 |
|------|----|----|----|----|----|----|----|---------------------------------|
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |                                 |
| 0    | 0  | 0  | 0  | 1  | 1  | 1  | 0  | Setting of M = +14 in I2C.BYTE7 |
| Sign | M6 | M5 | M4 | M3 | M2 | M1 | M0 |                                 |

$$\begin{aligned} F_{CPU} &= 120.0 + (0.22) * 14 = 123.08 \quad ( \% \text{ of frequency increased} = 2.6\% ) \\ F_{SDRAM} &= 120.0 * (1 + 2.6\%) = 123.12 \\ F_{3V66} &= 80.0 * (1 + 2.6\%) = 82.08 \\ F_{PCI} &= 40.0 * (1 + 2.6\%) = 41.04 \end{aligned}$$

**Motherboard Clock Generator for 815 with 133MHz FSB**
**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

| PARAMETERS                    | SYMBOL   | MIN.         | MAX.         | UNITS |
|-------------------------------|----------|--------------|--------------|-------|
| Supply Voltage                | $V_{DD}$ | $V_{SS}-0.5$ | 5.5          | V     |
| Input Voltage, dc             | $V_I$    | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V     |
| Output Voltage, dc            | $V_O$    | $V_{SS}-0.5$ | $V_{DD}+0.5$ | V     |
| Storage Temperature           | $T_S$    | -65          | 150          | °C    |
| Ambient Operating Temperature | $T_A$    | 0            | 70           | °C    |
| Junction Temperature          | $T_J$    |              | 125          | °C    |
| ESD Voltage                   |          |              | 2            | KV    |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

**2. AC/DC Electrical Specifications**

| PARAMETERS                | SYMBOL        | CONDITIONS                               | MIN.         | TYP.   | MAX.         | UNITS |
|---------------------------|---------------|------------------------------------------|--------------|--------|--------------|-------|
| Operating Supply Current  | $I_{DD3.3OP}$ | $C_L = 0 \text{ pF @ } 66\text{MHz}$     |              |        | 100          | mA    |
| Input High Current        | $I_{IH}$      | $V_{IH} = V_{DD}$                        | -5           |        | 5            | uA    |
| Input Low Current         | $I_{IL1}$     | $V_{IN} = 0$ ; With no pull-up resistors | -5           |        |              | uA    |
| Input Low Current         | $I_{IL2}$     | $V_{IN} = 0$ ; With pull-up resistors    | -200         |        |              | uA    |
| Input High Voltage        | $V_{IH}$      | All Inputs except XIN                    | 2            |        | $V_{DD}+0.3$ | V     |
| Input Low Voltage         | $V_{IL}$      | All inputs except XIN                    | $V_{SS}-0.3$ |        | 0.8          | V     |
| Input Frequency           | $F_{XIN}$     |                                          |              | 14.318 |              | Mhz   |
| Input Capacitance         | $C_{IN}$      | Logic Inputs                             |              |        | 5            | PF    |
|                           | $C_{OUT}$     | Output pin Capacitance                   |              |        | 6            |       |
|                           | $C_{XIN}$     |                                          | 27           |        | 45           |       |
| Power Down Supply Current | $I_{PD}$      | $C_L=0 \text{ pF}$                       |              |        | 600          | uA    |
| Pull up resistor          | $R_{PU}$      | Pin 1,12,26,27                           |              | 120    |              | Kohm  |
| Pull down resistor        | $R_{PD}$      | Pin 13,28                                |              | 120    |              | Kohm  |

**Motherboard Clock Generator for 815 with 133MHz FSB**
**2. Output Buffer Electrical Specifications**

 Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T<sub>A</sub>= 0°C to 70°C

| PARAMETERS           | SYMBOL             | OUTPUTS                       | CONDITIONS                                                         | MIN. | TYP. | MAX. | UNITS |
|----------------------|--------------------|-------------------------------|--------------------------------------------------------------------|------|------|------|-------|
| Output Rise time     | T <sub>OR</sub>    | CPU,IOAPIC                    | Measured @ 0.4V ~ 2.0V,<br>C <sub>L</sub> =10-20pf, 2.5V±0.5%      | 0.4  |      | 1.6  | ns    |
|                      |                    | REF,48MHZ,<br>24_48MHZ        | Measured @ 0.4V ~ 2.4V,<br>C <sub>L</sub> =10-20pf                 |      | 1.8  | 4    | ns    |
|                      |                    | SDRAM                         | Measured @ 0.4V ~ 2.4V,<br>C <sub>L</sub> =10-30pf                 | 0.4  |      | 1.6  | ns    |
|                      |                    | PCI,3V66                      |                                                                    | 0.5  |      | 2    |       |
| Output Fall time     | T <sub>OF</sub>    | CPU,IOAPIC                    | Measured @ 2.0V ~ 0.4V,<br>C <sub>L</sub> =10-20pf, 2.5V±0.5%      | 0.4  |      | 1.6  | ns    |
|                      |                    | REF,48MHZ,<br>24_48MHZ        | Measured @ 2.4V ~ 0.4V,<br>C <sub>L</sub> =10-20pf                 |      | 1.7  | 4    | ns    |
|                      |                    | SDRAM                         | Measured @ 2.4V ~ 0.4V,<br>C <sub>L</sub> =10-30pf                 | 0.4  |      | 1.6  | ns    |
|                      |                    | PCI,3V66                      |                                                                    | 0.5  |      | 2    |       |
| Duty Cycle           | D <sub>T</sub>     | CPU,IOAPIC                    | Measured @ 1.25V<br>C <sub>L</sub> =20pf, V <sub>DD</sub> =2.5V    | 45   | 50   | 55   | %     |
|                      |                    | REF,48MHZ,<br>SDRAM, PCI,3V66 | Measured @ 1.5V,<br>C <sub>L</sub> =20~30pf, V <sub>DD</sub> =3.3V |      |      |      |       |
| Clock Skew (pin-pin) | T <sub>PSKEW</sub> | CPU                           | 2.5V, Measured @ 1.25V                                             |      |      | 250  | ps    |
|                      |                    | IOAPIC                        |                                                                    |      |      | 250  |       |
|                      |                    | 3V66                          | Measured @ 1.5V                                                    |      |      | 175  |       |
|                      |                    | SDRAM,48MHz                   |                                                                    |      |      | 250  |       |
|                      |                    | PCI                           |                                                                    |      |      | 500  |       |
| Clock Skew           | T <sub>SKEW</sub>  | CPU-SDRAM                     | CPU @ 66Mhz                                                        | 2    | 2.5  | 3.0  | ns    |
|                      |                    |                               | CPU @ 100Mhz                                                       | 4.5  | 5.0  | 5.5  |       |
|                      |                    |                               | CPU @ 133Mhz                                                       | -0.5 | 0    | 0.5  |       |
|                      |                    | CPU-3V66                      | CPU @ 66Mhz                                                        | 7    | 7.5  | 8    |       |
|                      |                    |                               | CPU @ 100Mhz                                                       | 4.5  | 5.0  | 5.5  |       |
|                      |                    |                               | CPU @ 133Mhz                                                       | -0.5 | 0    | 0.5  |       |
|                      |                    | SDRAM-3V66                    | CPU @ any frequency                                                | -0.5 | 0    | 0.5  |       |
|                      |                    | 3V66-PCI                      |                                                                    | 1.5  | 2.5  | 3.5  |       |
|                      |                    | PCI-IOAPIC                    |                                                                    | -1   | 0    | 1    |       |

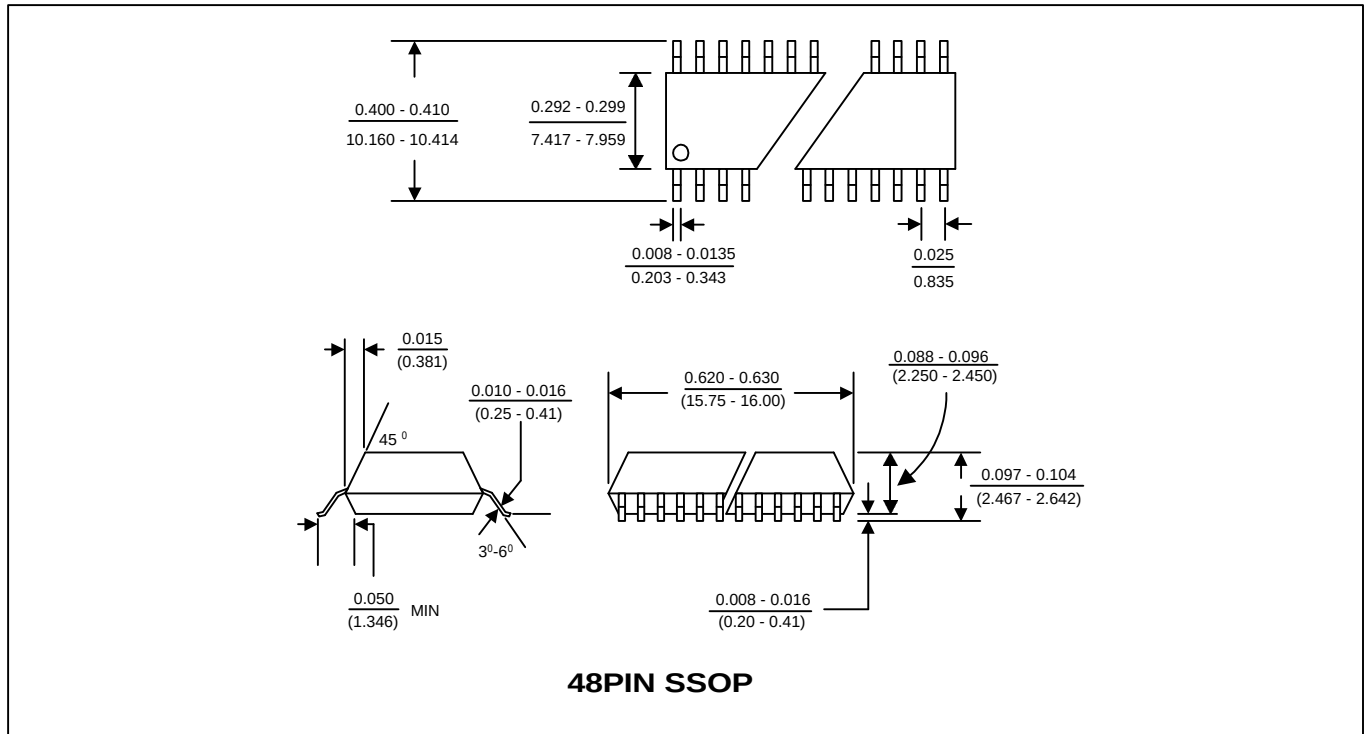
**Motherboard Clock Generator for 815 with 133MHz FSB**
**2. Output Buffer Electrical Specifications, continued**

 Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T<sub>A</sub>= 0°C to 70°C

| PARAMETERS              | SYMBOL               | OUTPUTS   | CONDITIONS                       | MIN. | TYP. | MAX. | UNITS |
|-------------------------|----------------------|-----------|----------------------------------|------|------|------|-------|
| Output Impedance        | Z <sub>O</sub>       | CPU       | V <sub>DD</sub> =2.5V±0.5%       | 13.5 |      | 45   | ohm   |
|                         |                      | IOAPIC    |                                  | 9    |      | 30   |       |
|                         |                      | REF,48MHZ | V <sub>DD</sub> =3.3V±0.5%       | 20   |      | 60   |       |
|                         |                      | SDRAM     |                                  | 10   |      | 24   |       |
|                         |                      | PCI,3V66  |                                  | 12   |      | 55   |       |
| Output High Current     | I <sub>OH</sub>      | CPU       | V <sub>OUT</sub> = 1.0V ~ 2.375V | -27  |      | 27   | mA    |
|                         |                      | IOAPIC    | V <sub>OUT</sub> = 1.0V ~ 2.375V | -27  |      | -27  |       |
|                         |                      | REF,48MHZ | V <sub>OUT</sub> = 1.0V ~ 3.135V | -29  |      | -23  |       |
|                         |                      | SDRAM     | V <sub>OUT</sub> = 2.0V ~ 3.135V | -54  |      | -46  |       |
|                         |                      | PCI,3V66  | V <sub>OUT</sub> = 1.0V ~ 3.135V | -33  |      | -33  |       |
| Output Low Current      | I <sub>OL</sub>      | CPU       | V <sub>OUT</sub> = 1.2V ~ 0.3V   | 27   |      | 30   | mA    |
|                         |                      | IOAPIC    | V <sub>OUT</sub> = 1.2V ~ 0.3V   | 27   |      | 30   |       |
|                         |                      | REF,48MHZ | V <sub>OUT</sub> = 1.95V ~ 0.4V  | 29   |      | 27   |       |
|                         |                      | SDRAM     | V <sub>OUT</sub> = 1.0V ~ 0.4V   | 54   |      | 53   |       |
|                         |                      | PCI,3V66  | V <sub>OUT</sub> = 1.95V ~ 0.4V  | 30   |      | 38   |       |
| Jitter (cycle to cycle) | J <sub>cyc-cyc</sub> | CPU       | Measured @ 1.25V                 |      |      | 250  | ps    |
|                         |                      | IOAPIC    |                                  |      |      | 500  |       |
|                         |                      | SDRAM     | Measured @ 1.5V                  |      |      | 250  |       |
|                         |                      | PCI,3V66  |                                  |      |      | 500  |       |
|                         |                      | REF,48MHZ |                                  |      |      | 1000 |       |

**Motherboard Clock Generator for 815 with 133MHz FSB**

**PACKAGE INFORMATION**



**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

45437 Warm Springs Blvd., Fremont, CA 94539, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range

**PLL203-01 X C**

PART NUMBER

TEMPERATURATURE  
C=COMMERCIAL  
M=MILITARY  
I=INDUSTRIAL  
PACKAGE TYPE  
X=SSOP

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