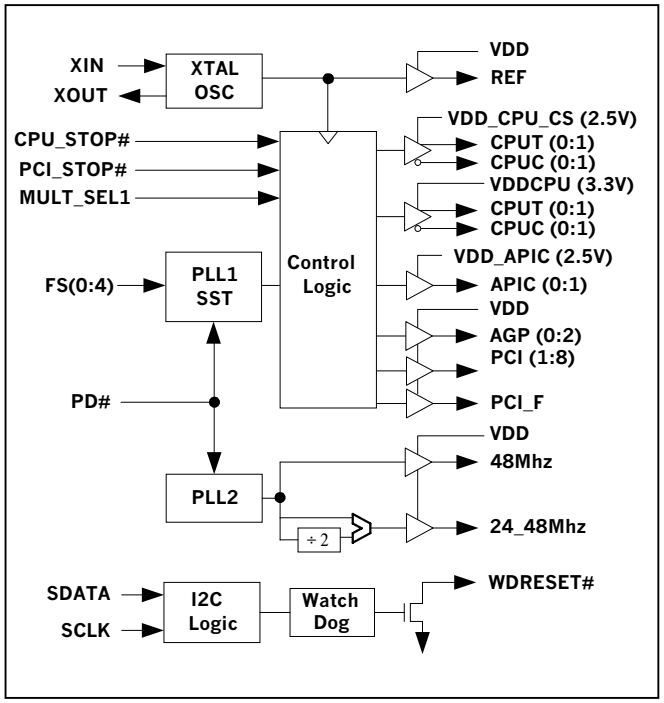
PLL202-16

Programmable Clock Generator for VIA P4X266

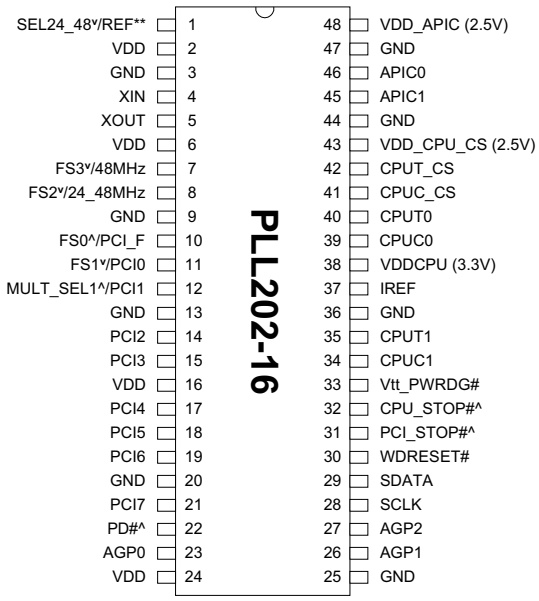
FEATURES

- Clock frequency generator for VIA Pentium4 chipsets.
- Provides 1 REF clock, 3 CPU (including one at 2.5V for the Chipset), 3 AGP, and 9 PCI clocks.
- One 48MHz clock, one 24_48MHz clock.
- Enhanced PCI Output Drive selectable by I2C.
- Two 2.5V APIC and one 14.318MHz ref. Clocks.
- Power management control for CPU and PCI.
- Single byte micro-step linear Frequency Programming via I2C with glitch free smooth switching.
- Built-in programmable watchdog timer up to 63 seconds with 1-second interval. It will generate a low reset output when timer expired, with programmable WD reset frequency.
- Spread Spectrum ±0.25% center, ±0.5% center, ±0.75% center.
- 50% duty cycle with low jitter.
- Available in 300 mil 48 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: ^: Pull up – ᵛ: Pull down – **#:** Active low – **: 2x drive strength

POWER GROUP

- 3.3V: VDD and VDDCPU – for REF, XIN, XOUT, PLL CORE, PCI, AGP, APIC, CPUT(0:1), and CPUC(0:1)
- 2.5V: VDD_APIC and VDD_CPU_CS – for CPUC_CS and CPUT_CS

KEY SPECIFICATIONS

- CPU Cycle to Cycle jitter: 250ps.
- PCI Cycle to Cycle jitter: 500ps.
- PCI to PCI skew: 500ps.
- CPU to CPU skew 175ps.
- CPU to PCI skew (CPU lead): typical 2ns.
- AGP to AGP skew: 250ps.

PIN DESCRIPTIONS

Name	Number	Type	Description
SEL24_48/REF	1	B	Bi-directional pin. At power-up, the SEL24_48 input value is sensed and internally latched. 0 = 24MHz, 1 = 48MHz. After power-up, the pin acts as 3.3V REF 14.318MHz output (2x drive strength). This pin has a 100kΩ internal pull-down.
XIN	4	I	14.318Mhz crystal input to be connected to one end of the crystal.
XOUT	5	O	14.318Mhz crystal output.
FS3/48MHz	7	B	Bi-directional pin. At power-up, the FS3 input value is sensed and internally latched. After power-up, the pin acts as fixed 48MHz output. This pin has a 100kΩ internal pull-down.
FS2/24_48MHz	8	B	Bi-directional pin. At power-up, the FS2 input value is sensed and internally latched. After power-up, the pin acts as fixed 48 or 24MHz output (I2C selectable). This pin has a 100kΩ internal pull-down.
FS0/PCI_F	10	B	Bi-directional pin. At power-up, the FS0 input value is sensed and internally latched. After power-up, the pin acts as PCI_F output. This pin has a 100kΩ internal pull-up.
FS1/PCI0	11	B	Bi-directional pin. At power-up, the FS1 input value is sensed and internally latched. After power-up, the pin acts as PCI1 output. This pin has a 100kΩ internal pull-down.
MULT_SEL1/PCI1	12	B	Bi-directional pin. At power-up, the MULT_SEL1 input value is sensed and internally latched. After power-up, the pin acts as PCI1 output. MULT_SEL1 is used to define the current multiplier of the CPU clock outputs. 0 selects Ioh = 4 x IREF, 1 selects Ioh = 6 x IREF. This pin has a 100kΩ internal pull-up.
PCI(2:7)	14,15,17, 18,19,21	O	PCI clock outputs.
PD#	22	I	Power Down Control input. When low, Power Down will disable all clock outputs including internal VCO and crystal clock. This pin has a 100kΩ internal pull-up.
AGP(0:2)	23,26,27	O	AGP clock outputs.
SCLK	28	B	Serial data input for serial interface port.
SDATA	29	I	
WDRESET#	30	O	Watchdog timer reset signal.
PCI_STOP#	31	I	Halts PCI clocks when low (except PCI_F which is free running). This pin has a 100kΩ internal pull-up.
CPU_STOP#	32	I	Halts CPU clocks when input low. This pin has a 100kΩ internal pull-up
Vtt_PWRG#	33	I	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS (0:3) and MULT_SEL1 inputs are valid and ready to be sampled (active low).

PIN DESCRIPTIONS (continued)

CPUT(0:1)	35,40	O	True clock of differential pair of CPU outputs.
CPUC(0:1)	34,39	O	Complementary clock of differential pair of CPU outputs.
IREF	37	I	This pin establishes the reference current for the CPU pairs, it requires a fixed precision resistor tied to ground in order to establish the appropriate current.
CPUT_CS	42	O	True CPU output for the Chipset (2.5V push-pull output).
CPUC_CS	41	O	Complementary CPU output for the Chipset (2.5V push-pull output).
APIC(0:1)	45,46	O	APIC clock outputs running at half of PCI output frequency.
VDD	2,6,16,24,38,48	P	3.3V Power Supply.
VDD_CPU_CS	43	P	2.5V Power Supply for CPUT_CS and CPUC_CS outputs.
VDD_APIC	48	P	2.5V Power Supply for APIC outputs.
GND	3,9,13,20, 25,36,44,47	P	Ground (0.0V) connector.

HOST SWING SELECT FUNCTIONS

MULT_SEL1	Board target trace (Z)	Reference R (Rr); IREF = VDD/(3*Rr)	Output Current	Voh @ Z
0	50 Ω	Rr = 221Ω (1%); IREF = 5.00mA	Ioh = 4 x IREF	1.0V @ 50
1	50 Ω	Rr = 475Ω (1%); IREF = 2.32mA	Ioh = 6 x IREF	0.7V @ 50

FREQUENCY (MHz) SELECTION TABLE

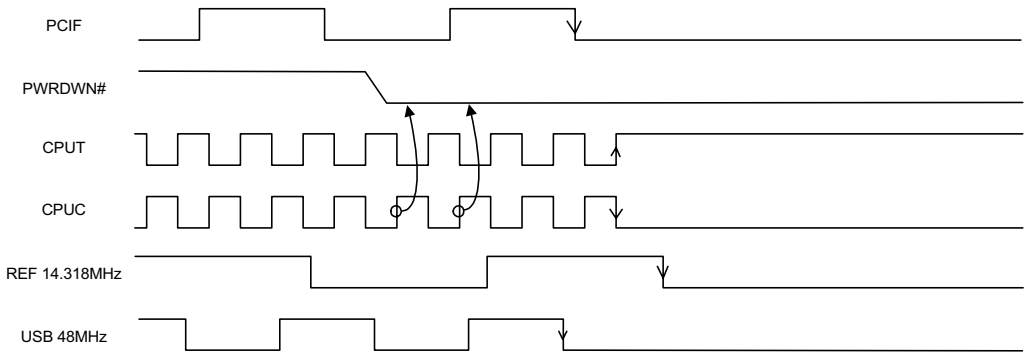
FS4	FS3	FS2	FS1	FS0	CPU	AGP	PCI	Spread Spectrum
0	0	0	0	0	66.67	66.66	33.33	± 0.25%
0	0	0	0	1	100	66.67	33.33	± 0.25%
0	0	0	1	0	133.33	66.67	33.33	± 0.25%
0	0	0	1	1	200	66.66	33.33	± 0.25%
0	0	1	0	0	100.9	67.27	33.63	± 0.25%
0	0	1	0	1	103	68.67	34.33	± 0.25%
0	0	1	1	0	107	71.33	35.67	± 0.25%
0	0	1	1	1	110	73.33	36.67	± 0.25%
0	1	0	0	0	133.9	66.95	33.48	± 0.25%
0	1	0	0	1	137.33	68.66	34.33	± 0.25%
0	1	0	1	0	140	70	35	± 0.25%
0	1	0	1	1	142.66	71.33	35.67	± 0.25%
0	1	1	0	0	145.33	72.66	36.33	± 0.25%
0	1	1	0	1	146.66	73.33	36.67	± 0.25%
0	1	1	1	0	153.33	76.66	38.33	± 0.25%
0	1	1	1	1	160	80	40	± 0.25%
1	0	0	0	0	66.67	66.66	33.33	± 0.50%
1	0	0	0	1	100	66.67	33.33	± 0.50%
1	0	0	1	0	133.33	66.67	33.33	± 0.50%
1	0	0	1	1	200	66.66	33.33	± 0.50%
1	0	1	0	0	66.67	66.66	33.33	± 0.75%
1	0	1	0	1	100	66.67	33.33	± 0.75%
1	0	1	1	0	133.33	66.67	33.33	± 0.75%
1	0	1	1	1	200	66.66	33.33	± 0.75%
1	1	0	0	0	201	67	35.5	± 0.25%
1	1	0	0	1	203	67.67	33.83	± 0.25%
1	1	0	1	0	205	68.33	34.17	± 0.25%
1	1	0	1	1	207	69	34.5	± 0.25%
1	1	1	0	0	66.66	66.66	33.33	± 0.25%
1	1	1	0	1	100	66.66	33.33	± 0.25%
1	1	1	1	0	200	66.66	33.33	± 0.25%
1	1	1	1	1	133.3	66.66	33.33	± 0.25%

Note: FS4 available through I2C only

PD# ASSERTION (Transition from Logic “1” to Logic “0”)

1. When Power-Down (PD#) is sampled low by two consecutive rising edges of CPUC clock, then all clock outputs must be held low on their next high to low transition (except CPUT which must be driven high with a value of 2 x IREF).
2. After the clocks have all been stopped, the internal PLL stages and the Crystal oscillator will all be driven to a low power stopped condition.

Figure: **PD# assertion (Transition from Logic '1' to Logic '0')**



PD# DE-ASSERTION (Transition from Topic "0" to Topic "1")

1. Power-Down (PD#) pin is taken from Low to High transition to return to normal running operation.
2. The Crystal Oscillator and the two PLL stages are released from PD to start-up to normal operation.
3. The CPU PLL clocks (differential CPU outputs) are then operating.
4. After the PCI clocks are released.
5. Following the 48 MHz (DOT and USB clocks) and the REF (14.318MHz) clocks are released.

Figure: **PD# de-assertion (Transition from Logic '0' to Logic '1')**

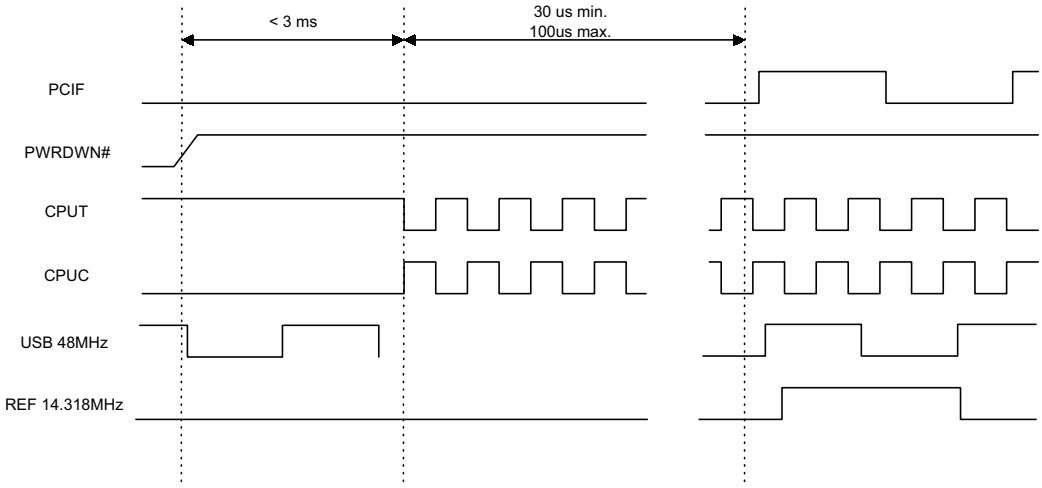
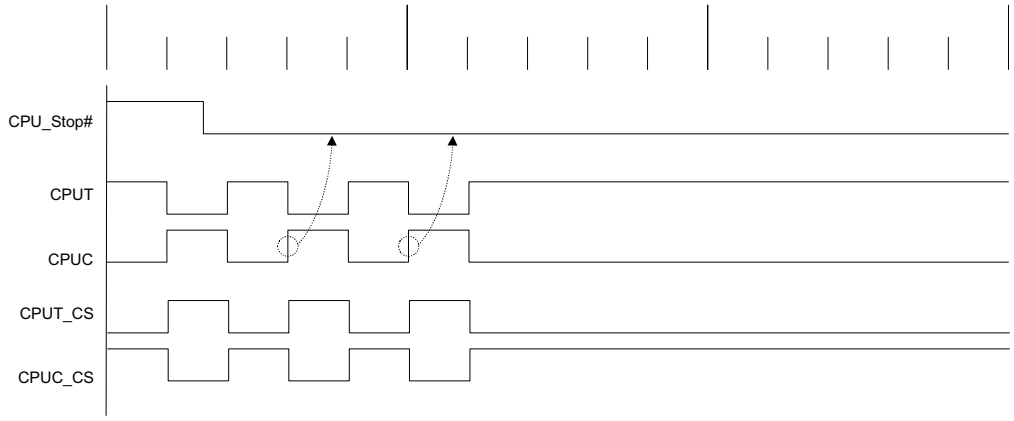
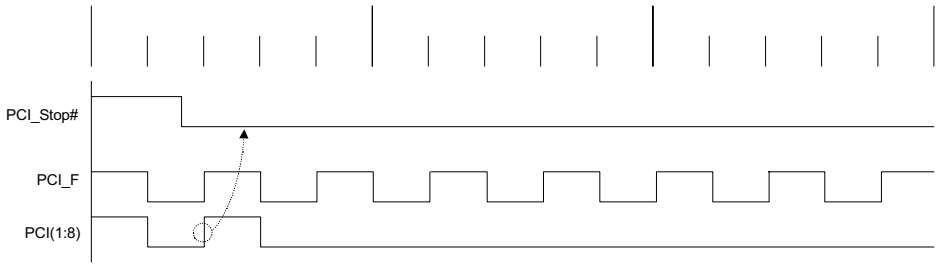


Figure: **Assertion CPU_Stop# Waveforms**



Note: CPU_STOP# assertion will stop all CPU outputs.

Figure: **Assertion PCI_Stop# Waveforms**



Note: PCI_F left free-running after PCI_STOP# assertion.

I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Serial Bits Reading	The serial bits will be read or sent by the clock driver in the following order Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in **Write Mode:** the **Command Byte** and **Byte Count Byte must be sent by the master** but ignored by the slave, in **Read Mode:** the **Byte Count Byte** will be **read by the master** then all other **Data Byte**.							

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	FS3 (see Frequency selection Table)
Bit 6	-	0	FS2 (see Frequency selection Table)
Bit 5	-	0	FS1 (see Frequency selection Table)
Bit 4	-	0	FS0 (see Frequency selection Table)
Bit 3	-	0	Frequency selection control bit 1=Via I2C, 0=Via External jumper
Bit 2	-	0	FS4 (see Frequency selection Table)
Bit 1	-	1	0 = OFF, 1 = Spread Spectrum Enable
Bit 0	-	0	0 = Normal, 1 = Tristate Mode for all outputs

2. BYTE 1: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	41,42	1	Enables/disables CPUT_CS, CPUC_CS. When disabled, defaults to CPUT_CS = 0 and CPUC_CS = 1
Bit 6	34,35	1	Enables/disables CPUT1, CPUC1. When disabled, defaults to CPUT1 = 1 and CPUC1 = 0
Bit 5	39,40	1	Enables/disables CPUT0, CPUC0. When disabled, defaults to CPUT0 = 1 and CPUC0 = 0
Bit 4	41,42	0	Reflects inverted MULT_SEL1 value latched at power-up (Read only)
Bit 3	-	X	Reflects inverted FS3 value latched at power-up (Read only)
Bit 2	-	X	Reflects inverted FS2 value latched at power-up (Read only)
Bit 1	-	X	Reflects inverted FS1 value latched at power-up (Read only)
Bit 0	-	X	Reflects inverted FS0 value latched at power-up (Read only)

3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	21	1	PCI7 (Active/Inactive)
Bit 6	19	1	PCI6 (Active/Inactive)
Bit 5	18	1	PCI5 (Active/Inactive)
Bit 4	17	1	PCI4 (Active/Inactive)
Bit 3	15	1	PCI3 (Active/Inactive)
Bit 2	14	1	PCI2 (Active/Inactive)
Bit 1	12	1	PCI1 (Active/Inactive)
Bit 0	11	1	PCI0 (Active/Inactive)

4. BYTE 3: AGP AND APIC Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	7	1	Enables/disables 48MHz
Bit 6	8	1	Enables/disables 24_48MHz
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	1	1	Enables/disables REF
Bit 2	-	0	Reserved
Bit 1	10	1	Enables/disables PCI_F
Bit 0	1	X	Reflects SEL 24_48; 0 = 24MHz; 1 = 48MHz (Read-Only)

5. BYTE 4: Frequency Select Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	46	1	Enables/disables APIC0
Bit 3	45	1	Enables/disables APIC1
Bit 2	23	1	Enables/disables AGP0
Bit 1	26	1	Enables/disables AGP1
Bit 0	27	1	Enables/disables AGP2

6. BYTE 5: Reserved Register

Bit	Pin#	Default	Description
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

7. BYTE 6: Fall-back Frequency / Revision ID / Vendor ID Register

Bit	Pin#	Default	Description	
Bit 7	-	X	WDT Fall-back Frequency selection for FS4	Revision ID Bit3*
Bit 6	-	X	WDT Fall-back Frequency selection for FS3	Revision ID Bit2*
Bit 5	-	X	WDT Fall-back Frequency selection for FS2	Revision ID Bit1*
Bit 4	-	X	WDT Fall-back Frequency selection for FS1	Revision ID Bit0*
Bit 3	-	0	WDT Fall-back Frequency selection for FS0	Vendor ID Bit 3*
Bit 2	-	0	Vendor ID Bit 2*	
Bit 1	-	1	Vendor ID Bit 1*	
Bit 0	-	1	Vendor ID Bit 0*	

Note: *: Default value at power-up

8. BYTE 7: Linear Programming Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0*	Linear programming sign bit (0 is "+", 1 is "–")
Bit 6	-	0*	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0*	Linear programming magnitude bit 5
Bit 4	-	0*	Linear programming magnitude bit 4
Bit 3	-	0*	Linear programming magnitude bit 3
Bit 2	-	0*	Linear programming magnitude bit 2
Bit 1	-	0*	Linear programming magnitude bit 1
Bit 0	-	0*	Linear programming magnitude bit 0 (LSB)

Note: **This register will be initialized to 0 following WATCHDOG RESET**

9. BYTE 8: WATCHDOG TIMER / Device ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description	
Bit 7	-	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable	
Bit 6	-	0	Device ID Bit 6*	
Bit 5	-	0	Watchdog Time Interval Bit 5 (MSB)	Device ID Bit 5*
Bit 4	-	0	Watchdog Time Interval Bit 4	Device ID Bit 4*
Bit 3	-	0	Watchdog Time Interval Bit 3	Device ID Bit 3*
Bit 2	-	0	Watchdog Time Interval Bit 2	Device ID Bit 2*
Bit 1	-	0	Watchdog Time Interval Bit 1	Device ID Bit 1*
Bit 0	-	1	Watchdog Time Interval Bit 0 (LSB)	Device ID Bit 0*

Note: *: Default value at power-up.

PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL202-16 device incorporates SMART-BYTE ™ technology with a single byte programming via I2C. Detail of PLL202-16's dual mode frequency programming method is described below:

1. **ROM-table Frequency Programming:**

   The pre-defined 32 frequencies found in Frequency table can be accessed through 3 external jumpers.

2. **Micro-step Linear Frequency Programming:**

   CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency changes. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha * M$$

Where:
1. M is magnitude factor defined in I2C Byte 7.bit (0:6)
2. ± (sign bit) of M is defined in I2C Byte7.bit 7
3. α is a constant equal to 0.22.

FREQUENCY PROGRAMMING EXAMPLE:

1. **Procedures to program target CPU frequency to 108 Mhz:**

   A. Locate the closest CPU frequency from Frequency-ROM table: 107
   B. α = 0.22
   C. Solve M (Linear Magnitude factor) in integer:

$$M = (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha$$
$$= (108 - 107) / 0.22$$
$$= 4$$

   D. Program I2C register:

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
Sign	M6	M5	M4	M3	M2	M1	M0

Setting of M = +4 in I2C.BYTE 7

F_{CPU} = 107 + (0.22) * 4 = 107.88 (% of frequency increased vs. ROM Table = 0.822 %)
F_{PCI} = 35.67 * (1 + 0.822 %) = 35.96

BUILT-IN WATCHDOG TIMER (WDT)

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into "Hang-up" state within a reasonable period of time (or Watchdog time interval). While disabled, the watchdog time interval can be programmed between 0 and 63 seconds with increment of 1 second by setting the value of I2C.Byte8.Bit(5:0). Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL202-16 will start from predefined Fall-back Frequency (the value of I2C Byte6, bits(7:3)). If system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

Example usage:

1. System power-up at CPU= 66.6MHz where external jumpers are used.

2A. Switch to target CPU=100.0MHz frequency with following I2C register setting:

7	6	5	4	3	2	1	0		
0	0	0	0	0	0	0	0	M =0	Setting in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0		

7	6	5	4	3	2	1	0		
1	0	0	0	1	1	1	1	WD-Timer = 15s	Setting in I2C.BYTE8
ENB		T5	T4	T3	T2	T1	T0		

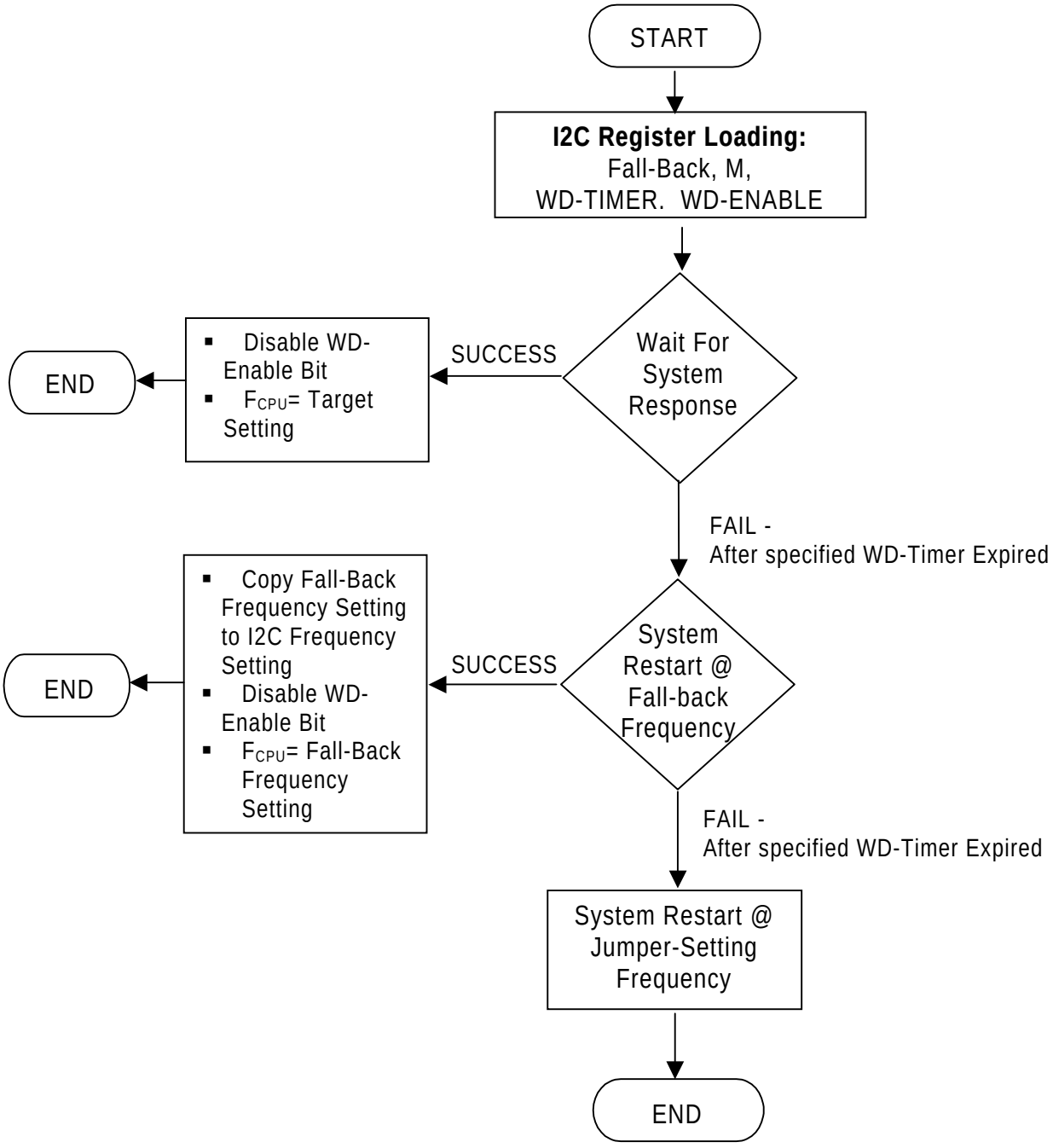
7	6	5	4	3	2	1	0		
0	0	0	0	1	0	0	0	FBSEL	Setting in I2C.BYTE6
FB4	FB3	FB2	FB1	FB0					

The fall-back frequency is set to the same location as that of FSEL since frequency switching between different timing groups will cause system to hang up. After WD timer expired or 15 seconds, the system will restart properly at target 100.0MHz if CPU is capable; otherwise WDT will perform another reset action to restart the system from 66.8 Mhz

2B. Switch to target CPU=78Mhz within the same timing Group

The fall-back frequency is recommended to set at the most safe and comfortable level to ensure a successful reboot such as 70 or 75.3 if system is unable to switch to 78Mhz.

WDT OPERATIONAL FLOW CHART



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC/AC Electrical Specifications

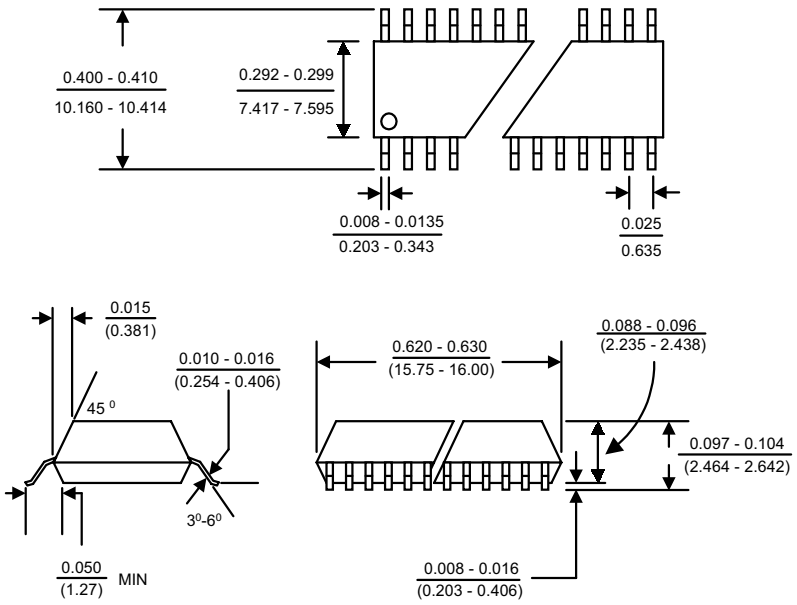
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	uA
Input Low Current	I_{IL1}	V_{IN}=0 with no pull-up resistor	-5			uA
Input Low Current	I_{IL2}	V_{IN}=0 with pull-up resistor	-200			
Supply Current	I_{DD}	C_L=0 pF@66MHz, 3.3V±5%			180	mA
	I_{DDL}	C_L=0 pF@133MHz, 3.3V±5%				
	I_{DD}	C_L=0 pF@66MHz, 2.5V±5%			72	
	I_{DDL}	C_L=0 pF@133MHz, 2.5V±5%			100	
Transition Time	T_{trans}	To 1st crossing of target Freq.			3	ms
Input frequency	F_I	V_{DD} = 3.3V	12	14.318	16	MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	XIN & XOUT pins	27	28	45	pF

2. DC/AC Electrical Specifications (continued)

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU	Measured @ 0.4V ~ 2.0V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 0.4V ~ 2.4V, C_L=10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 0.4V ~ 2.4V, C_L=10-30pf			2	
Output Fall time	T_{OF}	CPU	Measured @ 2.0 ~ 0.4V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 2.4V ~ 0.4V, C_L=10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 2.4V ~ 0.4V, C_L=10-30pf			2	
Duty Cycle	D_T	CPU,APIC,REF, 48MHz,24MHz	Measured @ 1.5V C_L=20pf	45	50	55	%
		PCI, AGP	Measured @ 1.5V, C_L=20~30pf	40		55	
Clock Skew	T_{SKEW}	CPU	Rising edge @ 1.25V, C_L=20pf			175	ps
		PCI	Rising edge @ 1.5V, C_L=30pf			500	
		AGP	Rising edge @ 1.5V, C_L=30pf			500	
Jitter(Cycle to Cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		REF	Measured @ 1.5V			500	
		PCI, AGP	Measured @ 1.5V			250	
Frequency Stabilization Time	T_{FST}	CPU,PCI_F,PCI, APIC,AGP,REF, 48MHz,24MHz	Assumes full supply voltage reached within 1ms from power-up. Short cycle exist prior to frequency stabilization.			3	ms
AC output impedance	Z_0	CPU	V_{DD}=3.3V(2.5V)±5%		20		ohm
		PCI,AGP	V_{DD}=3.3V±5%		30		
		REF,48MHz,24MHz	V_{DD}=3.3V±5%		40		

PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL202-16 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

***LIFE SUPPORT POLICY**: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.*