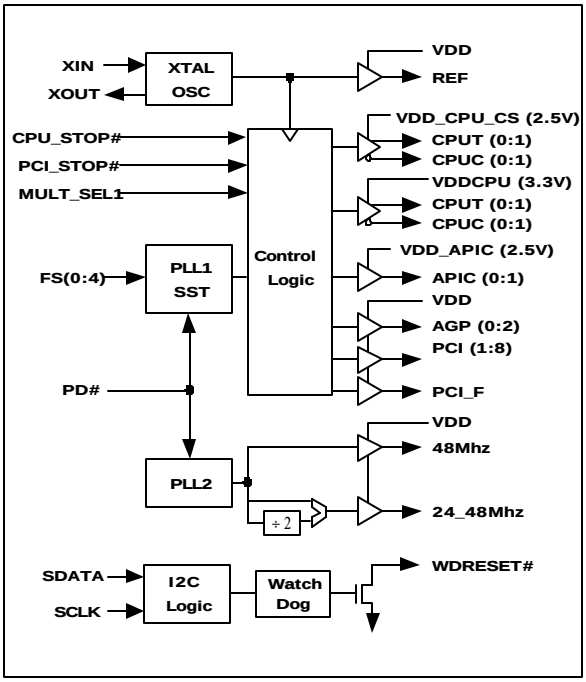
Programmable Clock Generator for VIA, ALI and SIS DDR SYSTEM

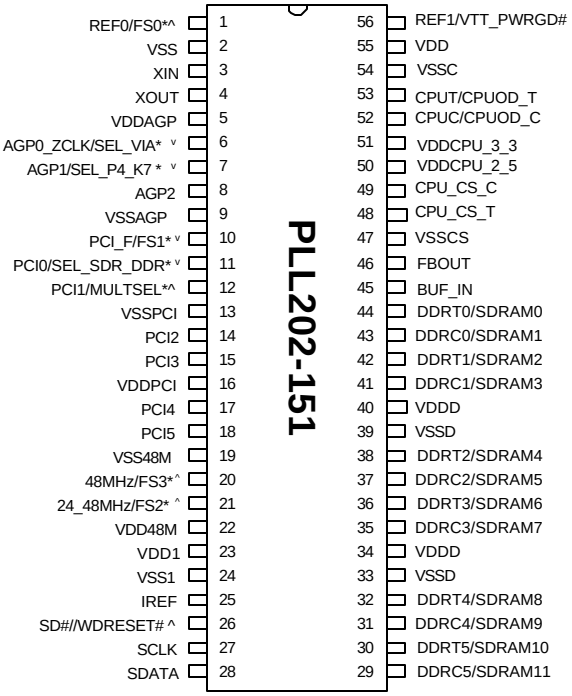
FEATURES

- Supports VIA P4M/KM266, ALI M1671 and SIS 645/650 Chipsets.
- Programmable Spread Spectrum Modulation from ±0.1% to ±1.5% with minimum step size of ±0.012%. Selectable either center or down.
- Selectable Spread Spectrum modulation profile.
- AccuSkew™, Programmable Precision skew tuning channel with maximum ±5% precision over the variation of temperature, process and voltage. Finest step starts with 80ps.
- AccuDrive™ Programmable Output Buffer drive strength with minimum 6mA per step. Selectable double strength drive for REF1, AGP0, PCI5.
- Programmable VCO frequency with one variable
- Programmable VCO Output Divider.
- On-chip 20 ohm series resistor for REF, PCI, USB, ZCLK and AGP clock outputs.
- 6 differential DDR pairs or 12 SDR clocks.
- 8 PCI, 1 USB, 2 REF and 3 AGP clock outputs.
- 1 programmable 24MHz or 48MHz for SIO.
- CPU frequency slow down to -30% if overheats.
- Support 2-wire I2C serial bus interface.
- Built-in programmable watchdog timer
- Available in 300 mil 56 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: ^: Pull up (100kΩ), v: Pull down (100kΩ), #: Active low, *: Bi-directional latched at power-up

POWER GROUP

- VDD, VSS: REF, XIN, XOUT, PLL ANALOG
- VDDPCI, VSSPCI: PCI
- VDDAGP, VSSAGP: AGP
- VDD48M, VSS48M: 48MHz
- VDDC, VSSC: CPUT/C
- VDDCS, VSSCS: CPUCS_T/C
- VDDD, VSSD: DDR(C:T 0:5)/SD(0:11)

KEY SPECIFICATIONS

- CPU Output Skew < 250ps.
- VIA Mode: CPU to AGP Skew < 250ps.
- Non-Via: CPU to AGP(ZCLK): 1 ~4 ns (typ 2ns)
- CPU to DDR/SDRAM Skew < 250ps.
- PCI to PCI Skew < 500ps.
- CPU to PCI : Min = 1.0ns, Typ = 2.0ns, Max = 4.0ns.

PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	3	I	14.318Mhz crystal input to be connected to one end of the crystal
XOUT	4	O	14.318Mhz crystal output
REF0/FS0	1	B	14.318Mhz Reference clock output. This pin latch FS0 value at power-up. (See Frequency Selection table). It has an internal pull up resistor and 20 ohm on-chip series resistor.
REF1/Vtt_PWRGD#	56	B	If SEL_K7_P4 = 1 (P4 mode), this 3.3V LVTTL input is a level sensitive strobe at power up used to determine when FS (0:3) and MULT_SEL1 inputs are valid and all outputs are enable when input is transited to a logic low. If SEL_K7_P4 = 0 (K7 mode), this input is ignored. This REF1 has I2C programmable double drive strength and it has a 20 ohm on-chip series resistor.
DDRT[0:5]/ SDRAM[0,2,4,6,8,10]	44,42,38, 36,32,30	O	In VIA Mode: If SEL_SDR_DDR=0, these outputs provide DDR clock outputs, copies of BUFIN signals; If SEL_SDR_DDR=1, these outputs provide SDRAM clock outputs, copies of BUFIN signals. In ALI_SIS Mode: If SEL_SDR_DDR=0, these outputs provide DDR clock outputs generating from internal PLL. If SEL_SDR_DDR=1, these outputs provide SDRAM clock outputs generating from internal PLL
DDRC[0:5]/ SD[1,3,5,7,9,11]	43,41,37, 35,31,29	O	In VIA Mode: If SEL_SDR_DDR=0, these outputs provide DDR clock outputs, complementary copies of BUFIN signals; If SEL_SDR_DDR=1, these outputs provide SDRAM clock outputs, copies of BUFIN signals. In ALI_SIS Mode: If SEL_SDR_DDR=0, these outputs provide DDR clock outputs generating from internal PLL. If SEL_SDR_DDR=1, these outputs provide SDRAM clock outputs generating from internal PLL
AGP1/SEL_K7_P4	7	B	This pin latches SEL_K7_P4 value at power-up. After power-up, the pin acts as AGP1 clock output. When SEL_K7_P4=1, it sets to P4 mode. SEL_K7_P4=0 in K7 mode. This pin has an internal pull-down resistor and a 20 ohm on-chip series resistor.
PCI1/MULTSEL	12	I/O	This pin latches the MULTSEL value at power-up. After power-up, this pin acts as PCI2 clock output. MULTSEL is used to select the current multiplier for the CPU outputs. This pin has a 20 ohm on-chip series resistor. If MULTSEL=0, IOH=4XIREF. If MULTSEL=1, IOH=6XIREF

PIN DESCRIPTIONS (Continue)

Name	Number	Type	Description
CPU[T,C]/ CPU0D_[T,C]	52,53	O	In P4 mode, these two pins are differential signals of CPUT and CPUC In K7 mode, these two pins are differential open drain outputs of CPUODT and CPUODC.
PCI_F/FS1	10	B	Bi-directional pin. At power-up, the FS1 input value is latched. After power-up, this pin acts as PCI_F output. It has an internal pull-down and a 20 ohm on-chip series resistor.
48MHz/FS3	20	B	Bi-directional pin. At power-up, the FS3 input value is latched. After power-up, this pin acts as 48MHz output. It has an internal pull-down and a 20 ohm on-chip series resistor.
PCI0/ SEL_SDR_DDR	11	B	Bi-directional pin. At power-up, the SEL_SDR_DDR input value is latched. After power-up, this pin acts as PCI0 output. It has an internal pull-down and a 20 ohm on-chip series resistor. If SEL_SDR_DDR=0, DDR mode is selected If SEL_SDR_DDR=1, SDRAM mode is selected.
PCI[2:5]	14,15,17,18	O	PCI clock output (see Frequency table) with a 20 ohm on-chip series resistor. PCI5 has I2C programmable double drive strength.
24_48MHz/FS2	21	B	Bi-directional pin. At power-up, the FS2 input value is latched. After power-up, this pin acts as 24_48MHz output. It has an internal pull-up and a 20 ohm on-chip series resistor. The selection of 24_48MHz is via I2C on Byte3 bit6. It will generate 48MHz as power on default.
AGP0_ZCLK/SEL_VIA	6	B	Bi-directional pin. At power-up, the SEL_VIA input value is latched. After power-up, this pin acts as AGP0_ZCLK clock output. It has an internal pull-down and a 20 ohm on-chip series resistor with I2C programmable double drive strength. If SEL_VIA=0, VIA mode is selected. If SEL_VIA=1, ALI_SIS mode is selected.
AGP2	8	O	AGP2 clock output. It has a 20 ohm on-chip series resistor.
Iref	25	I	This pin establishes the reference current for the CPU differential pairs, it requires a fixed precision resistor tied to ground in order to establish the appropriate current.
SDATA	28	B	Serial data inputs for serial interface port.
SCLK	27	I	Serial data inputs for serial interface port.
SD#//WDRESET#	26	B	When Byte 10 bit 7 is 1, this pin generates Watchdog timer reset signal after timer expires. By default, this input pin acts as Slow Down function to smoothly reduce output frequency by 15~30% depends on internal VCO divider when SD#=0.
BUF_IN	45	I	In VIA mode, 3.3V CMOS input for SDRAM mode; 2.5V input for DDR mode. In ALI_SIS mode, this input should be connected to ground.
FB_OUT	46	O	Feedback clock for chipset. Output voltage depends on VDDD.

PIN DESCRIPTIONS (Continue)

Name	Number	Type	Description
VDDPCI	16	P	3.3V Power Supply for PCIF, PCI[1:6] clock
VDDAGP	5	P	3.3V Power Supply for AGP clock.
VDD48M	22	P	3.3V Power Supply for 48MHz and 24_48MHz clock
VDD	55	P	3.3V power for internal PLL and REF outputs.
VDD1	23	P	3.3V power for I2C Inputs.
VDDCPU_2_5	50	P	2.5v power supply for CPUCS_[T,C] clocks.
VDDCPU_3_3	51	P	3.3v power supply for CPU[T,C]/CPUOD_[T,C] clocks.
VDDD	34,40	P	If SEL_SDR_DDR=0 supply DDR at 2.5V, If SELSDR_DDR=1 supply SDRAM at 3.3V
VSS	9,13,54,33, 39,19,47,24	P	Ground.

HOST SWING SELECT FUNCTIONS

MULTISEL0	Board Target Trace/Term Z	Reference R (Rr) I_{ref} = VDD/(3*Rr)	Output Current	V_{oh} @ Z
0	50Ω	Rr = 221Ω; 1% Iref = 5.0mA	I_{oh} = 4*IREF	1.0V @ 50Ω
1	50Ω	Rr = 475Ω; 1% Iref = 2.32 mA	I_{oh} = 6*IREF	0.7V @ 50Ω

FREQUENCY (MHz) SELECTION TABLE

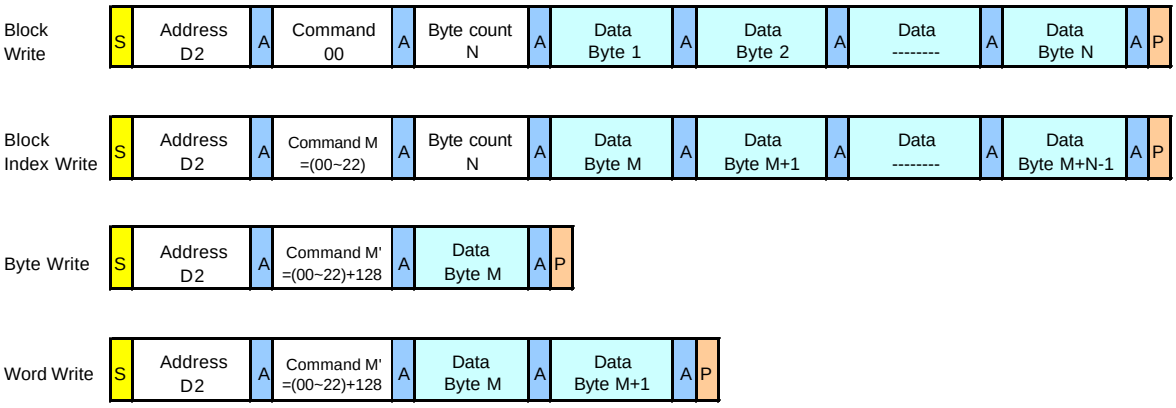
SEL_VIA Mode	FS3	FS2	FS1	FS0	CPU	DDR SDRAM	ZCLK	AGP	PCI	VCO	N
0	0	0	0	0	66.7	66.7	66.7	66.7	33.3	400	28,609
0	0	0	0	1	100	100	66.7	66.7	33.3	400	28,607
0	0	0	1	0	100	100	80	66.7	33.3	400	28,607
0	0	0	1	1	100	133.3	66.7	66.7	33.3	400	28,607
0	0	1	0	0	100	133.3	80	66.7	33.3	400	28,607
0	0	1	0	1	100	160	66.7	66.7	33.3	800	57,214
0	0	1	1	0	100	166.7	62.5	62.5	31.3	500	35,759
0	0	1	1	1	100	166.7	71.4	83.3	41.7	500	35,759
0	1	0	0	0	100	166.7	83.3	62.5	31.3	500	35,759
0	1	0	0	1	100.9	134.5	67.3	67.3	33.6	403.6	28,865
0	1	0	1	0	105	140	70	70	35	420	30,038
0	1	0	1	1	133.3	100	66.7	66.7	33.3	400	28,607
0	1	1	0	0	133.3	133.3	66.7	66.7	33.3	800	57,213
0	1	1	0	1	133.3	160	80	66.7	33.3	800	57,213
0	1	1	1	0	133.3	160	100	66.7	33.3	800	57,213
0	1	1	1	1	133.3	166.7	66.7	66.7	33.3	666.6	47,678
1	0	0	0	0	160	N/A		80	40	640	45,772
1	0	0	0	1	164			82	41	656	46,916
1	0	0	1	0	166.6			66.6	33.3	333.3	23,840
1	0	0	1	1	170			68	34	340	24,316
1	0	1	0	0	175			70	35	350	25,032
1	0	1	0	1	180			72	36	360	25,747
1	0	1	1	0	185			74	37	370	26,462
1	0	1	1	1	190			76	38	380	27,177
1	1	0	0	0	111			74	37	444	31,754
1	1	0	0	1	120			80	40	480	34,329
1	1	0	1	0	144			72	36	576	41,195
1	1	0	1	1	156			78	39	624	44,627
1	1	1	0	0	66.6			66.6	33.3	533	38,145
1	1	1	0	1	100			66.6	33.3	400	28,607
1	1	1	1	0	200			66.6	33.3	400	28,607
1	1	1	1	1	133.3			66.6	33.3	533	38,142

Note: SEL_VIA available through jumper setting only

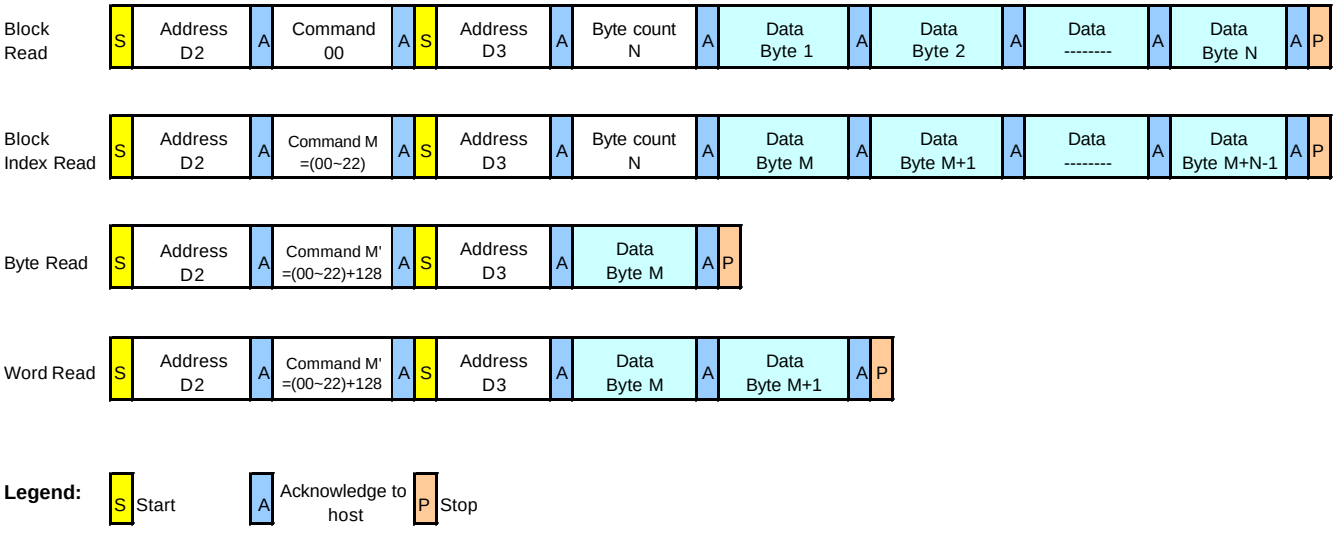
I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	This serial interface is designed to allow multiple protocols to write and read from the controller. It includes Block Read/Write, Block Index Read/Write, Byte Read/Write and Word Read/Write. In general, the bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).							

WRITE MODE



READ MODE



Legend: S Start | A Acknowledge to host | P Stop

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	20	Power-up Latched FS3:FS0 value	FS3
Bit 6	21		FS2
Bit 5	10		FS1
Bit 4	1		FS0
Bit 3	-	0	Frequency selection bit 1=Via I2C, 0=Via External jumper
Bit 2	-	0	Spread Spectrum modulation amplitude selection. 0= ±0.3% (center) 1= ±0.6% (center)
Bit 1	-	1	0=normal, 1= Spread Spectrum Enable
Bit 0	-	0	(Reserved).

2. BYTE 1: CPU clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	29	1	DDRC5/SDRAM11 (1=Active 0=Inactive)
Bit 6	10	1	PCI_F (1=Active 0=Inactive)
Bit 5	30	1	DDRT5/SDRAM10 (1=Active 0=Inactive)
Bit 4	31	1	DDRC4/SDRAM9 (1=Active 0=Inactive)
Bit 3	-	1	MULTSEL (IREF multiple) MODE Selection. 1= selection through hardware input pin 38 0= selection through I2C control by Byte2.bit[0,7]
Bit 2	32	1	DDRT4/SDRAM8 (1=Active 0=Inactive)
Bit 1	52,53	1	CPUT/CPU0D_T, CPUC/CPU0D_C (1=Active 0=Inactive)
Bit 0	48,49	1	CPU_CS_T, CPU_CS_C (1=Active 0=Inactive)

3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	MULTSEL1	1	IREF Multiplier setting, bit [0,7] 00= 4xIREF 01= 5xIREF 10= 6xIREF 11= 7xIREF
Bit 6	18	1	PCI5 (1=Active 0=Inactive)
Bit 5	17	1	PCI4 (1=Active 0=Inactive)
Bit 4	15	1	PCI3 (1=Active 0=Inactive)
Bit 3	14	1	PCI2 (1=Active 0=Inactive)
Bit 2	12	1	PCI1 (1=Active 0=Inactive)
Bit 1	11	1	PCI0 (1=Active 0=Inactive)
Bit 0	MULTSEL0	1	IREF Multiplier setting. See Bit 7.

4. BYTE 3: AGP Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	46	1	FBOUT (1=Active 0=Inactive)
Bit 6	21	1	24_48MHZ selection. 0=24Mhz, 1=48Mhz
Bit 5	56	1	REF1 double drive strength selection. 1=normal, 0=2X
Bit 4		1	REF1 (1=Active 0=Inactive)
Bit 3	8	1	AGP0_ZCLK double drive strength selection. 1=normal, 0=2X
Bit 2		1	AGP2 (1=Active 0=Inactive)
Bit 1	7	1	AGP1 (1=Active 0=Inactive)
Bit 0	6	1	AGP0 (1=Active 0=Inactive)

5. BYTE 4: REF Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS3 value (Read only)
Bit 6	-	X	Inverted Power-up latched FS2 value (Read only)
Bit 5	-	X	Inverted Power-up latched FS1 value (Read only)
Bit 4	-	X	Inverted Power-up latched FS0 value (Read only)
Bit 3	20	1	48Mhz (1=Active 0=Inactive)
Bit 2	21	1	24_48Mhz (1=Active 0=Inactive)
Bit 1	-	1	PCI5 double drive strength selection. 1=normal, 0=2X
Bit 0	1	1	REF0 (1=Active 0=Inactive)

6. BYTE 5: DDR/SDR Clock Register

Bit	Pin#	Default	Description
Bit 7	35	1	DDRC3/SDRAM7 (1=Active 0=Inactive)
Bit 6	36	1	DDRT3/SDRAM6 (1=Active 0=Inactive)
Bit 5	37	1	DDRC2/SDRAM5 (1=Active 0=Inactive)
Bit 4	38	1	DDRT2/SDRAM4 (1=Active 0=Inactive)
Bit 3	41	1	DDRC1/SDRAM3 (1=Active 0=Inactive)
Bit 2	42	1	DDRT1/SDRAM2 (1=Active 0=Inactive)
Bit 1	43	1	DDRC0/SDRAM1 (1=Active 0=Inactive)
Bit 0	44	1	DDRT0/SDRAM0 (1=Active 0=Inactive)

7. BYTE 6: Vendor ID and Revision ID Register

Bit	Pin#	Default	Description
Bit 7	-	0	Revision ID Bit 3 (read only)
Bit 6	-	0	Revision ID Bit 2 (read only)
Bit 5	-	0	Revision ID Bit 1 (read only)
Bit 4	-	0	Revision ID Bit 0 (read only)
Bit 3	-	0	Vendor ID Bit 3 (read only)
Bit 2	-	0	Vendor ID Bit 2 (read only)
Bit 1	-	1	Vendor ID Bit 1 (read only)
Bit 0	-	1	Vendor ID Bit 0 (read only)

8. BYTE 7: Linear Programming Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Linear programming sign bit (0 is “+”, 1 is “–”)
Bit 6	-	0	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0	Linear programming magnitude bit 5
Bit 4	-	0	Linear programming magnitude bit 4
Bit 3	-	0	Linear programming magnitude bit 3
Bit 2	-	0	Linear programming magnitude bit 2
Bit 1	-	0	Linear programming magnitude bit 1
Bit 0	-	0	Linear programming magnitude bit 0 (LSB)

9. BYTE 8: Byte Count Read back Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	This register will determine the number of byte counts to be read back.
Bit 6	-	0	
Bit 5	-	0	
Bit 4	-	0	
Bit 3	-	1	
Bit 2	-	1	
Bit 1	-	1	
Bit 0	-	1	

10. BYTE 9: WATCHDOG Fall Back Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Watchdog Timer Unit Bit[7:6]: 00 = 250 ms, 01 = 500ms, 10 = 1s, 11 = 4s
Bit 6	-	0	
Bit 5	-	0	Initialization setting for Linear Programming Byte after Watch dog reset. 0= Byte 7 initialized to 0 after WD-Reset generated. 1= Byte 7 unchanged after WD-Reset generated.
Bit 4	-	0	Reserved
Bit 3	-	0	WDT Fall-back Frequency selection for FS3
Bit 2	-	0	WDT Fall-back Frequency selection for FS2
Bit 1	-	0	WDT Fall-back Frequency selection for FS1
Bit 0	-	0	WDT Fall-back Frequency selection for FS0

11. BYTE 10: WATCHDOG TIMER Register (1=Enable, 0=Disable)

Bit	Name	Default	Description
Bit 7	WDT ENB	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable
Bit 6	-	0	0=Watch Dog falls back to hardware jumper setting frequency 1=Watch Dog falls back to fall back frequency setting in Byte 9.
Bit 5	WDT<5>	0	Watchdog Time Interval Bit 5 (MSB)
Bit 4	WDT<4>	0	Watchdog Time Interval Bit 4
Bit 3	WDT<3>	0	Watchdog Time Interval Bit 3
Bit 2	WDT<2>	0	Watchdog Time Interval Bit 2
Bit 1	WDT<1>	0	Watchdog Time Interval Bit 1
Bit 0	WDT<0>	0	Watchdog Time Interval Bit 0 (LSB)

12. BYTE 11: Programming Mode Counter Register (1=Enable, 0=Disable)

Bit	Name	Default	Description
Bit 7	-	0	Reserved
Bit 6	-	0	Initialization setting for Skew Control and Buffer drive strength registers after Watch dog reset. 0= Byte 13~19 initialized to 0 after WD-Reset generated. 1= Byte 13~19 unchanged after WD-Reset generated.
Bit 5	WDT Status	0	Watch Dog Timer Status info (read only)
Bit 4			
Bit 3	SST Profile	0	0= linear, 1= non-linear
Bit 2	Accu-SST Enable	0	Accu-SST programming Enable: 1= via I2C Byte12, 0= via ROM setting
Bit 1	Skew Enable	0	Enable Accu-Skew programming (byte13~15). 1=enable, 0=disable
Bit 0	VCO-N Enable	0	Enable VCO-N Counter programming (byte23~24) 1= programming through byte 23~24 0= programming through ROM selection

13. BYTE 12: Accu-Spread Spectrum Modulation Amplitude Programming Register:

Bit	NAME	Default	Description
Bit 7	-	1	Spread Spectrum mode selection. 1=Center Spread, 0= Down Spread
Bit 6	SST6	1	1. Center Spread: SST<6:0> = Modulation rate * N /7 2. Down Spread: SST<6:0> = Modulation rate * N /14
Bit 5	SST5	1	
Bit 4	SST4	1	
Bit 3	SST3	1	
Bit 2	SST2	1	
Bit 1	SST1	1	
Bit 0	SST0	1	

TABLE 1: Output Signals SKEW Programming Summary:

Bit<2:0>	AccuSkew Setting I (±80ps/step)		AccuSkew Setting II (±160ps/step)		Skew Setting III (125ps/step)	
111	+320ps	Setting applies to the following outputs: 1. CPU-Host 2. CPU-CS 3. DDR/SDRAM (non-VIA)	+640ps	Setting applies to the following outputs: 1. AGP0_ZCLK 2. AGP1, AGP2 3. All PCI	+875ps	Setting applies to the following outputs: 1.DDR/SDRAM (Via mode)
110	+240ps		+480ps		+750ps	
101	+160ps		+320ps		+625ps	
100	+80ps		+160ps		+500ps	
011	Default		Default		+375ps	
010	-80ps		-160ps		+250ps	
001	-160ps		-320ps		+125ps	
000	-240ps		-480ps		Default	

Bit<3:0>	Skew Setting IV (125ps/step)	
1111	+1,875ps	Setting applies to the following outputs 1. FBOUT (VIA mode)
1110	+1,750ps	
1101	+1,625ps	
1100	+1,500ps	
1011	+1,375ps	
1010	+1,250ps	
1001	+1,125ps	
1000	+1,000ps	
0111	+875ps	
0110	+750ps	
0101	+625ps	
0100	+500ps	
0011	+375ps	
0010	+250ps	
0001	+125ps	
0000	Default	

14. SKEW Control Register (1=Enable, 0=Disable)

Byte #	Bit	Name		Def	Description
Byte 13	Bit 7	Skew CPU Host	Bit <2>	0	These three bits will adjust timing of CPU_Host signals (CPUT/CPUC) either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
	Bit 6		Bit <1>	1	
	Bit 5		Bit <0>	1	
	Bit 4	Skew CPU CS	Bit <2>	0	These three bits will adjust timing of CPU_chip_sets signals (CPU_CS_T/CPU_CS_C) either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
	Bit 3		Bit <1>	1	
	Bit 2		Bit <0>	1	
	Bit 1	Skew DDR/SDRAM (non-VIA mode)	Bit <2>	0	These three bits will adjust timing of DDR/SDRAM signals in non-VIA mode either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
	Bit 0		Bit <1>	1	
Byte 14	Bit 7		Bit <0>	1	
	Bit 6	Skew DDR/SDRAM (VIA mode)	Bit <2>	0	These three bits will adjust timing of DDR/SDRAM signals in VIA buffer mode either positive or negative delay up to +500ps or –375ps with ±125ps per step.
	Bit 5		Bit <1>	1	
	Bit 4		Bit <0>	1	
	Bit 3	Skew FBOUT (VIA mode)	Bit <3>	0	These four bits will adjust timing of FBOUT signal in VIA buffer mode either positive or negative delay up to +1000ps or –875ps with ±125ps per step.
	Bit 2		Bit <2>	1	
	Bit 1		Bit <1>	1	
	Bit 0		Bit <0>	1	
Byte 15	Bit 7	Skew AGP0_ZCLK	Bit <2>	0	These three bits will adjust timing of AGP0_ZCLK either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
	Bit 6		Bit <1>	1	
	Bit 5		Bit <0>	1	
	Bit 4	Skew AGP[1:2]	Bit <2>	0	These three bits will adjust timing of AGP1 and AGP2 either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
	Bit 3		Bit <1>	1	
	Bit 2		Bit <0>	1	
	Bit 1	Skew PCI	Bit <2>	0	These three bits will adjust timing of all PCI signals either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
	Bit 0		Bit <1>	1	
Byte 16	Bit 7		Bit <0>	1	

TABLE 2: Output Drive Strength Programming Summary:

Bit<2:0>	Setting I		Setting II		Setting III	
111	+50%	Setting applies to the following outputs 1. CPU-CS 2. DDR[0:2] 3. DDR[3:5] 4. FBOUT	+40%	Setting applies to the following outputs 1. AGP0_ZCLK 2. AGP[1:2] 3. 48M, 24_48MHz	+50%	Setting applies to the following outputs 1. PCIF,PCI[0:1] 2. PCI[2:5] 3. REF[0:1]
110	+38%		+30%		+38%	
101	+25%		+20%		+25%	
100	+12%		+10%		+13%	
011	Default		Default		Default	
010	-12%		-10%		-13%	
001	-25%		-20%		-25%	
000	-38%		-30%		-38%	

Bit<0>	Setting IV	
1	+30%	1. CPU-Host (K7 mode)
0	Default	

15. Buffer Strength Control Register:

Byte #	Bit	Name		Def	Description
Byte 16	Bit 6	CPU Host Strength	Bit <0>	0	This bit will allow drive strength to increase 30% for CPUT/CPUC in K7 mode.
	Bit 5	CPU CS Strength	Bit <2>	0	These three bits will program drive strength for CPU_CS_C and CPU_CS_T output clocks (see Table 2).
	Bit 4		Bit <1>	1	
	Bit 3		Bit <0>	1	
	Bit 2	DDR[0:2] Strength	Bit <2>	0	These three bits will program drive strength for DDR[0:2]C, DDR[0:2]T output clocks (see Table 2).
	Bit 1		Bit <1>	1	
	Bit 0		Bit <0>	1	
Byte 17	Bit 7	DDR[3:5] Strength	Bit <2>	0	These three bits will program drive strength for DDR[3:5]C, DDR[3:5]T output clocks (see Table 2).
	Bit 6		Bit <1>	1	
	Bit 5		Bit <0>	1	

16. Buffer Strength Control Register (continued):

Byte #	Bit	Name		Def	Description
Byte 17	Bit 4	AGP0_ZCLK Strength	Bit <2>	0	These three bits will program drive strength for AGP0_ZCLK output clock (see Table 2).
	Bit 3		Bit <1>	1	
	Bit 2		Bit <0>	1	
	Bit 1	AGP[1:2] Strength	Bit <2>	0	These three bits will program drive strength for AGP1 and AGP2 output clocks (see Table 2).
	Bit 0		Bit <1>	1	
Byte 18	Bit 7		Bit <0>	1	
	Bit 6	USB Strength	Bit <2>	0	These three bits will program drive strength for 48Mhz and 24_48Mhz output clocks (see Table 2).
	Bit 5		Bit <1>	1	
	Bit 4		Bit <0>	1	
	Bit 3	PCIF,PCI[0:1] Strength	Bit <2>	0	These three bits will program drive strength for PCI_F, PCI0, PCI1 output clocks. (see Table 2).
	Bit 2		Bit <1>	1	
	Bit 1		Bit <0>	1	
	Bit 0	PCI[2:5] Strength	Bit <2>	0	These three bits will program drive strength for PCI[2:5] output clocks. (see Table 2).
Byte 19	Bit 7		Bit <1>	1	
	Bit 6		Bit <0>	1	
	Bit 5	REF[0:1] Strength	Bit <2>	0	These three bits will program drive strength for REF[0:1] output clocks. (see Table 2).
	Bit 4		Bit <1>	1	
	Bit 3		Bit <2>	1	
	Bit 2	FBOUT Strength	Bit <2>	0	These three bits will program drive strength for FBOUT output clock. (see Table 2).
	Bit 1		Bit <1>	1	
	Bit 0		Bit <0>	1	

TABLE 3: VCO Divider Programming Summary:

Bit<2:0>	CPU-Divider		AGP-Divider		PCI-Divider	
111	Default ROM Selection	1. CPU-Host 2. CPU-CS 3. DDR/SDRAM	Default ROM Selection	1. AGP0_ZCLK 2. AGP[1:2]	Default ROM Selection	1. PCI
110	/8		/12		/24	
101	/7		/10		/20	
100	/6		/8		/16	
011	/5		/7		/14	
010	/4		/6		/12	
001	/3		/5		/10	
000	/2		/4		/8	

17. VCO Divider Control Register:

Byte #	Bit	Name		Default	Description
Byte 20	Bit 7	-		1	Reserved
	Bit 6	-		1	Reserved
	Bit 5	CPU-Host Divider	Bit <2>	1	These three bits will program output frequency for CPU_T and CPU_C clocks (see Table 3).
	Bit 4		Bit <1>	1	
	Bit 3		Bit <0>	1	
	Bit 2	CPU-CS Divider	Bit <2>	1	These three bits will program output frequency for CPU_CS_C and CPU_CS_T clocks (see Table 3).
	Bit 1		Bit <1>	1	
	Bit 0		Bit <0>	1	
Byte 21	Bit 7	-		1	Reserved
	Bit 6	-		1	Reserved
	Bit 5	DDR/SDRAM Divider	Bit <2>	1	These three bits will program all output frequency for DDR/SDRAM clocks (see Table 3).
	Bit 4		Bit <1>	1	
	Bit 3		Bit <0>	1	
	Bit 2	AGP0_ZCLK Divider	Bit <2>	1	These three bits will program output frequency for AGP0_ZCLK clock (see Table 3).
	Bit 1		Bit <1>	1	
	Bit 0		Bit <0>	1	

18. VCO Divider Control Register (Continued):

Byte #	Bit	Name		Default	Description
Byte 22	Bit 7	-		1	Reserved
	Bit 6	-		1	Reserved
	Bit 5	AGP[1:2] Divider	Bit <2>	1	These three bits will program output frequency for AGP1 and AGP2 clocks (see Table 3).
	Bit 4		Bit <1>	1	
	Bit 3		Bit <0>	1	
	Bit 2	PCI Divider	Bit <2>	1	These three bits will program output frequency for all PCI clocks (see Table 3).
	Bit 1		Bit <1>	1	
	Bit 0		Bit <0>	1	

19. BYTE 23: VCO N Counter Register:

Bit	Name	Default	Description
Bit 7	N<15>	1	N<15:0>= VCO*1024/14.31818
Bit 6	N<14>	1	
Bit 5	N<13>	1	
Bit 4	N<12>	1	
Bit 3	N<11>	1	
Bit 2	N<10>	1	
Bit 1	N<9>	1	
Bit 0	N<8>	1	

20. BYTE 24: VCO N Counter Register

Bit	Name	Default	Description
Bit 7	N<7>	1	N<15:0>= VCO*1024/14.31818
Bit 6	N<6>	1	
Bit 5	N<5>	1	
Bit 4	N<4>	1	
Bit 3	N<3>	1	
Bit 2	N<2>	1	
Bit 1	N<1>	1	
Bit 0	N<0>	1	

PROGRAMMING OF CPU FREQUENCY Using Smart-Byte:

To simplify traditional loop counter setting, the PLL202-151 device incorporates SMART-BYTE ™ technology with a single byte programming via I2C. Detail of PLL202-151's dual mode frequency programming method is described below:

1. ROM-table Frequency Programming:

   The pre-defined 32 frequencies found in Frequency table can be accessed through 4 external jumpers.

2. Micro-step Linear Frequency Programming:

   CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency changes. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha * M$$

Where:
1. M is magnitude factor defined in I2C Byte 7.bit (0:6)
2. ± (sign bit) of M is defined in I2C Byte7.bit 7
3. α is a constant equal to 0.9/(CPUDivider) ranging from 0.11~0.45.

FREQUENCY PROGRAMMING EXAMPLE:

1. Procedures to program target CPU frequency to 110 Mhz:

   A. Locate the closest CPU frequency from Frequency-ROM table: 100 (‘0001)
   B. VCO=400, CPU=100, CPUDivider=400/100=4, α = (0.9/4)= 0.225
   C. Solve M (Linear Magnitude factor) in integer:

$$M = (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha$$
$$= (110 - 100) / 0.225$$
$$= 44$$

   D. Program I2C register:

7	6	5	4	3	2	1	0
0	0	1	0	1	1	0	0
Sign	M6	M5	M4	M3	M2	M1	M0

Setting of M = +44 in I2C.BYTE 7

F_{CPU} = 100 + (0.225) * 44 = 109.9 (% of frequency increased vs. ROM Table = 9.9 %)
F_{PCI} = 33.3 * (1 + 1.83 %) = 36.6

BUILT-IN WATCHDOG TIMER (WDT)

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into "Hang-up" state within a reasonable period of time (or Watchdog time interval). While disabled, the watchdog time interval can be programmed between 0 and 63 seconds with increment of 1 second by setting the value of I2C.Byte10.Bit(5:0). Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL202-151 will start from predefined Fall-back Frequency (the value of I2C Byte9, bits(5:3)). If system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

Example usage:

1. System power-up at CPU= 66.6MHz where external jumpers are used.

2A. Switch to target CPU=100.0MHz frequency with following I2C register setting:

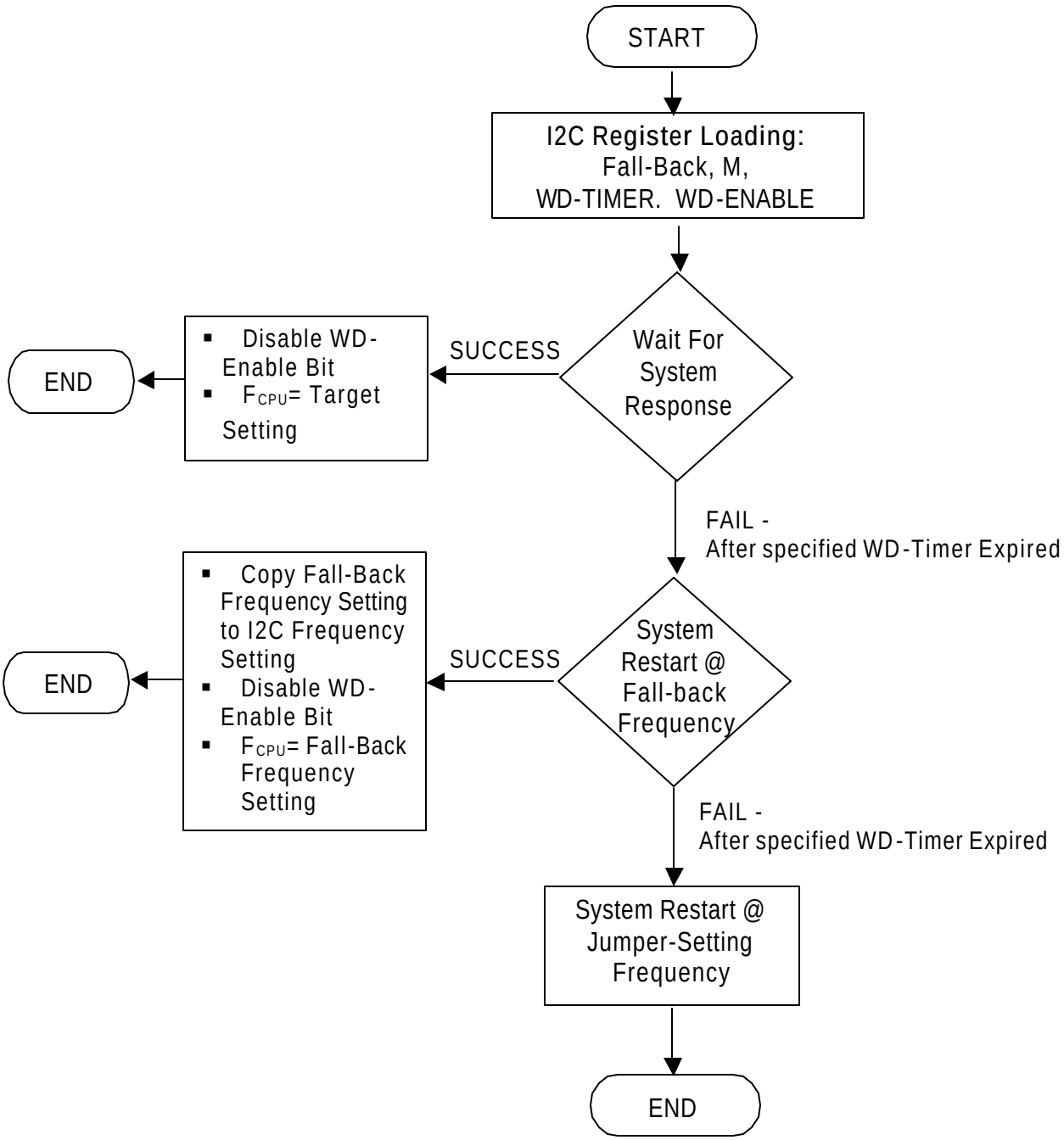
7	6	5	4	3	2	1	0		
0	0	0	0	0	0	0	0	M =0	Setting in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0		
7	6	5	4	3	2	1	0		
1	0	0	0	1	1	1	1	WD-Timer = 15s	Setting in I2C.BYTE8
ENB		T5	T4	T3	T2	T1	T0		
7	6	5	4	3	2	1	0		
0	0	0	0	1	0	0	0	FBSEL	Setting in I2C.BYTE6
FB4	FB3	FB2	FB1	FB0					

The fall-back frequency is set to the same location as that of FSEL since frequency switching between different timing groups will cause system to hang up. After WD timer expired or 15 seconds, the system will restart properly at target 100.0MHz if CPU is capable; otherwise WDT will perform another reset action to restart the system from 66.8 Mhz

2B. Switch to target CPU=103Mhz within the same timing Group

The fall-back frequency is recommended to set at the most safe and comfortable level to ensure a successful reboot such as 100 if system is unable to switch to 103Mhz.

WDT OPERATIONAL FLOW CHART



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC/AC Electrical Specifications

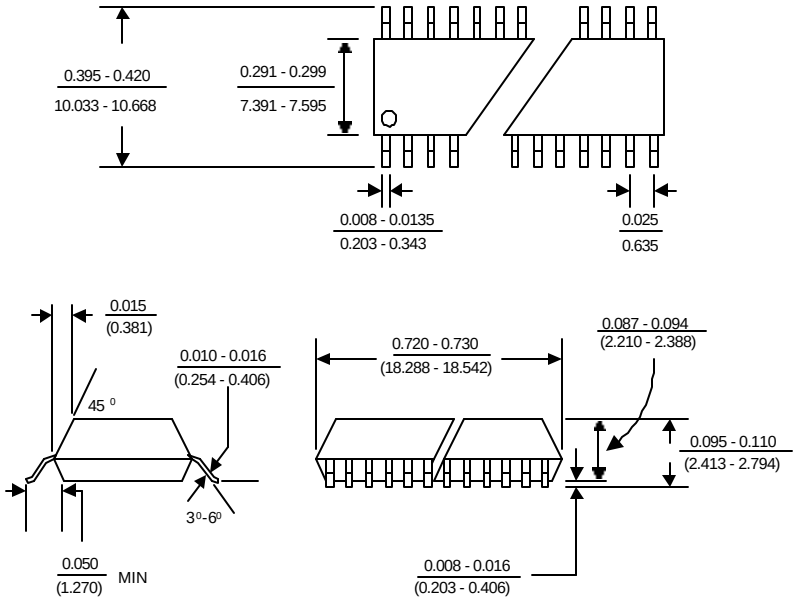
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	uA
Input Low Current	I_{IL1}	V_{IN}=0 with no pull-up resistor	-5			uA
Input Low Current	I_{IL2}	V_{IN}=0 with pull-up resistor	-200			
Supply Current	I_{DD}	C_L=0 pF@66MHz, 3.3V±5%			180	mA
	I_{DDL}	C_L=0 pF@133MHz, 3.3V±5%				
	I_{DD}	C_L=0 pF@66MHz, 2.5V±5%			72	
	I_{DDL}	C_L=0 pF@133MHz, 2.5V±5%			100	
Transition Time	T_{trans}	To 1st crossing of target Freq.			3	ms
Input frequency	F_I	V_{DD} = 3.3V	12	14.318	16	MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	XIN & XOUT pins	27	28	45	pF

2. DC/AC Electrical Specifications (continued)

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU	Measured @ 0.4V ~ 2.0V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 0.4V ~ 2.4V, C_L=10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 0.4V ~ 2.4V, C_L=10-30pf			2	
Output Fall time	T_{OF}	CPU	Measured @ 2.0 ~ 0.4V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 2.4V ~ 0.4V, C_L=10-20pf			4	
		PCI_F, PCI, AGP, APIC	Measured @ 2.4V ~ 0.4V, C_L=10-30pf			2	
Duty Cycle	D_T	CPU,APIC,REF, 48MHz,24MHz	Measured @ 1.5V C_L=20pf	45	50	55	%
		PCI, AGP	Measured @ 1.5V, C_L=20~30pf	40		55	
Clock Skew	T_{SKEW}	CPU	Rising edge @ 1.25V, C_L=20pf			175	ps
		PCI	Rising edge @ 1.5V, C_L=30pf			500	
		AGP	Rising edge @ 1.5V, C_L=30pf			500	
Jitter(Cycle to Cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		REF	Measured @ 1.5V			500	
		PCI, AGP	Measured @ 1.5V			250	
Frequency Stabilization Time	T_{FST}	CPU,PCI_F,PCI, APIC,AGP,REF, 48MHz,24MHz	Assumes full supply voltage reached within 1ms from power-up. Short cycle exist prior to frequency stabilization.			3	ms
AC output impedance	Z_0	CPU	V_{DD}=3.3V(2.5V)±5%		20		ohm
		PCI,AGP	V_{DD}=3.3V±5%		30		
		REF,48MHz,24MHz	V_{DD}=3.3V±5%		40		

PACKAGE INFORMATION



56PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL202-151 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP