PhaseLink Corporation

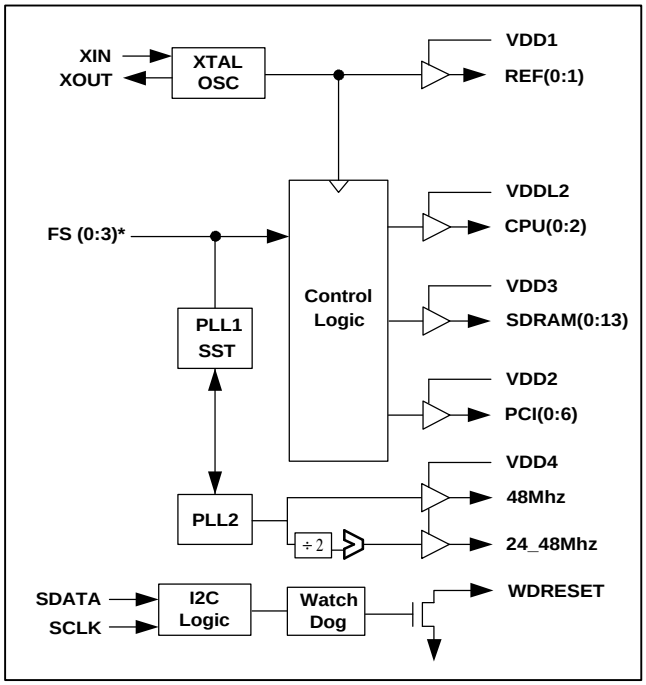
PLL202-13

Motherboard Clock Generator for SIS540/630 with 133MHz FSB

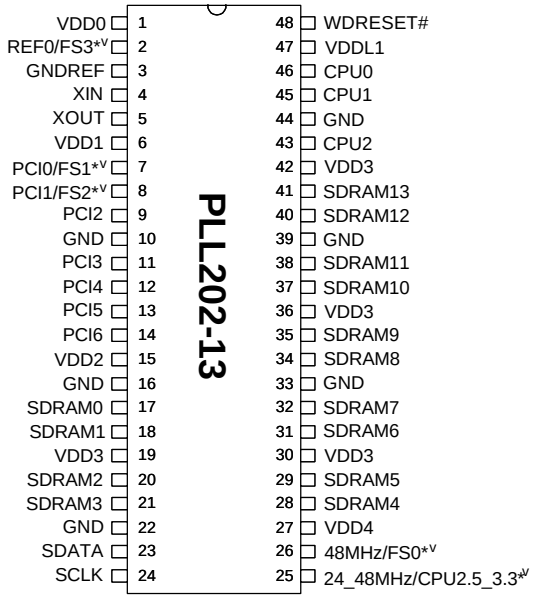
FEATURES

- Generates all clock frequencies for SIS540, SIS630 Pentium II and K6 chip sets, requiring multiple CPU clocks and high speed SDRAM buffers.
- Support 3 CPU clocks, 7PCI and 14 high-speed SDRAM buffers for 3-DIMM applications.
- One I2C selectable 24 or 48MHz clock output (default 24 MHz).
- One 48 MHz USB clock output.
- Two14.318MHz reference clocks.
- Support 2-wire I2C serial bus interface with built-in Vendor ID, Device ID and Revision ID.
- Single byte micro-step linear Frequency Programming via I2C with Glitch free smooth switching.
- Built-in programmable watch dog timer up to 63 seconds with 1-second interval. It will generate a LOW reset output when timer expired.
- Spread Spectrum ±0.25% center or -0.5% down.
- 50% duty cycle with low jitter.
- Available in 300 mil 48 pin SSOP.

BLOCK DIAGRAM



PIN CONFIGURATION



Note: v: Pull down, #: Active low *: Bi-directional latched at power-up

POWER GROUP

- VDD0: PLL CORE
- VDD1: REF0, XIN, XOUT
- VDD2: PCI(0:6)
- VDD3: SDRAM(0:13)
- VDD4: 48MHz, 24_48MHz
- VDDL1: CPU(0:2)

KEY SPECIFICATIONS

- CPU Cycle to Cycle jitter: 250ps.
- PCI to PCI output skew: 500ps.
- CPU to SDRAM output skew: 500ps.
- CPU to CPU output skew: 250ps.
- SDRAM to SDRAM output skew: 250ps.
- CPU to PCI skew (CPU leads): 1 ~ 4 ns.

PIN DESCRIPTIONS

Name	Number	Type	Description
VDD0	1	P	Power supply for PLL Core.
VDD1	6	P	Power supply for REF0, REF1, and crystal oscillator.
VDD2	15	P	Power supply for PCI (0:6).
VDD3	19,30,36,42	P	Power supply for SDRAM (0:13).
VDD4	27	P	Power supply for 24_48MHz and 48MHz.
VDDL1	47	P	Power supply for CPU (0:2) 2.5V.
GND	3,10,16,22, 33,39,44	P	Ground.
XIN	4	I	14.318MHz crystal input to be connected to one end of the crystal.
XOUT	5	O	14.318MHz crystal output.
REF0/FS3* PCI0/FS1* PCI1/FS2* 48MHz/FS0*	2,7,8,26	B	At power up, these pins are input pins and will determine the CPU clock frequency. After input sampling, these pins will generate output clocks. They have internal pull down (low by default).
PCI (0:6)	7,8,9,11,12, 13,14	O	PCI clocks with frequencies defined by Frequency Table.
CPU (0:2)	46,45,43	O	CPU clocks with frequencies defined by Frequency Table.
SDRAM (0:13)	17,18,20,21,28, 29,31,32,34,35, 37,38,40,41	O	SDRAM clocks with frequencies defined by Frequency Table.
SDATA	23	B	Serial data input for serial interface port.
SCLK	24	I	
48MHz	26	O	48MHz output for USB after input data latched during power-up.
24_48MHz/ CPU2.5_3.3*	25	B	Clock output for SUPER I/O after input data latched during power-up. It can be programmed by setting I2C byte1.bit7 to select either 24Mhz (default) or 48Mhz. CPU2.5_3.3 input will program internal CPU skew circuits based on CPU voltage. If high, it selects 2.5V. If Low, it selects 3.3V (default).
WDRESET#	48	O	This pin is an open drain output. It will be Low at watchdog timer expiration.
REF0	2	O	Buffered reference clock after input data latched during power-up.

Motherboard Clock Generator for SIS540/630 with 133MHz FSB

FREQUENCY (MHz) SELECTION TABLE

I2C Byte0 bit7	FS3	FS2	FS1	FS0	CPU	SDRAM	PCI	Spread Spectrum Modulation
0 default	0	0	0	0	66.6	100.0	33.3	0 to -0.5%
	0	0	0	1	100.0	100.0	33.3	0 to -0.5%
	0	0	1	0	150.0	100.0	37.6	±0.25%
	0	0	1	1	133.3	100.0	33.3	0 to -0.5%
	0	1	0	0	66.8	133.6	33.4	±0.25%
	0	1	0	1	100.0	133.3	33.3	0 to -0.5%
	0	1	1	0	100.0	150.0	37.6	±0.25%
	0	1	1	1	133.3	133.3	33.3	0 to -0.5%
	1	0	0	0	66.8	66.8	33.4	±0.25%
	1	0	0	1	97.0	97.0	32.3	0 to -0.5%
	1	0	1	0	68.0	113.3	28.3	±0.25%
	1	0	1	1	95.0	95.0	31.6	±0.25%
	1	1	0	0	95.0	126.7	31.6	±0.25%
	1	1	0	1	112.0	112.0	37.3	±0.25%
	1	1	1	0	166.0	111.0	27.6	±0.25%
	1	1	1	1	96.2	96.2	32.1	0 to -0.5%
1	0	0	0	0	66.8	100.2	33.4	±0.25%
	0	0	0	1	100.2	100.2	33.4	±0.25%
	0	0	1	0	97.0	97.0	32.3	±0.25%
	0	0	1	1	100.2	133.6	33.4	±0.25%
	0	1	0	0	75.0	100.0	37.5	±0.25%
	0	1	0	1	83.3	125.0	31.2	±0.25%
	0	1	1	0	105.0	140.0	35.0	±0.25%
	0	1	1	1	133.6	133.6	33.4	±0.25%
	1	0	0	0	110.2	147.0	36.7	±0.25%
	1	0	0	1	115.0	153.4	38.3	±0.25%
	1	0	1	0	120.0	120.0	30.0	±0.25%
	1	0	1	1	138.0	138.0	34.5	±0.25%
	1	1	0	0	140.0	140.0	35.0	±0.25%
	1	1	0	1	145.0	145.0	36.2	±0.25%
	1	1	1	0	147.6	147.6	36.9	±0.25%
	1	1	1	1	160.0	160.0	26.6	±0.25%

Motherboard Clock Generator for SIS540/630 with 133MHz FSB

FREQUENCY (MHz) SELECTION TABLE BY TIMING GROUP

Group Timing (CPU:SDRAM)	I2C Byte0 bit7	FS3	FS2	FS1	FS0	CPU	SDRAM	PCI	Spread Spectrum Modulation
A (2:2)	0	1	0	0	0	66.8	66.8	33.4	±0.25%
	0	1	0	1	1	95.0	95.0	31.6	±0.25%
	0	1	1	1	1	96.2	96.2	32.1	0 to -0.5%
	0	1	0	0	1	97.0	97.0	32.3	0 to -0.5%
	1	0	0	1	0	97.0	97.0	32.3	±0.25%
	0	0	0	0	1	100.0	100.0	33.3	0 to -0.5%
	1	0	0	0	1	100.2	100.2	33.4	±0.25%
	0	1	1	0	1	112.0	112.0	37.3	±0.25%
	1	1	0	1	0	120.0	120.0	30.0	±0.25%
	0	0	1	1	1	133.3	133.3	33.3	0 to -0.5%
	1	0	1	1	1	133.6	133.6	33.4	±0.25%
	1	1	0	1	1	138.0	138.0	34.5	±0.25%
	1	1	1	0	0	140.0	140.0	35.0	±0.25%
	1	1	1	0	1	145.0	145.0	36.2	±0.25%
	1	1	1	1	0	147.6	147.6	36.9	±0.25%
	1	1	1	1	1	160.0	160.0	26.6	±0.25%
B (2:3)	0	0	0	1	0	150.0	100.0	37.6	±0.25%
	0	1	1	1	0	166.0	111.0	27.6	±0.25%
C (3:2)	0	0	0	0	0	66.6	100.0	33.3	0 to -0.5%
	1	0	0	0	0	66.8	100.2	33.4	±0.25%
	1	0	1	0	1	83.3	125.0	31.2	±0.25%
	0	0	1	1	0	100.0	150.0	37.6	±0.25%
D (3:4)	0	0	0	1	1	133.3	100.0	33.3	0 to -0.5%
E (4:2)	0	0	1	0	0	66.8	133.6	33.4	±0.25%
F (4:3)	1	0	1	0	0	75.0	100.0	37.5	±0.25%
	0	1	1	0	0	95.0	126.7	31.6	±0.25%
	0	0	1	0	1	100.0	133.3	33.3	0 to -0.5%
	1	0	0	1	1	100.2	133.6	33.4	±0.25%
	1	0	1	1	0	105.0	140.0	35.0	±0.25%
	1	1	0	0	0	110.2	147.0	36.7	±0.25%
	1	1	0	0	1	115.0	153.4	38.3	±0.25%
G (5:3)	0	1	0	1	0	68.0	113.3	28.3	±0.25%

I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Serial Bits Reading	The serial bits will be read or sent by the clock driver in the following order Byte 0 – Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 – Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N – Bits 7, 6, 5, 4, 3, 2, 1, 0							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in **Write Mode:** the **Command Byte** and **Byte Count Byte must be sent by the master** but ignored by the slave, in **Read Mode:** the **Byte Count Byte** will be **read by the master** then all other **Data Byte**.							

I2C CONTROL REGISTERS

1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	FS4 (see Frequency selection Table)
Bit 6	8	0	FS2 (see Frequency selection Table)
Bit 5	7	1	FS1 (see Frequency selection Table)
Bit 4	26	0	FS0 (see Frequency selection Table)
Bit 3	-	0	Frequency selection control bit 1=Via I2C, 0=Via External jumper
Bit 2	2	0	FS3 (see Frequency selection Table)
Bit 1	-	1	0=Normal 1=Spread Spectrum enable
Bit 0	-	0	0=Normal 1=Tristate Mode for all outputs

2. BYTE 1: CPU Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Select 24_48MHZ output. 0=48Mhz, 1=24Mhz
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	43	1	CPU2 (Active/Inactive)
Bit 2	45	1	CPU1 (Active/Inactive)
Bit 1	46	1	CPU0 (Active/Inactive)
Bit 0	-	1	Reserved

3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted power up latched CPU2.5_3.3 value (Read-back only)
Bit 6	14	1	PCI6 (Active/Inactive)
Bit 5	13	1	PCI5 (Active/Inactive)
Bit 4	12	1	PCI4 (Active/Inactive)
Bit 3	11	1	PCI3 (Active/Inactive)
Bit 2	9	1	PCI2 (Active/Inactive)
Bit 1	8	1	PCI1 (Active/Inactive)
Bit 0	7	1	PCI0 (Active/Inactive)

4. BYTE 3: SDRAM Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	32	1	SDRAM7 (Active/Inactive)
Bit 6	31	1	SDRAM6 (Active/Inactive)
Bit 5	29	1	SDRAM5 (Active/Inactive)
Bit 4	28	1	SDRAM4 (Active/Inactive)
Bit 3	21	1	SDRAM3 (Active/Inactive)
Bit 2	20	1	SDRAM2 (Active/Inactive)
Bit 1	18	1	SDRAM1 (Active/Inactive)
Bit 0	17	1	SDRAM0 (Active/Inactive)

5. BYTE 4: Reserved Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	25	1	24_48MHz (Active/Inactive)
Bit 6	26	1	48MHz (Active/Inactive)
Bit 5	41	1	SDRAM13 (Active/Inactive)
Bit 4	40	1	SDRAM12 (Active/Inactive)
Bit 3	38	1	SDRAM11 (Active/Inactive)
Bit 2	37	1	SDRAM10 (Active/Inactive)
Bit 1	35	1	SDRAM9 (Active/Inactive)
Bit 0	34	1	SDRAM8 (Active/Inactive)

6. BYTE 5: Peripheral Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	X	Inverted power up latched FS3 value (Read-back only)
Bit 4	-	X	Inverted power up latched FS2 value (Read-back only)
Bit 3	-	X	Inverted power up latched FS1 value (Read-back only)
Bit 2	-	X	Inverted power up latched FS0 value (Read-back only)
Bit 1	48	1	REF1 (Active/Inactive)
Bit 0	2	1	REF0 (Active/Inactive)

7. BYTE 6: Fall-Back Frequency / Revision / Vendor ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description	
Bit 7	-	0	WDT Fall-back Frequency selection for FS4	Revision ID Bit 3*
Bit 6	-	0	WDT Fall-back Frequency selection for FS3	Revision ID Bit 2*
Bit 5	-	0	WDT Fall-back Frequency selection for FS2	Revision ID Bit 1*
Bit 4	-	0	WDT Fall-back Frequency selection for FS1	Revision ID Bit 0*
Bit 3	-	0	WDT Fall-back Frequency selection for FS0	Vendor ID Bit 3*
Bit 2	-	0	Vendor ID Bit 2*	
Bit 1	-	1	Vendor ID Bit 1*	
Bit 0	-	1	Vendor ID Bit 0*	

Note: *: Default value at power-up

8. BYTE 7: Linear Programming (M) Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0*	Linear programming sign bit (0 is "+", 1 is "–")
Bit 6	-	0*	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0*	Linear programming magnitude bit 5
Bit 4	-	0*	Linear programming magnitude bit 4
Bit 3	-	0*	Linear programming magnitude bit 3
Bit 2	-	0*	Linear programming magnitude bit 2
Bit 1	-	0*	Linear programming magnitude bit 1
Bit 0	-	0*	Linear programming magnitude bit 0 (LSB)

Note: This register will be initialized to 0 following WATCHDOG RESET.

9. BYTE 8: WATCHDOG TIMER / Device ID Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description	
Bit 7	-	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable	
Bit 6	-	0	Device ID Bit 6*	
Bit 5	-	0	Watchdog Time Interval Bit 5 (MSB)	Device ID Bit 5*
Bit 4	-	0	Watchdog Time Interval Bit 4	Device ID Bit 4*
Bit 3	-	0	Watchdog Time Interval Bit 3	Device ID Bit 3*
Bit 2	-	1	Watchdog Time Interval Bit 2	Device ID Bit 2*
Bit 1	-	1	Watchdog Time Interval Bit 1	Device ID Bit 1*
Bit 0	-	1	Watchdog Time Interval Bit 0 (LSB)	Device ID Bit 0*

Note: *: Default value at power-up

PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL202-13 device incorporates SMART-BYTE ™ technology with a single byte programming via I2C to better optimize clock jitter and spread spectrum performance. Detail of PLL202-13's dual mode frequency programming method is described below:

1. ROM-table Frequency Programming:

The pre-defined 32 frequencies found in Frequency table can be accessed either through 5 external jumpers or by setting internal I2C register in BYTE0.

2. Micro-step Linear Frequency Programming:

CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency change. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha \text{ (=0.22, 0.15, 0.11 or 0.09)} * M$$

Where:
1. M is magnitude factor defined in I2C Byte 7.bit(0:6)
2. ± (sign bit) of M is defined in I2C Byte7.bit 7
3. α is a constant but related to CPU's seven Timing groups definition
   α = 0.22 (for Group A, B) or α = 0.15 (for Group C,D)
   or α = 0.11 (for Group E, F) or α = 0.09 (for Group G)

FREQUENCY PROGRAMMING EXAMPLE:

1. Procedures to program target CPU frequency to 139.0 Mhz in Group A timing:

A. Locate the closest CPU frequency from Frequency-ROM table: 133.6
B. α = 0.22 for Group A
C. Solve M (Linear Magnitude factor) in integer:

$$M = (F_{CPU} - F_{CPU\text{-}ROMTABLE}) / \alpha$$
$$= (139 - 133.6) / 0.22$$
$$= 25$$

D. Program I2C register:

7	6	5	4	3	2	1	0	
0	1	1	1	**1**	1	0	0	Setting of I2C.BYTE0
FS3	FS2	FS1	FS0	CTR	FS4			

7	6	5	4	3	2	1	0	
0	0	0	1	1	0	0	1	Setting of M = +25 in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0	

F_{CPU} = 133.6 + (0.22) * 25 = 139.1 (% of frequency increased = 4.1 %)
F_{SDRAM} = 133.6 * (1+4.1%) = 139.1
F_{PCI} = 33.4 * (1+4.1%) = 34.7

BUILT-IN WATCHDOG TIMER (WDT)

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into "Hang-up" state within a reasonable period of time (or Watchdog time interval). The watchdog time interval can be programmed between 0 and 63 seconds with increment of 1 second by setting the value of I2C.Byte8.Bit(5:0). Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL202-13 will start from predefined Fall-back Frequency (the value of I2C Byte6,bits(7:3)). If system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

Example usage:

1. System power-up at CPU= 66.8MHz (Group A) where external jumpers are used.

2A. Switch to target CPU=100.0MHz frequency (Group C) with following I2C register setting:

7	6	5	4	3	2	1	0	
0	1	1	0	**1**	0	0	0	FSEL Setting in I2C.BYTE0
FS3	FS2	FS1	FS0	CTR	FS4			

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	M =0 Setting in I2C.BYTE7
Sign	M6	M5	M4	M3	M2	M1	M0	

7	6	5	4	3	2	1	0	
1	0	0	0	1	1	1	1	WD-Timer = 15s Setting in I2C.BYTE8
ENB		T5	T4	T3	T2	T1	T0	

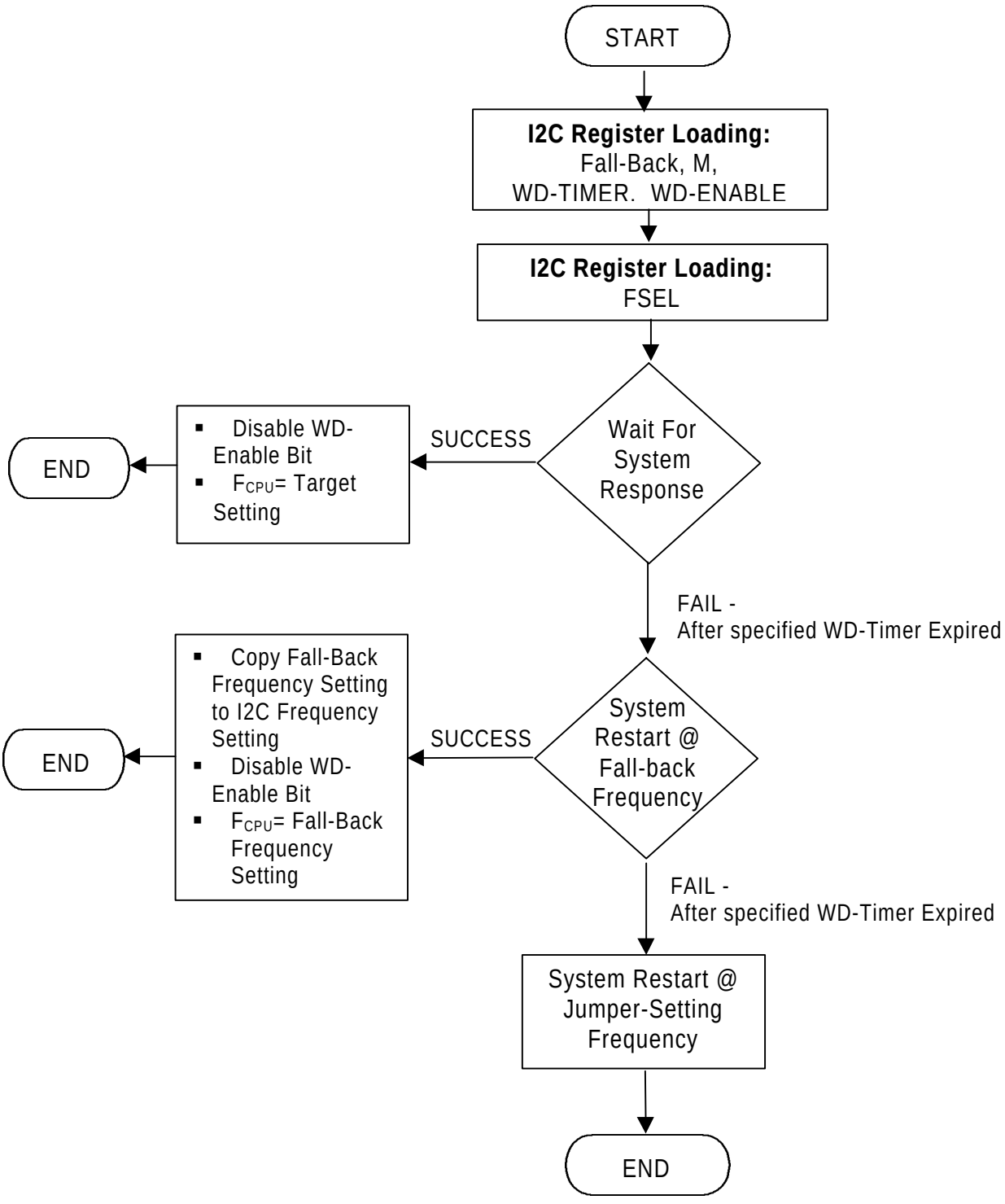
7	6	5	4	3	2	1	0	
0	0	1	1	0	0	0	0	FBSEL Setting in I2C.BYTE6
FB4	FB3	FB2	FB1	FB0				

The fall-back frequency is set to the same location as that of FSEL since frequency switching between different timing groups will cause system to hang up. After WD timer expired or 15 seconds, the system will restart properly at target 100.0MHz if CPU is capable; otherwise WDT will perform another reset action to restart the system from 66.8 Mhz

2B. Switch to target CPU=98Mhz within the same timing Group

The fall-back frequency is recommended to set at the most safe and comfortable level to ensure a successful reboot such as 95 or 96 if system is unable to switch to 98Mhz.

WDT OPERATIONAL FLOW CHART



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC/DC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2.0		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			10	uA
Input Low Current	I_{IL2}	Logic inputs with internal pull-down resistors			10	uA
Pull-down resistor	R_{Pd}	2,7,8,25,26			120	Kohm
Input frequency	F_I	V_{DD} = 3.3V		14.318		Mhz
Input Capacitance	C_{IN}	Logic Inputs			5	PF
	C_{INX}	XIN & XOUT pins	27		45	PF

2. Output Buffer Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU	Measured @ 0.4V ~ 2.4V, C_L=10-20pf, 3.3V±5%	1		4	V/ns
		REF0, REF1	Measured @ 0.4V ~ 2.4V, C_L=10-20pf	1		4	
		SDRAM, PCI	Measured @ 0.4V ~ 2.4V, C_L=10-30pf	1		4	
		24_48MHz	Measured @ 0.4V ~ 2.4V, C_L=10-30pf, 3.3V±5%				
Output Fall time	T_{OF}	CPU	Measured @ 2.4V ~ 0.4V, C_L=10-20pf, 3.3V±5%	1		4	V/ns
		REF0, REF1	Measured @ 2.4V ~ 0.4V, C_L=10-20pf	1		4	
		SDRAM, PCI	Measured @ 2.4V ~ 0.4V, C_L=10-30pf	1		4	
		24_48MHz	Measured @ 2.4V ~ 0.4V, C_L=10-30pf, 3.3V±5%				
Duty Cycle	D_T	CPU, 24_48MHz, 48MHz, REF, PCI, SDRAM	Measured @ 1.5V C_L=20pf, V_{DD}=2.5V	45		55	%
Clock Skew	T_{SKEW}	CPU to CPU	Measured @ 1.5V, equal loads			250	ps
		SDRAM to SDRAM				250	
		PCI to PCI				250	
		CPU to SDRAM				500	
		SDRAM to SDRAM				250	
		CPU to PCI		1		4	ns
Output Impedance	Z_0	CPU	V_{DD}=3.3V(2.5V)±5%		30		Ohm
		REF0, PCI, 48Mhz, 24_48Mhz	V_{DD}=3.3V±5%		25		
		SDRAM			20		
		REF1			20		

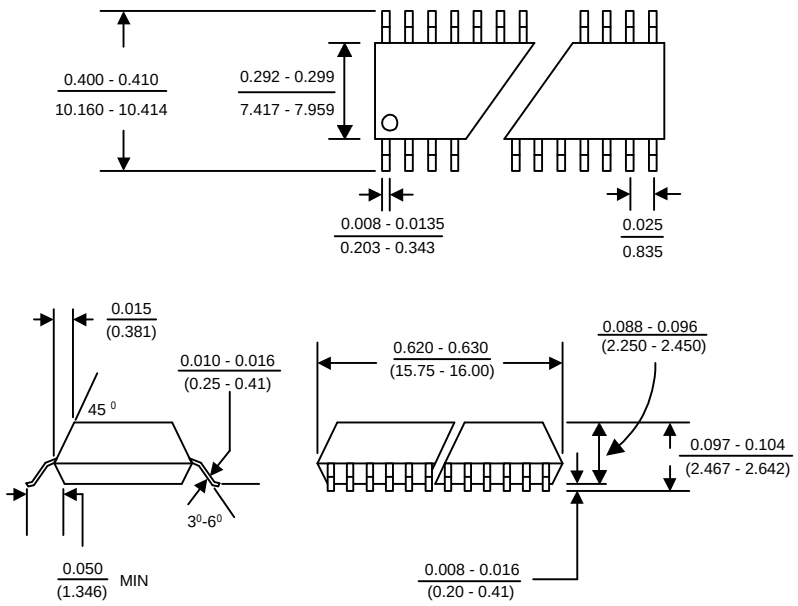
2. Output Buffer Electrical Specifications, continued

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Current	I_{OH}	CPU(0:2)	V_{OH} = 1.25V (V_{DD}=2.5V±5%)	45	70	105	mA
		SDRAM(0:13)	V_{OL} = 1.5V	80	110	155	
		PCI(0:6)		55	75	105	
		REF0		60	75	90	
		REF1		45	60	75	
		24_48MHz		55	75	105	
Output Low Current	I_{OL}	CPU(0:2)	V_{OH} = 1.25V (V_{DD}=2.5V±5%)	40	65	95	mA
		SDRAM(0:13)	V_{OL} = 1.5V	80	120	175	
		PCI(0:6)		55	85	125	
		REF0		60	85	110	
		REF1		45	65	90	
		24_48MHz		55	85	125	
Jitter, One Sigma	J_{sigma}	CPU	Measured @ 1.25V				ps
		PCI	Measured @ 1.5V			500	
		REF,48MHz,24MHz				800	
Jitter, Absolute	J_{Abs}	CPU	Measured @ 1.25V				ps
		PCI	Measured @ 1.5V			500	
		REF,48MHz,24MHz				800	
Jitter (cycle to cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		SDRAM	Measured @ 1.5V			250	
		PCI	Measured @ 1.5V			500	

Motherboard Clock Generator for SIS540/630 with 133MHz FSB

PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL202-13 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP