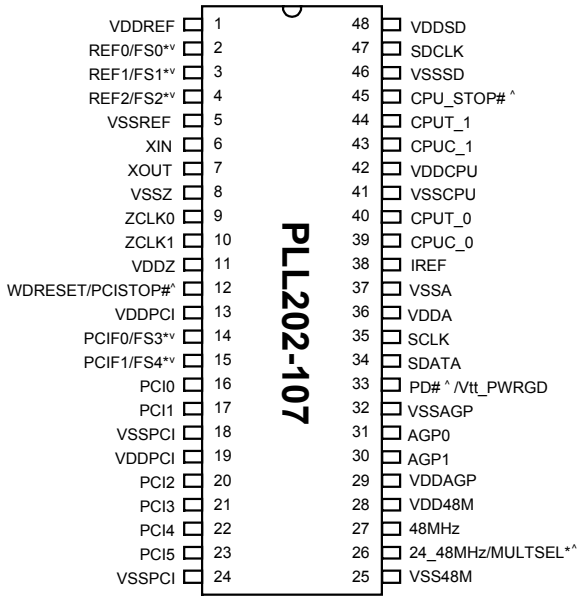
PLL202-107

Programmable Clock Generator for SIS 645/650 P4 Chip Sets

FEATURES

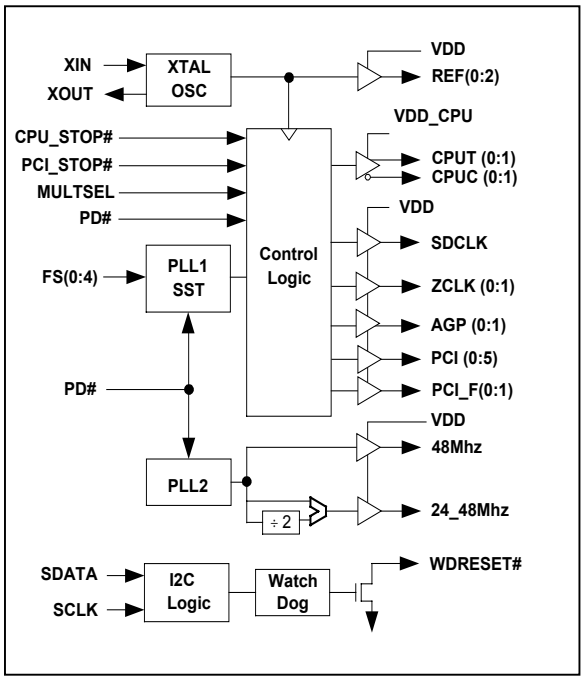
- Supports SIS 645/650, 646, 648 Chipsets.
- Programmable Spread Spectrum Modulation from ±0.1% to ±1.5% with step size as small as ±0.012%.
- Selectable Spread Spectrum either center or down.
- Selectable Spread Spectrum modulation profile.
- AccuSkew™, Programmable Precision skew tuning channel with maximum ±5% precision over the variation of temperature, process and voltage with step size as small as 80ps.
- AccuDrive™ Programmable Output Buffer drive strength with up to +50% or –40%.
- Programmable VCO frequency with one variable
- Programmable Output Divider for CPU, SDRAM, ZCLK, AGP and PCI.
- 2 differential CPUCLK, 1 SDRAM, 2 ZCLK, 2 AGP, 8 PCI, 1 USB and 3 REF clock outputs.
- 1 programmable 24MHz or 48MHz for SIO.
- Support 2-wire I2C serial bus interface.
- Built-in programmable watchdog timer
- Available in 300 mil 48 pin SSOP.

PIN CONFIGURATION



Note: ^: Pull Up (120kΩ), v: Pull down (120kΩ), **#**: Active low, *: Bi-directional latched at power-up

BLOCK DIAGRAM



POWER GROUP

- VDDREF (3.3V), VSSREF: REF, XIN, XOUT
- VDDPCI (3.3V), VSSPCI: PCI
- VDDAGP (3.3V), VSSAGP: AGP
- VDD48M (3.3V), VSS48M: 48MHz, 24_48MHz
- VDDCPU (3.3V), VSSCPU: CPUT/C_[0:1]
- VDDSD (3.3V), VSSSD: SDCLK
- VDDA (3.3V), VSSA: PLL Analog
- VDDZ (3.3V), VSSZ: ZCLK

KEY SPECIFICATIONS

- CPU - CPU Output Skew < 150ps.
- AGP(Z) - AGP(Z) Output Skew < 175ps
- PCI - PCI Output Skew <500ps
- CPU to SDCLK Skew: -2 to 2 ns (Typ 0ns).
- CPU (early) to AGP Skew: 1 to 4 ns (Typ 2ns).
- CPU (early) to Z Skew: 1 to 4 ns (Typ 2ns).
- CPU (early) to PCI Skew: 1 to 4ns (Typ 2ns).

PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	6	I	14.318Mhz crystal input to be connected to one end of the crystal
XOUT	7	O	14.318Mhz crystal output
REF[0:2]/FS[0:2]	2,3,4	B	14.318Mhz Reference clock output. This pin latch FS[0:2] value at power-up. (See Frequency Selection table). It has an internal pull down resistor.
PD#/Vtt_PWRGD	33	I	At power-up, this pin is the input of Vtt_PWRGD After the first high to low, this pin acts as PD# to disable all clock outputs including internal VCO and crystal clock when Low. When Vtt_PWRGD input is high, FS (0:4) and MULTSEL0 inputs are latched and all outputs are enabled.
AGP[0:1]	30,31	O	AGP clock output (see Frequency table).
ZCLK[0:1]	9,10	O	Hyper Zip clock output (see Frequency table).
CPU_STOP#	45	I	Stop all CPU clock outputs when low. It has 120K ohm internal pull up resistor.
WDRESET/ PCI_STOP#	12	B	Watch Dog reset will be generated after timer expires when I2C Enable bit (Byte12.bit7) is set active. When It is inactive, this pin acts as PCI_STOP input to stop all PCI clock outputs except PCIF[0:1] when low. It has 120K ohm internal pull up resistor.
PCI[0:5]	16,17,20 21,22,23	O	PCI clock output (see Frequency table). PCI5 has I2C programmable double drive strength.
24_48MHz/MULTSEL	26	B	This pin latches the MULTSEL value at power-up. After power-up, this pin acts as 24_48Mhz clock output with default 24MHz or selection by I2C. MULTSEL is used to select the current multiplier for the CPU outputs. If MULTSEL=0, IOH=4XIREF. If MULTSEL=1, IOH=6XIREF
CPU[C/T]_0	39,40	O	Differential pair output for CPU Host.
CPU[C/T]_1	43,44	O	Differential pair output for CPU Chip Sets.
PCIF[0:1]/FS[3:4]	14,15	B	Bi-directional pin. At power-up, the FS[3:4] input value is latched. After power-up, this pin acts as PCIF[0:1] output. It has an internal pull-down resistor.
SDCLK	37	O	SDRAM clock output
48MHz	27	O	USB clock output.
Iref	38	I	This pin establishes the reference current for the CPU differential pairs, it requires a fixed precision resistor tied to ground in order to establish the appropriate current.
SDATA	34	B	Serial data inputs for serial interface port.
SCLK	35	I	Serial data inputs for serial interface port.

PIN DESCRIPTIONS (Continue)

Name	Number	Type	Description
VDDPCI	13	P	3.3V Power Supply for PCIF[0:1], PCI[0:5] clock
VDDZ	11	P	3.3V Power Supply for Zclock.
VDDAGP	29	P	3.3V Power Supply for AGP clock.
VDDSD	48	P	3.3V Power Supply for SDCLK clock.
VDD48M	28	P	3.3V Power Supply for 48MHz and 24_48MHz clock
VDDA	36	P	3.3V power for internal PLL.
VDDCPU	42	P	3.3v power supply for CPU[T,C]_[0:1] clocks.
VDDREF	1	P	3.3v power supply for REF[0:2] clocks
VSS	5,8,18,19 27,34,41,46	P	Ground.

HOST SWING SELECT FUNCTIONS

MULTISEL0	Board Target Trace/Term Z	Reference R (Rr) I_{ref} = VDD/(3*Rr)	Output Current	V_{oh} @ Z
0	50Ω	Rr = 221Ω; 1% Iref = 5.0mA	I_{oh} = 4*IREF	1.0V @ 50Ω
1	50Ω	Rr = 475Ω; 1% Iref = 2.32 mA	I_{oh} = 6*IREF	0.7V @ 50Ω

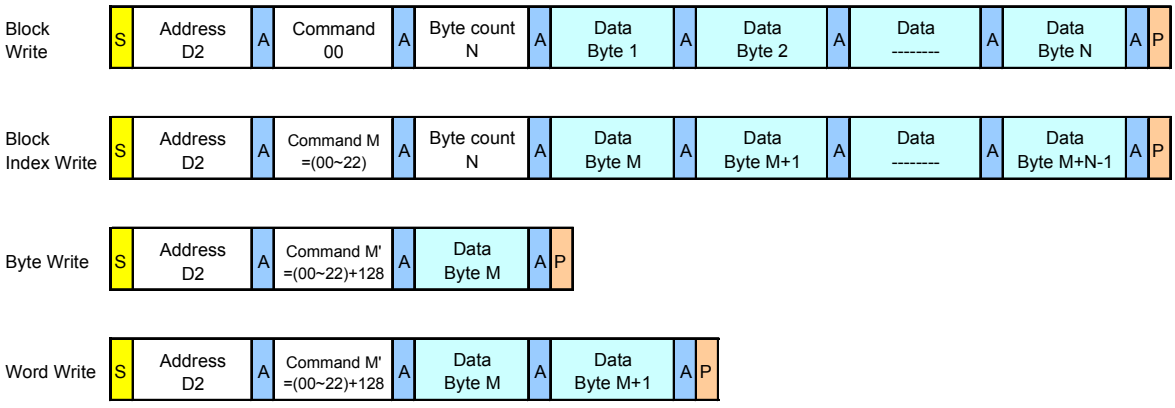
FREQUENCY (MHz) SELECTION TABLE

FS4	FS3	FS2	FS1	FS0	CPU	SDCLK	ZCLK	AGP	PCI	SST Amplitude	VCO	α (CPU)	N
0	0	0	0	0	66.67	66.67	66.67	66.67	33.33	±0.5% center	400	0.30	14,303
0	0	0	0	1	100.00	133.33	66.67	66.67	33.33	±0.3% center	400	0.45	14,303
0	0	0	1	0	111.17	166.75	66.70	66.70	33.35	±0.3% center	667	0.30	23,851
0	0	0	1	1	100.00	200.00	66.67	66.67	33.33	±0.3% center	400	0.45	14,303
0	0	1	0	0	100.00	100.00	133.33	66.67	33.33	±0.3% center	400	0.45	14,303
0	0	1	0	1	133.40	133.40	133.40	66.70	33.35	±0.3% center	667	0.36	23,851
0	0	1	1	0	133.40	166.75	133.40	66.70	33.35	±0.3% center	667	0.36	23,851
0	0	1	1	1	133.33	200.00	133.33	66.67	33.33	±0.3% center	400	0.60	14,303
0	1	0	0	0	100.00	166.67	66.67	66.67	33.33	±0.3% center	1000	0.18	35,759
0	1	0	0	1	100.00	133.33	133.33	66.67	33.33	±0.3% center	400	0.45	14,303
0	1	0	1	0	111.17	166.75	133.40	66.70	33.35	±0.3% center	667	0.30	23,851
0	1	0	1	1	100.00	200.00	133.33	66.67	33.33	±0.3% center	400	0.45	14,303
0	1	1	0	0	100.00	133.33	100.00	66.67	33.33	±0.3% center	400	0.45	14,303
0	1	1	0	1	133.33	133.33	100.00	66.67	33.33	±0.3% center	400	0.60	14,303
0	1	1	1	0	100.00	166.67	133.33	66.67	33.33	±0.3% center	1000	0.18	35,759
0	1	1	1	1	166.75	133.40	133.40	66.70	33.35	±0.3% center	667	0.45	23,851
1	0	0	0	0	166.67	200.00	133.33	66.67	33.33	±0.3% center	1000	0.30	35,759
1	0	0	0	1	150.00	150.00	120.00	60.00	30.00	±0.3% center	600	0.45	21,455
1	0	0	1	0	140.00	140.00	140.00	70.00	35.00	±0.3% center	700	0.36	25,031
1	0	0	1	1	166.75	166.75	133.40	66.70	33.35	±0.3% center	667	0.45	23,851
1	0	1	0	0	100.00	133.33	66.67	50.00	33.33	±0.3% center	400	0.45	14,303
1	0	1	0	1	100.00	133.33	80.00	50.00	33.33	±0.3% center	400	0.45	14,303
1	0	1	1	0	133.40	133.40	66.70	55.58	33.35	±0.3% center	667	0.36	23,851
1	0	1	1	1	133.40	166.75	83.38	55.58	33.35	±0.3% center	667	0.36	23,851
1	1	0	0	0	111.17	133.40	133.40	66.70	33.35	±0.3% center	667	0.30	23,851
1	1	0	0	1	125.00	166.67	166.67	62.50	33.33	±0.3% center	500	0.45	17,879
1	1	0	1	0	100.00	140.00	140.00	58.33	35.00	±0.3% center	700	0.26	25,031
1	1	0	1	1	120.00	150.00	150.00	60.00	33.33	±0.3% center	600	0.36	21,455
1	1	1	0	0	133.33	133.33	133.33	57.14	33.33	±0.3% center	400	0.60	14,303
1	1	1	0	1	100.00	133.33	133.33	50.00	33.33	±0.3% center	400	0.45	14,303
1	1	1	1	0	180.00	150.00	128.57	60.00	30.00	±0.3% center	900	0.36	32,183
1	1	1	1	1	200.00	200.00	133.33	66.67	33.33	±0.3% center	800	0.45	28,607

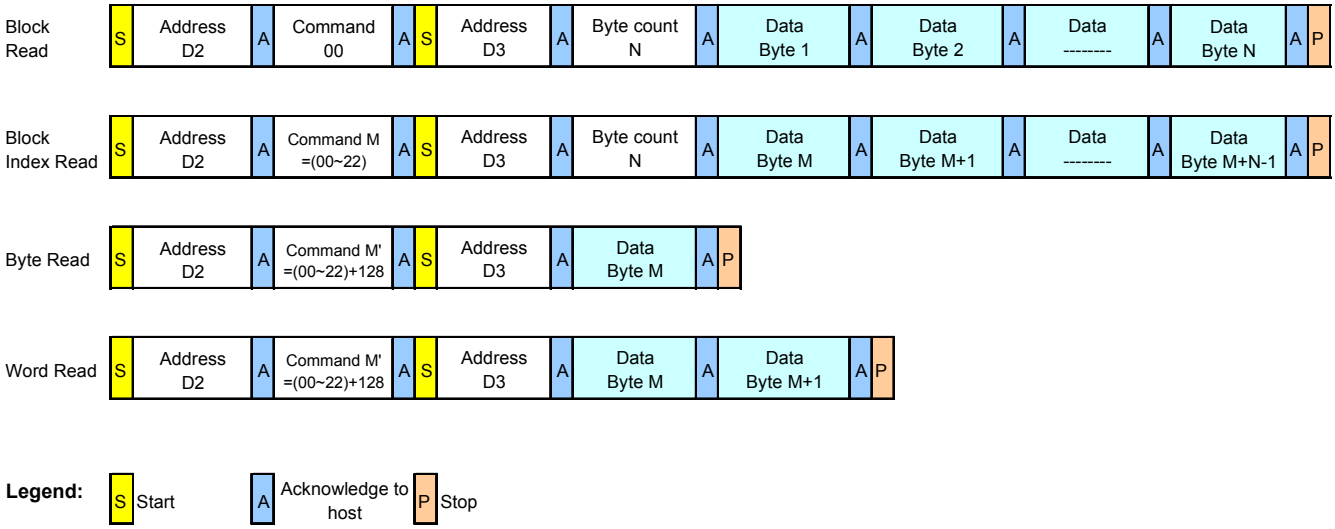
I2C BUS CONFIGURATION SETTING

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	_
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbits/s							
Data Protocol	This serial interface is designed to allow multiple protocols to write and read from the controller. It includes Block Read/Write, Block Index Read/Write, Byte Read/Write and Word Read/Write. In general, the bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3).							

WRITE MODE



READ MODE



Legend:

I2C CONTROL REGISTERS

1. BYTE 0~ 3: For External Zero Delay Buffer

2. BYTE 4: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	14	Power-up Latched FS3:FS0 value	FS3
Bit 6	4		FS2
Bit 5	3		FS1
Bit 4	2		FS0
Bit 3	-	0	Frequency selection bit: 1=Via I2C, 0=Via External jumper
Bit 2	15	Power-up Latched FS4 value	FS4
Bit 1	-	1	0=normal, 1= Spread Spectrum Enable
Bit 0	-	0	Spread Spectrum modulation amplitude selection. 0= defined in Frequency Table. 1= ±0.6% (center) fixed.

3. BYTE 5: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	30	1	AGP1 (1=Active 0=Inactive)
Bit 6	31	1	AGP0 (1=Active 0=Inactive)
Bit 5	30	1	24_48MHZ selection. 1=24Mhz, 0=48Mhz
Bit 4	15	X	Inverted Power-up latched FS4 value (Read only)
Bit 3	14	X	Inverted Power-up latched FS3 value (Read only)
Bit 2	4	X	Inverted Power-up latched FS2 value (Read only)
Bit 1	3	X	Inverted Power-up latched FS1 value (Read only)
Bit 0	2	X	Inverted Power-up latched FS0 value (Read only)

4. BYTE 6: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	10	1	ZCLK1 (1=Active, 0=Inactive)
Bit 6	9	1	ZCLK0 (1=Active, 0=Inactive)
Bit 5	14	0	PCI_STOP# setting for PCIF0 (0=Free Running, 1=Stopped)
Bit 4	15	0	PCI_STOP# setting for PCIF1 (0=Free Running, 1=Stopped)
Bit 3	39,40	1	CPU_STOP# setting for CPU[C/T]_0 (0=Free Running, 1=Stopped)
Bit 2	43,44	0	CPU_STOP# setting for CPU[C/T]_1 (0=Free Running, 1=Stopped)
Bit 1	39,40	1	CPU[C/T]_0 (1=Active 0=Inactive)
Bit 0	43,44	1	CPU[C/T]_1 (1=Active 0=Inactive)

5. BYTE 7: PCI Clock Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	15	1	PCIF1 (1=Active 0=Inactive)
Bit 6	14	1	PCIF0 (1=Active 0=Inactive)
Bit 5	23	1	PCI5 (1=Active 0=Inactive)
Bit 4	22	1	PCI4 (1=Active 0=Inactive)
Bit 3	21	1	PCI3 (1=Active 0=Inactive)
Bit 2	20	1	PCI2 (1=Active 0=Inactive)
Bit 1	17	1	PCI1 (1=Active 0=Inactive)
Bit 0	16	1	PCI0 (1=Active 0=Inactive)

6. BYTE 8: Vendor ID and Revision ID Register

Bit	Pin#	Default	Description
Bit 7	-	0	Vendor ID Bit 3 (read only)
Bit 6	-	0	Vendor ID Bit 2 (read only)
Bit 5	-	1	Vendor ID Bit 1 (read only)
Bit 4	-	1	Vendor ID Bit 0 (read only)
Bit 3	-	0	Revision ID Bit 3 (read only)
Bit 2	-	0	Revision ID Bit 2 (read only)
Bit 1	-	0	Revision ID Bit 1 (read only)
Bit 0	-	0	Revision ID Bit 0 (read only)

7. BYTE 9: Output Control Register

Bit	Pin#	Default	Description
Bit 7	27	1	48MHz (1=Active, 0=Inactive)
Bit 6	26	1	24_48MHz (1=Active, 0=Inactive)
Bit 5	47	1	SDCLK (1=Active, 0=Inactive)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	4	1	REF2 (1=Active, 0=Inactive)
Bit 1	3	1	REF1 (1=Active, 0=Inactive)
Bit 0	2	1	REF0 (1=Active, 0=Inactive)

8. BYTE 10: Control Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	MULTSEL1	0	IREF Multiplier setting, bit [0,7] 00= 4xIREF 01= 5xIREF 10= 6xIREF 11= 7xIREF
Bit 6	MULTSEL0	0	
Bit 5	-	0	MULTSEL (IREF multiple) MODE Selection. 0= selection through hardware input pin 26 1= selection through I2C control by bit[6,7]
Bit 4	26	0	Latched MULTSEL readback (read only)
Bit 3	-	0	(Reserved)
Bit 2	-	0	(Reserved)
Bit 1	-	0	(Reserved)
Bit 0	-	0	PCI5 double drive strength selection. 0=normal, 1=2X

9. BYTE 11: Linear Programming Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Linear programming sign bit (0 is "+", 1 is "–")
Bit 6	-	0	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0	Linear programming magnitude bit 5
Bit 4	-	0	Linear programming magnitude bit 4
Bit 3	-	0	Linear programming magnitude bit 3
Bit 2	-	0	Linear programming magnitude bit 2
Bit 1	-	0	Linear programming magnitude bit 1
Bit 0	-	0	Linear programming magnitude bit 0 (LSB)

10. BYTE 12: WATCHDOG Fall Back Register (1=Enable, 0=Disable)

Bit	Pin#	Default	Description
Bit 7	-	0	Watchdog Timer Unit Bit[7:6]: 00 = 250 ms, 01 = 500ms, 10 = 1s, 11 = 4s
Bit 6	-	0	
Bit 5	-	0	Initialization setting for Linear Programming Byte after Watch dog reset. 0= Byte 11 initialized to 0 after WD-Reset generated. 1= Byte 11 unchanged after WD-Reset generated.
Bit 4	-	0	WDT Fall-back Frequency selection for FS4
Bit 3	-	0	WDT Fall-back Frequency selection for FS3
Bit 2	-	0	WDT Fall-back Frequency selection for FS2
Bit 1	-	0	WDT Fall-back Frequency selection for FS1
Bit 0	-	0	WDT Fall-back Frequency selection for FS0

11. BYTE 13: WATCHDOG TIMER Register (1=Enable, 0=Disable)

Bit	Name	Default	Description
Bit 7	WDT ENB	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable
Bit 6	-	0	0=Watch Dog falls back to hardware jumper setting frequency 1=Watch Dog falls back to fall back frequency setting in Byte 12.
Bit 5	WDT<5>	0	Watchdog Time Interval Bit 5 (MSB)
Bit 4	WDT<4>	0	Watchdog Time Interval Bit 4
Bit 3	WDT<3>	0	Watchdog Time Interval Bit 3
Bit 2	WDT<2>	0	Watchdog Time Interval Bit 2
Bit 1	WDT<1>	0	Watchdog Time Interval Bit 1
Bit 0	WDT<0>	0	Watchdog Time Interval Bit 0 (LSB)

12. BYTE 14: Programming Mode Counter Register (1=Enable, 0=Disable)

Bit	Name	Default	Description
Bit 7	AccuSkew Enable	0	AccuSkew Setting for ± 5% process independent accuracy. 1=enable, 0=disable.
Bit 6	-	0	Initialization setting for Skew Control and Buffer drive strength registers after Watch dog reset. 0= Byte 16~22 initialized to 0 after WD-Reset generated. 1= Byte 16~22 unchanged after WD-Reset generated.
Bit 5	WDT Status	0	Watch Dog Timer Status info (read only)
Bit 4			
Bit 3	SST Profile	0	0= linear, 1= non-linear
Bit 2	Accu-SST Enable	0	Accu-SST programming Enable: 1= via I2C Byte12, 0= via ROM setting
Bit 1	Skew Enable	0	Enable Skew programming (byte16~18). 1=enable, 0=disable
Bit 0	VCO-N Enable	0	Enable VCO-N Counter programming (byte26~27) 1= programming through setting I2C byte 26~27 0= programming through Frequency ROM setting

13. BYTE 15: Spread Spectrum Modulation Amplitude Programming Register:

Bit	NAME	Default	Description
Bit 7	-	1	Spread Spectrum mode selection. 1=Center Spread, 0= Down Spread
Bit 6	SST6	1	1. Center Spread: SST<6:0> = Modulation rate * N /7 2. Down Spread: SST<6:0> = Modulation rate * N /14
Bit 5	SST5	1	
Bit 4	SST4	1	
Bit 3	SST3	1	
Bit 2	SST2	1	
Bit 1	SST1	1	
Bit 0	SST0	1	

TABLE 1: Output Signals SKEW Programming Summary:

Bit<2:0>	Skew Setting I (±80ps/step)		Skew Setting II (±160ps/step)	
111	+320ps	Setting applies to the following outputs: 1. CPU0 2. CPU1 3. SDCLK	+640ps	Setting applies to the following outputs: 1. ZCLK 2. AGP 3. All PCI
110	+240ps		+480ps	
101	+160ps		+320ps	
100	+80ps		+160ps	
011	**Default**		**Default**	
010	-80ps		-160ps	
001	-160ps		-320ps	
000	-240ps		-480ps	

14. Byte 16: SKEW Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	Skew CPU0	Bit <2>	0	These three bits will adjust timing of CPU_Host signals (CPUT_0/CPUC_0) either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	Skew CPU1	Bit <2>	0	These three bits will adjust timing of CPU_chip_sets signals (CPUT_1/CPUC_1) either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

16. Byte 17: SKEW Control Register

Bit	Name		Default	Description
Bit 7	CPU-PCI/AGP/Z Skew		1	Skew setting between CPU and Z/AGP/PCI clocks Bit[7:6]: 00 = 0.5 ns, 01 = 1.3 ns, 10 = 2 ns (default) 11 = 2.5ns
Bit 6			0	
Bit 5	Skew SDCLK	Bit <2>	0	These three bits will adjust timing of SDCLK signal either positive or negative delay up to +320ps or –240ps with ±80ps per step and ± 5% accuracy.
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	Skew ZCLK	Bit <2>	0	These three bits will adjust timing of ZCLK[0:1] clock signals either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

16. Byte 18: SKEW Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	Skew AGP	Bit <2>	0	These three bits will adjust timing of AGP0 and AGP1 clock signals either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	Skew PCI	Bit <2>	0	These three bits will adjust timing of all PCI clock signals either positive or negative delay up to +640ps or –480ps with ±160ps per step and ± 5% accuracy.
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

TABLE 2: Output Drive Strength Programming Summary:

Bit<2:0>	Setting I		Setting II		Setting III	
111	+33%	Setting applies to the following outputs 1. SDCLK	+40%	Setting applies to the following outputs 1. ZCLK[0:1] 2. AGP[0:1] 3. 48M, 24_48MHz	+50%	Setting applies to the following outputs 1. PCIF[0:1],PCI0 2. PCI[1:5] 3. REF[0:2]
110	+25%		+30%		+38%	
101	+17%		+20%		+25%	
100	+8%		+10%		+13%	
011	**Default**		**Default**		**Default**	
010	-8%		-10%		-13%	
001	-16%		-20%		-25%	
000	-25%		-30%		-38%	

18. Byte 19: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	-		0	Reserved.
Bit 4	-		0	Reserved.
Bit 3	-		0	Reserved.
Bit 2	SDCLK Strength	Bit <2>	0	These three bits will program drive strength for SDCLK output clock (see Table 2).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

18. Byte 20: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	ZCLK Strength	Bit <2>	0	These three bits will program drive strength for ZCLK0 and ZCLK1 output clocks (see Table 2).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	AGP Strength	Bit <2>	0	These three bits will program drive strength for AGP0 and AGP1 output clocks (see Table 2).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

19. Byte 21: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	USB Strength	Bit <2>	0	These three bits will program drive strength for 48MHz and 24_48MHz output clocks (see Table 2).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	PCIF,PCI0 Strength	Bit <2>	0	These three bits will program drive strength for PCIF[0:1] and PCI0 output clocks (see Table 2).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

20. Byte 22: Buffer Drive Strength Control Register

Bit	Name		Default	Description
Bit 7	-		0	Reserved.
Bit 6	-		0	Reserved.
Bit 5	PCI[1:5] Strength	Bit <2>	0	These three bits will program drive strength for PCI[1:5] output clocks (see Table 2).
Bit 4		Bit <1>	1	
Bit 3		Bit <0>	1	
Bit 2	REF Strength	Bit <2>	0	These three bits will program drive strength for REF[0:2] output clocks (see Table 2).
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

TABLE 3: VCO Divider Programming Summary:

Bit<3:0>	High Speed Divider		Mid Speed Divider		Low Speed Divider	
1111	Default ROM Selection	1. CPU0 2. CPU1 3. SDCLK	Default ROM Selection	1. ZCLK 2. AGP[0:1]	Default ROM Selection	1. PCIF,PCI
1110	/16		/16		/32	
1101	/12		/12		/24	
1100	/10		/10		/20	
1011	N/A		N/A		N/A	
1010	/8		/8		/16	
1001	/6		/6		/12	
1000	/4		/15		/30	
0111	/7		/7		/14	
0110	/8		/8		/16	
0101	/6		/6		/12	
0100	/5		/5		/10	
0011	N/A		N/A		N/A	
0010	/4		/4		/8	
0001	/3		/3		/6	
0000	/2		/7.5		/15	

21. Byte 23: VCO Divider Control Register

Bit	Name		Default	Description
Bit 7	CPU-Host Divider -	Bit <3>	1	These four bits will program VCO divider for CPUT_0 and CPUC_0 clocks (see Table 3).
Bit 6		Bit <2>	1	
Bit 5		Bit <1>	1	
Bit 4		Bit <0>	1	
Bit 3	CPU-CS Divider	Bit <3>	1	These four bits will program VCO divider for CPUC_1 and CPUT_1 clocks (see Table 3).
Bit 2		Bit <2>	1	
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

22. Byte 24: VCO Divider Control Register

Bit	Name		Default	Description
Bit 7	SDCLK Divider	Bit <3>	1	These four bits will program VCO divider SDRAM clock (see Table 3).
Bit 6		Bit <2>	1	
Bit 5		Bit <1>	1	
Bit 4		Bit <0>	1	
Bit 3	ZCLK Divider	Bit <3>	1	These four bits will program VCO divider for ZCLK clocks (see Table 3).
Bit 2		Bit <2>	1	
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

23. Byte 25: VCO Divider Control Register

Bit	Name		Default	Description
Bit 7	AGP[0:1] Divider	Bit <3>	1	These four bits will program VCO divider for AGP0 and AGP1 clocks (see Table 3).
Bit 6		Bit <2>	1	
Bit 5		Bit <1>	1	
Bit 4		Bit <0>	1	
Bit 3	PCI Divider	Bit <3>	1	These four bits will program VCO divider all PCI clocks (see Table 3).
Bit 2		Bit <2>	1	
Bit 1		Bit <1>	1	
Bit 0		Bit <0>	1	

24. BYTE 26: VCO N Counter Register:

Bit	Name	Default	Description
Bit 7	N<15>	1	VCO(MHz)= N<15:0> * 14.318/ 512
Bit 6	N<14>	1	
Bit 5	N<13>	1	
Bit 4	N<12>	1	
Bit 3	N<11>	1	
Bit 2	N<10>	1	
Bit 1	N<9>	1	
Bit 0	N<8>	1	

25. BYTE 27: VCO N Counter Register

Bit	Name	Default	Description
Bit 7	N<7>	1	VCO(MHz)= N<15:0> * 14.318/ 512
Bit 6	N<6>	1	
Bit 5	N<5>	1	
Bit 4	N<4>	1	
Bit 3	N<3>	1	
Bit 2	N<2>	1	
Bit 1	N<1>	1	
Bit 0	N<0>	1	

PROGRAMMING OF CPU FREQUENCY

To simplify traditional loop counter setting, the PLL202-107 device incorporates SMART-BYTE ™ and AccuVCO technology with one single variable programming via I2C. Detail of PLL202-107's tri-mode frequency programming method is described below:

1. **ROM-table Frequency Programming:**

   The pre-defined 32 frequencies found in Frequency table can be accessed through external jumpers or 5 bits I2C setting.

2. **Micro-step Linear Frequency Programming:**

   CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency changes.

$$F_{CPU} = F_{CPU.ROM\text{-}Table} \pm \alpha * M$$

   Where:
   1. M is a magnitude factor defined in I2C Byte 11.bit (0:6)
   2. ± (sign bit) of M is defined in I2C Byte11.bit 7
   3. α is defined in Frequency table or = 1.79/(VCO_Divider).

3. **VCO Frequency Programming:**

   Internal VCO frequency is defined as the function of N times a fixed constant of 0.028.

$$F_{VCO} = N * 0.028$$

   Where:
   1. F_{VCO} is limited in the range between 200(Mhz) to 1200(Mhz).
   2. N (counter) is defined in I2C byte 26,27

   Programmable VCO divider via I2C in Table 3 or pre-defined VCO divider in Frequency table will then determine the output CPU Frequency. Other bus frequencies will be changed proportionally with the rate that CPU frequency changes. The formula is as follow:

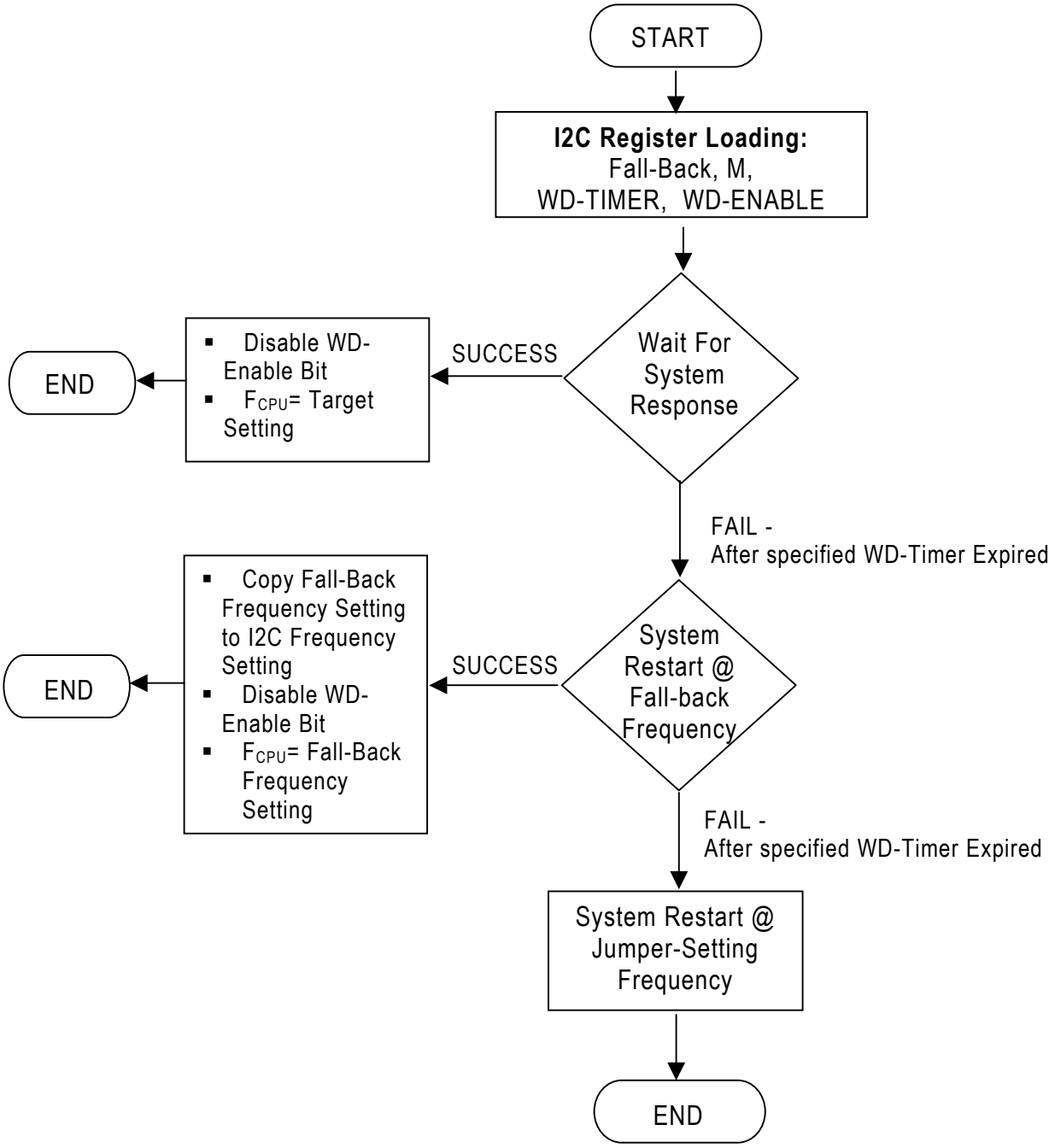
$$F_{CPU} = F_{VCO} \div VCO\_divider$$

   Where:
   1. VCO_divider is either predefined by frequency table or through I2C Byte 23-25

BUILT-IN WATCHDOG TIMER (WDT)

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into "Hang-up" state within a reasonable period of time (or Watchdog time interval). While disabled, the watchdog time interval can be programmed between 250ms and 256 seconds by setting the timer unit and timer interval. Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL202-107 will start from predefined Fall-back Frequency if system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

WDT OPERATIONAL FLOW CHART



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	0	70	°C
Junction Temperature	T_J		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. DC/AC Electrical Specifications

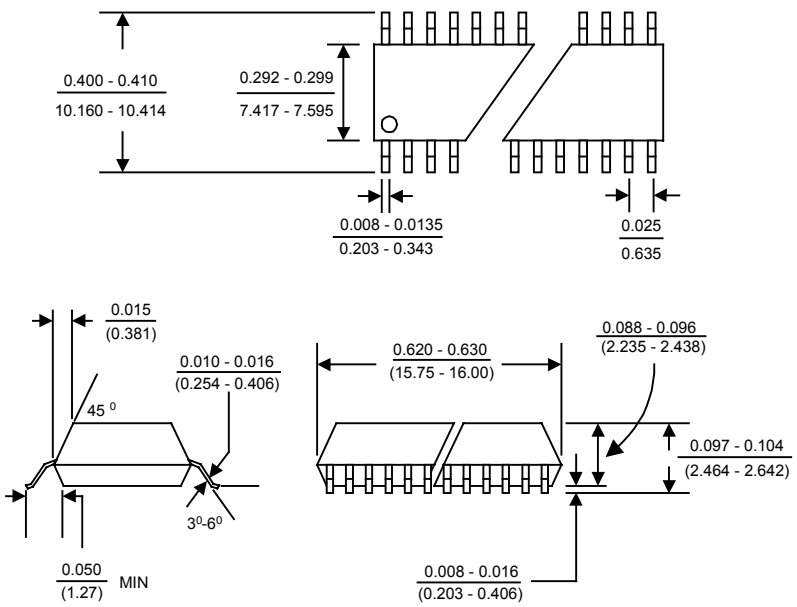
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	V_{IH}	All Inputs except XIN	2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}	All inputs except XIN	V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	uA
Input Low Current	I_{IL1}	V_{IN}=0 with no pull-up resistor	-5			uA
Input Low Current	I_{IL2}	V_{IN}=0 with pull-up resistor	-200			
Supply Current	I_{DD}	C_L=0 pF@66MHz, 3.3V±5%			180	mA
	I_{DDL}	C_L=0 pF@133MHz, 3.3V±5%				
	I_{DD}	C_L=0 pF@66MHz, 2.5V±5%			72	
	I_{DDL}	C_L=0 pF@133MHz, 2.5V±5%			100	
Transition Time	T_{trans}	To 1st crossing of target Freq.			3	ms
Input frequency	F_I	V_{DD} = 3.3V	12	14.318	16	MHz
Input Capacitance	C_{IN}	Logic Inputs			5	pF
	C_{INX}	XIN & XOUT pins	27	28	45	pF

2. DC/AC Electrical Specifications (continued)

Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T_A= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T_{OR}	CPU	Measured @ 0.4V ~ 2.0V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 0.4V ~ 2.4V, C_L=10-20pf			4	
		PCIF, PCI, AGP, APIC	Measured @ 0.4V ~ 2.4V, C_L=10-30pf			2	
Output Fall time	T_{OF}	CPU	Measured @ 2.0 ~ 0.4V, C_L=10-20pf, 2.5V±5%			1.6	ns
		REF, 48MHz, 24MHz	Measured @ 2.4V ~ 0.4V, C_L=10-20pf			4	
		PCIF, PCI, AGP, APIC	Measured @ 2.4V ~ 0.4V, C_L=10-30pf			2	
Duty Cycle	D_T	CPU,APIC,REF, 48MHz,24MHz	Measured @ 1.5V C_L=20pf	45	50	55	%
		PCI, AGP	Measured @ 1.5V, C_L=20~30pf	40		55	
Clock Skew	T_{SKEW}	CPU	Rising edge @ 1.25V, C_L=20pf			175	ps
		PCI	Rising edge @ 1.5V, C_L=30pf			500	
		AGP	Rising edge @ 1.5V, C_L=30pf			500	
Jitter(Cycle to Cycle)	$J_{cyc-cyc}$	CPU	Measured @ 1.25V			250	ps
		REF	Measured @ 1.5V			500	
		PCI, AGP	Measured @ 1.5V			250	
Frequency Stabilization Time	T_{FST}	CPU,PCIF,PCI, APIC,AGP,REF, 48MHz,24MHz	Assumes full supply voltage reached within 1ms from power-up. Short cycle exist prior to frequency stabilization.			3	ms
AC output impedance	Z_0	CPU	V_{DD}=3.3V(2.5V)±5%		20		ohm
		PCI,AGP	V_{DD}=3.3V±5%		30		
		REF,48MHz,24MHz	V_{DD}=3.3V±5%		40		

PACKAGE INFORMATION



48PIN SSOP

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL202-107 X C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
X=SSOP