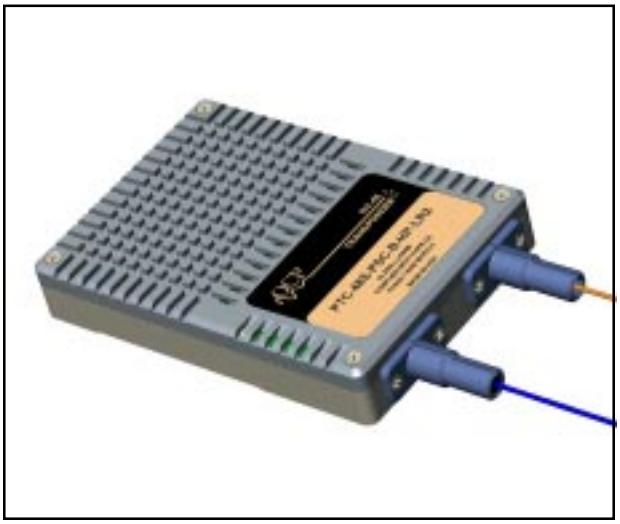
OCP©

PTC-48S

Compact 2.5 Gbits/s Transponder with 16-Channel 155Mbits/s Multiplexer/Demultiplexer with Clock Recovery



Features

- ☑ *Full Compliance with OC-48/STM-16 SONET/SDH Specifications*
- ☑ *Long Reach, Intermediate Reach & Short Reach*
- ☑ *Eye Safe (Class I Laser Safety)*
- ☑ *Laser bias & Facet monitor output*
- ☑ *Pigtailed Optical Interface*
- ☑ *Framing Support*
- ☑ *Compact size (2.85"x 2.00" x 0.47")*
- ☑ *-40°C to +85°C Operating Temperature ("A" Option)*
- ☑ *Single + 3.3 V supply*

Description

The PTC-48S fiber optic transponder offers a simple, convenient way to interface to single mode fiber optic cables for OC-48 short reach (SR), intermediate reach (IR), and long reach (LR) applications. The transponders are designed to meet or exceed the SONET/SDH optical interface requirements at OC-48/STM-16 (2488 Mb/s) data rate. Many versions are available with 1300nm Fabry Perot laser for SR, 1310nm DFB for IR1 and LR1, 1550nm DFB lasers for IR2 and LR2 applications. The modules are fully compliant to all applicable SONET/SDH specifications. All modules satisfy Class I Laser Safety requirements in accordance with the US FDA/CDRH and international IEC-825 standards.

On the transmitter side, the PTC-48S multiplexes sixteen 155 Mbits/s parallel data and transmits serialized optical signal at 2488Mbits/s to the fiber. On the receiver side, the module receives a 2488Mbits/s optical signal, which is converted to an electrical signal. The module regenerates the clock signal and demultiplexes the serialized data into sixteen 155 Mbits/s differential LVPECL data signals.

The transmit and receive functions are contained in a two-row, 160-pin (2x80) package with pigtail, which is terminated with LC, SC, ST or FC Optical connector. The transmitter incorporates all the necessary control and driver circuitry for converting parallel differential data signals to serial light. A Transmitter Disable input and Laser Bias Monitor output is provided. The receiver uses a PIN photodiode for SR & IR and an APD for LR to convert the serial light signal into a parallel differential electrical output signal. A Loss of Signal function which indicates loss of optical input is also provided.

The PTC-48S transceiver operates from a single +3.3V power supply over an operating temperature range of 0°C to +70°C ("B" Option) or -40°C to +85°C ("A" Option). The transceiver package is made of metal for good EMI shielding. It has a compact dimension of 2.85"x 2.00" x 0.47".

Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
Storage Temperature		T_{st}	- 40	+ 85	°C
Operating Case Temperature	"A" Option	T_{op}	- 40	+ 85	°C
	"B" Option		0	+ 70	
Operating Ambient Temperature [1]			0	+ 65	
Maximum Optical Input Power ("LR" only)		$P_{in,\ max}$	-	- 5.0	dBm
Supply Voltage		V_{CC}	0	+ 6.0	V

[1] With minimum of 150 linear foot per minute airflow.

PTC-48S

Transmitter Optical Characteristics (over Operating Case Temperature Range)

Parameter		Symbol	Minimum	Typical	Maximum	Units
Serial Optical Output Data Rate		B_O	-	2.488	-	Gb/s
Average Optical Output Power (50% duty cycle)	L1	P_o	- 10.0	- 7.0	- 3.0	dBm
	L0		- 5.0	- 3.0	0	
	HP		- 2.0	0	3.0	
Extinction Ratio		P_{hi}/P_{lo}	8.2	-	-	dB
Center Wavelength	SR (Short Reach)	λ_c	1266	1310	1360	nm
	IR1 (Intermediate Reach 1310 nm)		1266	1310	1360	
	IR2 (Intermediate Reach1550 nm)		1430	1550	1580	
	LR1 (Long Reach 1310 nm)		1280	1310	1335	
	LR2 (Long Reach 1550 nm)		1500	1550	1580	
Spectral Width (RMS)	SR (Short Reach)	$\Delta\lambda_{RMS}$	-	-	4.0	nm
Spectral Width (-20 dB)	IR1,IR2, LR1 & LR2	$\Delta\lambda_{20}$	-	-	1.0	
Side Mode Suppression Ratio	IR1, IR2, LR1 & LR2	$SMSR$	30	-	-	dB
Optical Output Eye	compliant with Bellcore TR-NWT-000253 and ITU-T Recommendation G.957					

Receiver Optical Characteristics (over Operating Case Temperature Range)

Parameter			Symbol	Minimum	Typical	Maximum	Units
Serial Optical Input Data Rate			B_O	2.48832 - 500 ppm	2.48832	2.48832 + 500 ppm	Gb/s
Receiver Sensitivity (10^{-10} BER) [1]	SR & IR (Short & Intermediate Reach)		P_{min}	- 19.0	- 21.0	-	dBm
	LR (Long Reach)			- 28.0	- 31.0	-	
Maximum Input Optical Power (10^{-10} BER) [1]	SR (Short Reach)		P_{max}	-	-	- 3.0	dBm
	IR (Intermediate Reach)			-	-	0	
	LR (Long Reach)			-	-	- 8.0	
Signal Detect Thresholds	SR & IR	Increasing Light Input	P_{sd+}	-	-	- 19.0	dBm
		Decreasing Light Input	P_{sd-}	- 35.0	-	-	
	LR	Increasing Light Input	P_{sd+}	-	-	- 28.0	dBm
		Decreasing Light Input	P_{sd-}	- 42.0	-	-	
Signal Detect Timing			-	3	-	100	μs
Signal Detect Hysteresis			-	0.5	1.0	-	dB
Optical Power Monitor Current	LR (P_{in} from -28 dBm to -17 dBm)		I_{PM}	-	6	-	μA/μW
	IR & SR (P_{in} from -20 dBm to 0 dBm)						
Wavelength of Operation			λ	1100	-	1600	nm
Optical Path Penalty [2]			-	-	-	1	dB
Jitter Tolerance & Transfer Function			compliant with ITU Recommendation G.958				

[1] Specified in Average Optical Input Power and measured at 2.48832 Gb/s and 1300 nm or 1550 nm wavelength with 2^{23}-1 PRBS.
[2] Optical Path Penalty for distance up to 40Km. Penalty for 80km is 2dB.

Power Supply Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage	V_{CC}	3.13	3.3	3.47	V
Supply Current [1]	I_{CC}	-	1500	1800	mA

[1] Supply current does not include termination resistor current.

Transmitter Electrical Characteristics (over Operating Case Temperature Range)

Parameter		Symbol	Minimum	Typical	Maximum	Units
Parallel Input Data Rate		B_E	155.52 - 500ppm	155.52	155.52 + 500ppm	Mb/s
Input Clock Duty Cycle		-	40	50	60	%
Reference Clock Signal Voltage swing	Differential	V_{INDIFF}	300	-	1200	mV
	Single-Ended	$V_{INSINGLE}$	150	-	600	
Reference Clock Input Duty Cycle		-	45	50	55	%
Differential Input Resistance		R_{DIFF}	80	100	120	Ω
Input Voltage (TxD[0:15] & PICLKP/N)	HIGH	V_{IH}	V_{CC} - 1.20	-	V_{CC} - 0.30	V
	LOW	V_{IL}	V_{CC} - 2.00	-	V_{CC} - 1.50	V
Diagnostic Loopback Enable (DLLOP, LVTTL)	HIGH	V_{IH}	2.0	-	V_{CC}	V
	LOW	V_{IL}	0.0	-	0.8	V
Phase Error , (PHEER, Single Ended, LVPECL)	HIGH	V_{OH}	V_{CC} - 1.30	-	V_{CC} - 0.60	V
	LOW	V_{OL}	V_{CC} - 1.95	-	V_{CC} - 1.35	V
Line Loopback Enable (LLOOP, LVTTL)	HIGH	V_{IH}	2.0	-	V_{CC}	V
	LOW	V_{IL}	0.0	-	0.8	V
Phase Initialization (PHINIT, LVPECL)	HIGH	V_{IH}	V_{CC} - 1.00	-	V_{CC} - 0.57	V
	LOW	V_{IL}	V_{CC} - 2.30	-	V_{CC} - 1.44	V
Transmitter Disable Voltage (TxDIS, LV-TTL)	Disable	V_{DIS}	2.0	-	V_{CC}	V
	Enable	V_{EN}	0.0	-	0.8	V
LD Degradation Alarm Voltage (LSRALRM, LVTTL)	HIGH	V_{ALMH}	2.15	-	V_{CC}	V
	LOW	V_{ALML}	0.0	-	0.50	V
Laser Bias Monitor Voltage (LSRBIAS)		$V_{BM,DIF}$	-	200	1600	mV
Laser Back Facet Monitor Voltage (LPM)		$V_{FM,DIF}$	35	500	1000	mV

Receiver Electrical Characteristics (over Operating Case Temperature Range)

Parameter		Symbol	Minimum	Typical	Maximum	Units
Parallel Output Data Rate		B_E	-	155.52	-	Mb/s
Clock Duty Cycle		-	40	50	60	%
Clock Sampling Point		-	See Figure 5.			
Output Clock Jitter		CLK_J	-	-	0.01	Ulrms
Output Voltage (RxQ[0:15] , FP & POCLCKP/N, LVPECL)	HIGH	V_{OH}	V_{CC} -1.15	-	V_{CC} -0.60	V
	LOW	V_{OL}	V_{CC} -1.95	-	V_{CC} -1.50	
Input Voltage (OOF & FRAMEN, LVTTL)	HIGH	V_{IH}	2.0	-	V_{CC}	V
	LOW	V_{IL}	0	-	0.8	
Output Voltage (Search & LOS, LVTTL)	HIGH	V_{OH}	2.1	-	V_{CC}	V
	LOW	V_{OL}	0	-	0.5	

Pin Assignment

Pin #	Pin Name	I/O	Logic	Description
01	FGND	I	Supply	Frame Ground
02	IPDMON	O	Analog	Receiver Photodiode Current Monitor
03	TxDGND	I	Supply	Transmitter Digital Ground
04	TxD15P	I	LVPECL	Transmitter 155 Mbits/s MSB Data Input
05	TxD15N	I	LVPECL	Transmitter 155 Mbits/s MSB Data Input
06	TxD13P	I	LVPECL	Transmitter 155 Mbits/s Data Input
07	TxD13N	I	LVPECL	Transmitter 155 Mbits/s Data Input
08	TxDGND	I	Supply	Transmitter Digital Ground
09	TxD11P	I	LVPECL	Transmitter 155 Mbits/s Data Input
10	TxD11N	I	LVPECL	Transmitter 155 Mbits/s Data Input
11	TxD09P	I	LVPECL	Transmitter 155 Mbits/s Data Input
12	TxD09N	I	LVPECL	Transmitter 155 Mbits/s Data Input
13	TxDGND	I	Supply	Transmitter Digital Ground
14	TxD07P	I	LVPECL	Transmitter 155 Mbits/s Data Input
15	TxD07N	I	LVPECL	Transmitter 155 Mbits/s Data Input
16	TxD05P	I	LVPECL	Transmitter 155 Mbits/s Data Input
17	TxD05N	I	LVPECL	Transmitter 155 Mbits/s Data Input
18	TxDGND	I	Supply	Transmitter Digital Ground
19	TxD03P	I	LVPECL	Transmitter 155 Mbits/s Data Input
20	TxD03N	I	LVPECL	Transmitter 155 Mbits/s Data Input
21	TxD01P	I	LVPECL	Transmitter 155 Mbits/s Data Input
22	TxD01N	I	LVPECL	Transmitter 155 Mbits/s Data Input
23	TxDGND	I	Supply	Transmitter Digital Ground
24	PICLKP	I	LVPECL	Byte-aligned Parallel Input Clock at 155 MHz
25	PICLKN	I	LVPECL	Byte-aligned Parallel Input Clock at 155 MHz
26	LOCKDET	O	LVTTL	Lock Detect (active low)
27	TxDGND	I	Supply	Transmitter Digital Ground
28	Tx3.3D	I	Supply	Transmitter 3.3 V Digital Supply
29	Tx3.3D	I	Supply	Transmitter 3.3 V Digital Supply
30	TxAGND	I	Supply	Transmitter Analog Ground
31	Tx3.3A	I	Supply	Transmitter 3.3 V Analog Supply
32	Tx3.3A		Supply	Transmitter 3.3 V Analog Supply
33	TxAGND	I	Supply	Transmitter Analog Ground
34	LPM	O	Analog	Laser Power Monitor (Back Facet Monitor)
35	LSRALRM	O	LVTTL	Laser Degrade Alarm (active High or Low depedns on Prom)
36	LSRBIAS	O	Analog	Transmitter Laser Bias Output
37	NC	-	-	No User Connection Permitted
38	DLOOP	I	LVTTL	Dignostic Loopback (active low)
39	NC	-	-	No User Connection Permitted
40	FP	O	LVPECL	Frame Pulse
41	FRAMEN	I	LVTTL	Frame Enable
42	RxDGND	I	Supply	Receiver Digital Ground

Pin Assignment (Continued)

Pin #	Pin Name	I/O	Logic	Description
43	Rx3.3D	I	Supply	Receiver 3.3 V Digital Supply
44	Rx3.3D	I	Supply	Receiver 3.3 V Digital Supply
45	NC	-	-	No User Connection Permitted
46	RxAGND	I	Supply	Receiver Analog Ground
47	RxAGND	I	Supply	Receiver Analog Ground
48	Rx3.3A	I	Supply	Receiver 3.3 V Analog Supply
49	RxAGND	I	Supply	Receiver Analog Ground
50	RxAGND	I	Supply	Receiver Analog Ground
51	RxDGND	I	Supply	Receiver Digital Ground
52	NC	-	-	No User Connection Permitted
53	NC	-	-	No User Connection Permitted
54	NC	-	-	No User Connection Permitted
55	RxDGND	I	Supply	Receiver Digital Ground
56	RxQ14P	O	LVPECL	Receiver 155 Mbits/s Data Output
57	RxQ14N	O	LVPECL	Receiver 155 Mbits/s Data Output
58	RxQ12P	O	LVPECL	Receiver 155 Mbits/s Data Output
59	RxQ12N	O	LVPECL	Receiver 155 Mbits/s Data Output
60	RxDGND	I	Supply	Receiver Digital Ground
61	RxQ10P	O	LVPECL	Receiver 155 Mbits/s Data Output
62	RxQ10N	O	LVPECL	Receiver 155 Mbits/s Data Output
63	RxQ08P	O	LVPECL	Receiver 155 Mbits/s Data Output
64	RxQ08N	O	LVPECL	Receiver 155 Mbits/s Data Output
65	RxDGD	I	Supply	Supply Receiver Digital Ground
66	RxQ06P	O	LVPECL	Receiver 155 Mbits/s Data Output
67	RxQ06N	O	LVPECL	Receiver 155 Mbits/s Data Output
68	RxQ04P	O	LVPECL	Receiver 155 Mbits/s Data Output
69	RxQ04N	O	LVPECL	Receiver 155 Mbits/s Data Output
70	RxDGND	I	Supply	Receiver Digital Ground
71	RxQ02P	O	LVPECL	Receiver 155 Mbits/s Data Output
72	RxQ02N	O	LVPECL	Receiver 155 Mbits/s Data Output
73	RxQ00P	O	LVPECL	Receiver 155 Mbits/s LSB Data Output
74	RxQ00N	O	LVPECL	Receiver 155 Mbits/s LSB Data Output
75	RxDGND	I	Supply	Receiver Digital Ground
76	NC	-	-	No User Connection Permitted
77	NC	-	-	No User Connection Permitted
78	NC	-	-	No User Connection Permitted
79	NC	-	-	No User Connection Permitted
80	FGND	I	Supply	Frame Ground
81	FGND	I	Supply	Frame Ground
82	RESET	I	LVTTL	Master Reset (active low)
83	TxDGND	I	Supply	Transmitter Digital Ground
84	TxREFCLKP	I	LVPECL	Transmitter 155 Mbits/s Reference Clock Input

Pin Assignment (Continued)

Pin #	Pin Name	I/O	Logic	Description
85	TxREFCLKN	I	LVPECL	Transmitter 155 Mbits/s Reference Clock Input
86	TxD14P	I	LVPECL	Transmitter 155 Mbits/s Data Input
87	TxD14N	I	LVPECL	Transmitter 155 Mbits/s Data Input
88	TxDGND	I	Supply	Transmitter Digital Ground
89	TxD12P	I	LVPECL	Transmitter 155 Mbits/s Data Input
90	TxD12N	I	LVPECL	Transmitter 155 Mbits/s Data Input
91	TxD10P	I	LVPECL	Transmitter 155 Mbits/s Data Input
92	TxD10N	I	LVPECL	Transmitter 155 Mbits/s Data Input
93	TxDGND	I	Supply	Transmitter Digital Ground
94	TxD08P	I	LVPECL	Transmitter 155 Mbits/s Data Input
95	TxD08N	I	LVPECL	Transmitter 155 Mbits/s Data Input
96	TxD06P	I	LVPECL	Transmitter 155 Mbits/s Data Input
97	TxD06N	I	LVPECL	Transmitter 155 Mbits/s Data Input
98	TxDGND	I	Supply	Transmitter Digital Ground
99	TxD04P	I	LVPECL	Transmitter 155 Mbits/s Data Input
100	TxD04N	I	LVPECL	Transmitter 155 Mbits/s Data Input
101	TxD02P	I	LVPECL	Transmitter 155 Mbits/s Data Input
102	TxD02N	I	LVPECL	Transmitter 155 Mbits/s Data Input
103	TxDGND	I	Supply	Transmitter Digital Ground
104	TxD00P	I	LVPECL	Transmitter 155 Mbits/s LSB Data Input
105	TxD00N	I	LVPECL	Transmitter 155 Mbits/s LSB Data Input
106	TxDGND	I	Supply	Transmitter Digital Ground
107	PCLKP	O	LVPECL	Transmitter Parallel Reference Clock lutput
108	PCLKN	O	LVPECL	Transmitter Parallel Reference Clock Output
109	TxDGND	I	Supply	Transmitter Digital Ground
110	TxAGND	I	Supply	Transmitter Analog Ground
111	Tx3.3D	I	Supply	Transmitter Digital 3.3 V Supply
112	Tx3.3A	I	Supply	Transmitter Analog 3.3 V Supply
113	NC	-	-	No User Connection Permitted
114	PHINIT	I	LVPECL	Phase Initialization
115	TxDIS	I	TTL	Transmitter Disable
116	NC	-	-	No User Connection Permitted
117	PHERR	O	LVPECL	Phase Error
118	LLOOP	I	LVTTL	Line Loopback (active-low)
119	LOS	O	LVTTL	Loss of Signal (active low)
120	RxDGND	I	Supply	Receiver Digital Ground
121	OOF	I	LVTTL	Out of Frame (enable frame detection)
122	RxDGND	I	Supply	Receiver Digital Ground
123	Rx3.3D	I	Supply	Receiver Digital 3.3 V Supply
124	Rx3.3D	I	Supply	Receiver Digital 3.3 V Supply
125	SEARCH	O	LVTTL	Frame Search Output
126	RxAGND	I	Supply	Receiver Analog Ground
127	RxAGND	I	Supply	Receiver Analog Ground
128	Rx3.3A	I	Supply	Receiver Analog 3.3 V Supply

Pin Assignment (Continued)

Pin #	Pin Name	I/O	Logic	Description
127	RxAGND	I	Supply	Receiver Analog Ground
128	Rx3.3A	I	Supply	Receiver Analog 3.3 V Supply
129	POCLKP	O	LVPECL	Byte-Aligned Parallel Output Clock at 155 MHz
130	POCLKN	O	LVPECL	Byte-Aligned Parallel Output Clock at 155 MHz
131	NC	-	-	No User Connection Permitted
132	NC	-	-	No User Connection Permitted
133	NC	-	-	No User Connection Permitted
134	NC	-	-	No User Connection Permitted
135	RxDGND	I	Supply	Receiver Digital Ground
136	RxQ15P	O	LVPECL	Receiver MSB 155 Mbits/s Data Output
137	RxQ15N	O	LVPECL	Receiver MSB 155 Mbits/s Data Output
138	RxQ13P	O	LVPECL	Receiver 155 Mbits/s Data Output
139	RxQ13N	O	LVPECL	Receiver 155 Mbits/s Data Output
140	RxDGND	I	Supply	Receiver Digital Ground
141	RxQ11P	O	LVPECL	Receiver 155 Mbits/s Data Output
142	RxQ11N	O	LVPECL	Receiver 155 Mbits/s Data Output
143	RxQ09P	O	LVPECL	Receiver 155 Mbits/s Data Output
144	RxQ09N	O	LVPECL	Receiver 155 Mbits/s Data Output
145	RxDGND	I	Supply	Receiver Digital Ground
146	RxQ07P	O	LVPECL	Receiver 155 Mbits/s Data Output
147	RxQ07N	O	LVPECL	Receiver 155 Mbits/s Data Output
148	RxQ05P	O	LVPECL	Receiver 155 Mbits/s Data Output
149	RxQ05N	O	LVPECL	Receiver 155 Mbits/s Data Output
150	RxDGND	I	Supply	Receiver Digital Ground
151	RxQ03P	O	LVPECL	Receiver 155 Mbits/s Data Output
152	RxQ03N	O	LVPECL	Receiver 155 Mbits/s Data Output
153	RxQ01P	O	LVPECL	Receiver 155 Mbits/s Data Output
154	RxQ01N	O	LVPECL	Receiver 155 Mbits/s Data Output
155	RxDGND	I	Supply	Receiver Digital Ground
156	NC	-	-	No User Connection Permitted
157	NC	-	-	No User Connection Permitted
158	NC	-	-	No User Connection Permitted
159	NC	-	-	No User Connection Permitted
160	FGND	I	Supply	Frame Ground

Laser Safety: All transmitters are Class I Laser products per FDA/CDRH and IEC-825 standards. They must be operated under specified operating conditions.

Optical Communication Products, Inc.
DATE OF MANUFACTURE:

MANUFACTURED IN THE USA
This product complies with
21 CFR 1040.10 and 1040.11
Meets Class I Laser Safety Requirements

Application notes:

TxD[0:15]P and TxD[[0:15]N: Transmitter interfaces to 16-bit differential parallel input data lines. TxD00P/N is the least significant bit of input word and is the last bit serialized.The input signal is LVPECL and it could be terminated as shown in Fig. 1.

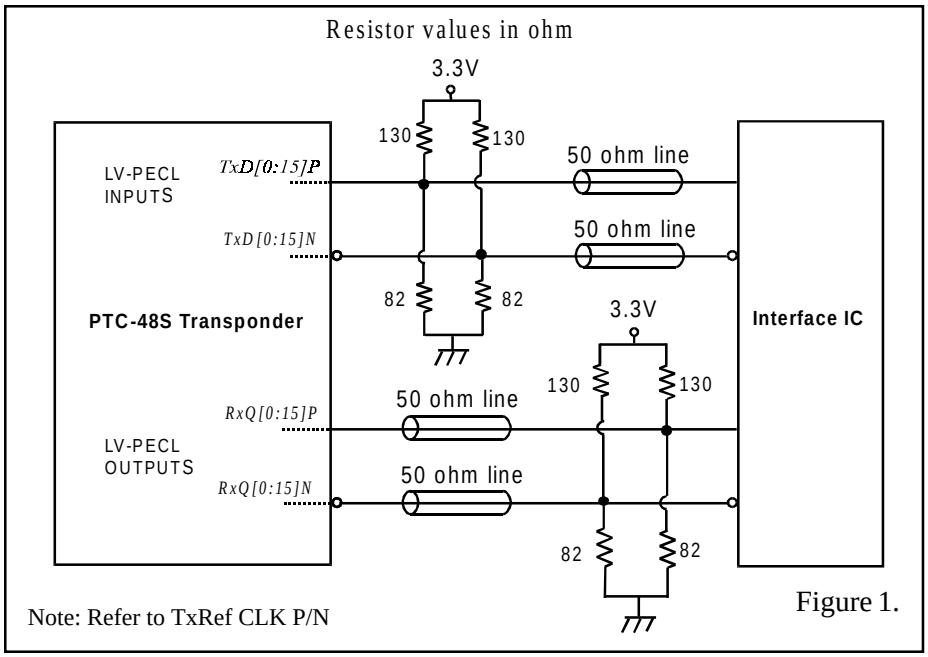


Figure 1.

RxD[0:15]P and RxD[0:15]P: Receiver interfaces to 16-bit differential parallel output data lines. RxD00P/N is the least significant bit of received word and is the last bit to be de-serialized. The output signal is LVPECL and it could be terminated as shown in Fig. 1.

IPDMON: This output will allow the user to measure the photocurrent generated by the optical receiver's photodiode. The current output has a gain of 8 for Pin version and gain of 1 for APD version. The recommended circuit is shown in Fig. 2.

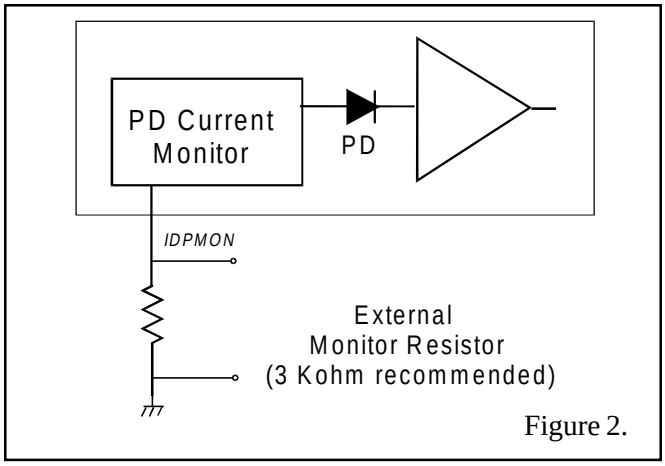


Figure 2.

LOCKDET: Lock Detect output is a LVTTL signal. If this output is logic "LOW" it indicates POCLK is equal to clocked signal provided at the TxREFCLK.

DLOOP: Diagnostic Loopback Enable. The input is LVTTL. When the input is logic "LOW", 2.5 Gb/s serial data stream from the transmeitter's parallel-to-serial converter receiver's is looped back internally to the receiver's serial-to-parallel converter receiver along with an internally generated bit synchronous serial clock. The receiver serial data path from the optical receiver is disabled temporally.

TxREFCLKP/N: Differential LVPECL low jitter 155.52 MHz Input Reference Clock. This input is used as the reference for the internal clock frequency synthesizer which generates the 2.5 GHz bit rate clock used to shift data out of the parallel-to-serial converter and also for the byte-rate clock, which transfers the 16-bit parallel input data from the input holding register into the parallel-to-serial shift register. Unlike TxD p/n this input is AC-coupled and internally biased and terminated.

RESET: Master Reset function is used to reset the multiplexer/ demultipler. A logic "LOW" at the input clears all registers and buffers. While resetting, the multiplexer/demultiplexer, POCLK and PCLK does not toggle.

LLOOP: Line Loopback Enable is a LVTTL input signal. When LLOOP is logic "LOW", the 2.5Gbits/s serial data and Recovered clock from the optical receiver are looped directly back to the optical transmitter. The multiplexed serial data from the parallel-to-serial converter is ignored

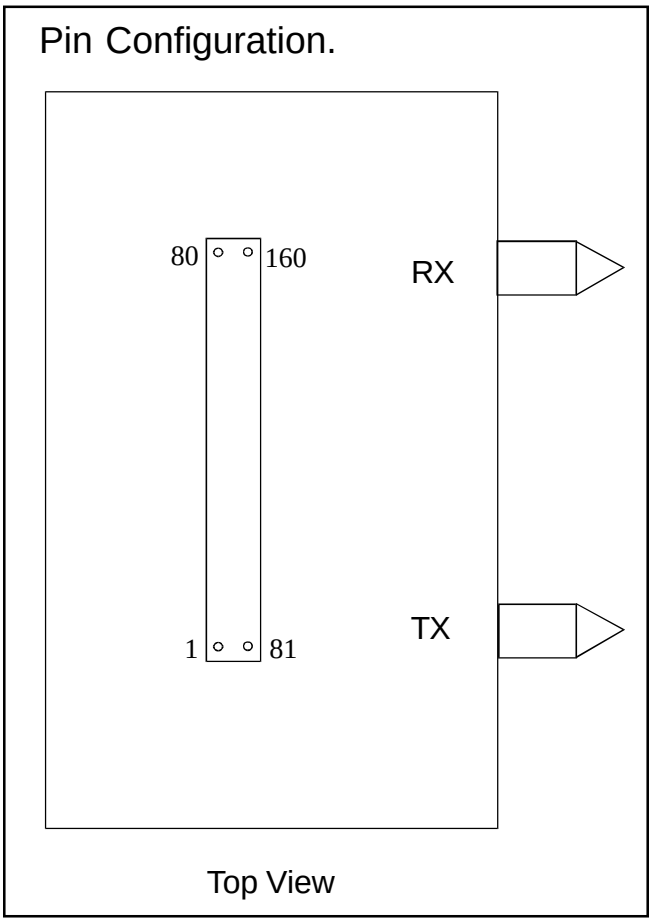
TxDIS: Transmitter disable input. Logic "HIGH" at the input will deactivate the laser so there is no optical output.

Application notes (continued)

PCLKP and **PCLKN:** Parallel Byte Clock is a differential LVPECL signal. A byte-rate reference clock generated by dividing the internal 2.488GHz serial bit clock by 16. This output is normally used to synchronize byte-wide transfers from upstream logic into the PTC-48S transponder.(Terminated as in figure 1.)

PHERR: Phase Error Signal is a Single-Ended LVPECL signal. This signal pulses high during each PCLK cycle for which there is potential setup/hold timing violations between the internal byte clock and the PICLK timing domains. PHERR is updated on the falling edge of the PICLK output.(Terminated as in figure 1.)

FP: Frame Pulse is LVPECL output signal. It indicates the frame boundaries in the received serial data stream. If framing pattern detection is enabled, FP pulses high for one POCLK cycle when a 32-bit sequence matching the framing pattern is detected in the received serial data. (Terminated as in figure 1.)



SEARCH: A1 A2 Frame Search Output is a LVTTL signal. When the output of this pin is logic "HIGH" it indicates that the frame detection circuit is active and is searching for a new A1 A2 byte alignment. The output will remain high during the A1 A2 frame search.

LOS: Loss of Signal is output and indicates the a loss of signal when insufficient optical power is received.

LSRBIAS: Laser Bias Monitor indicates the health of the laser in the transmitter. If this output voltage reaches 1.4V (70mA of bias current), the automatic power control circuit is struggling to maintain output power. This may indicate that the laser has reached an end-of-life condition.

LSRALRM: Laser Degrade Alarm logic "LOW" output will indicate that the transmitters automatic power control circuits are unable to maintain the nominal output power. This output will become active "LOW" when the optical output power degrades 3 dB below the nominal operating power.

LPM: Laser Power Monitor output is a analog output which indicate the level of the transmitting power from the transmitter. This output is set a 500mV for the nominal transmitter optical output power.

OOF: Out of Frame is LVTTL input signal. This indicator is used to enable framing pattern detection logic in transponder. The framing pattern detection logic is enabled by a rising edge on OFF, and remains enabled until frame boundary is detected. OFF is an asynchronous signal with a minimum pulse width of one POCLK period.

PICLKP and **PICLKN**: Differential LVPECL Parallel input Clock. A 155MHz nominally 50% duty cycle input clock to which TxD[0:15]P and TxD[0:15]N are assigned. The rising edge of PICLK transfers the data on the 16 TxD inputs into the holding register of the parallel-to-serial converter. Should be terminated the same as TxD P/N. fig.1

POCLKP and **POCLKN**: Differntial LVPECL Parallel Output Clock. A 155MHz normally 50% duty cycle, Byte rate output clock that is aligned to the RxQ[0:15] byte serial output data. Rx[0:15] and FP are updated on the falling edge of POCLK. Should be terminated the same as RxD P/N. fig.1

Transmitter Timing Characteristics

Phase Adjust Timing

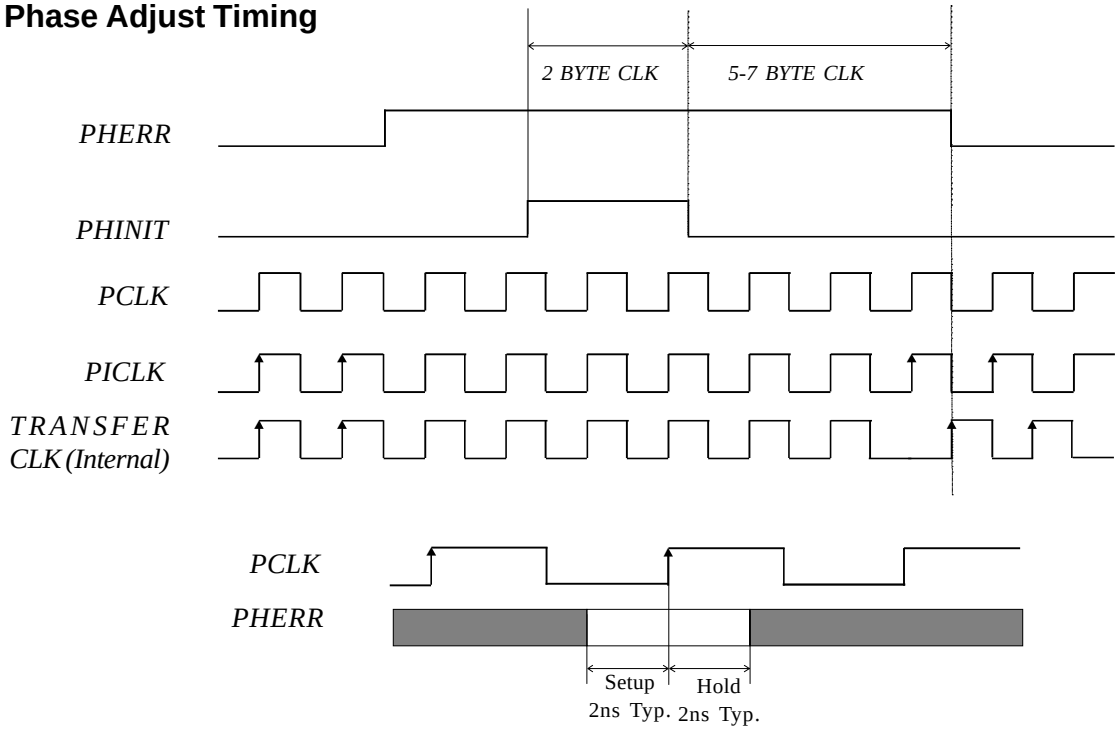


Figure 3.

AC Input Timing

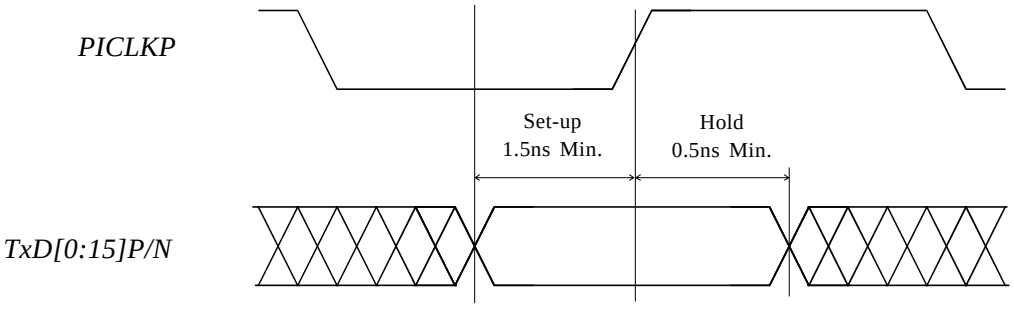


Figure 4.

Receiver Timing Characteristics

Output Timing Diagram

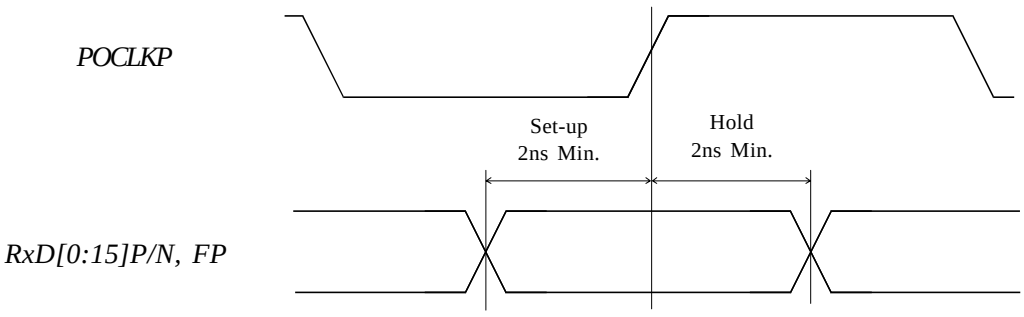
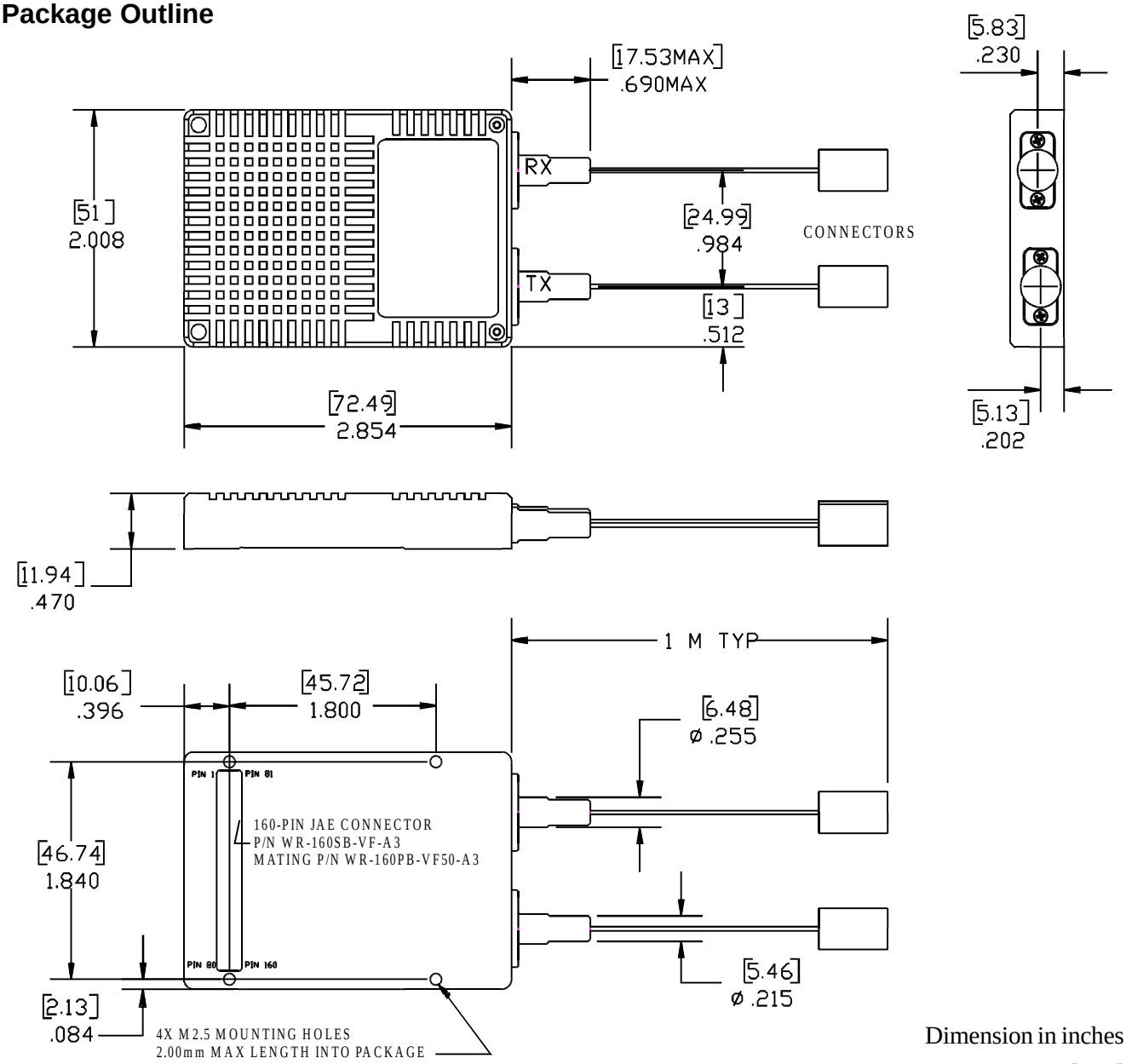


Figure 5.

Package Outline



Dimension in inches
[mm]

Ordering Information

PTC - 48S - P*zz* - *T* - *yy* - *DRn*

Package style
- PSC : Pigtailed with SC
- PST : Pigtailed with ST
- PFC : Pigtailed with FC
- PLC : Pigtailed with LC

Temperature Range
- A: -40°C to +85°C (Consult OCP)
- B: 0°C to +70°C

Light Output Power
- L1: - 7 dBm (typ.)
- L0: - 3 dBm (typ.)
- HP: 0 dBm (typ.)

Distance Option
- SR : Short Reach ("L1" only), (2km[1])
- IR1 : Intermediate Reach ("L0" only, 15km[1])
- IR2 : Intermediate Reach ("L0" only, 15km[1])
- LR1: Long Reach, (40km[1])
- LR2: Extended Long Reach , (80km[1])

[1]These are target distances to be used for classifications and not for specification, per ITU-T Recommendations G.957.

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