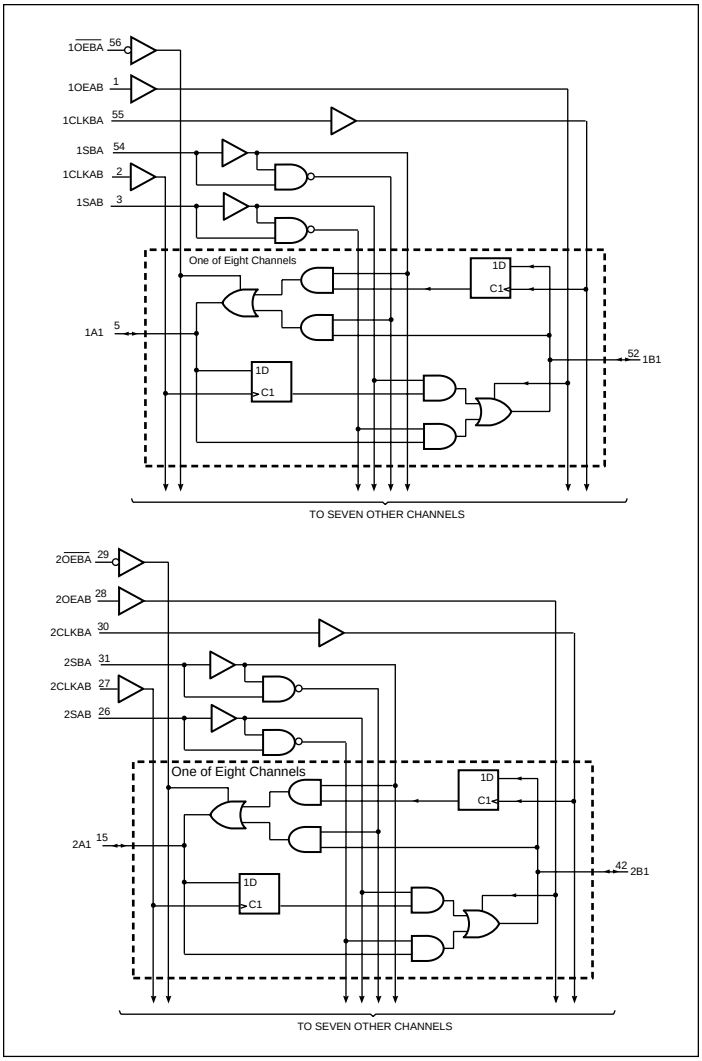
2.5V 16-Bit Bus Transceiver and Register with 3-State Outputs

Product Features

- PI74ALVTC16652 is designed for low voltage operation, V_{DD} = 1.65V to 3.6V
- Supports Live Insertion
- 3.6V I/O Tolerant Inputs and Outputs
- Bus Hold
- High Drive, –32/64mA @ 3.3V
- Uses patented noise reduction circuitry
- Power-off high impedance inputs and outputs
- Industrial operation at –40°C to +85°C
- Packages available:
  - –56-pin 240-mil wide plastic TSSOP (A56)
  - –56-pin 173-mil wide plastic TVSOP (K56)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74ALVTC series of logic circuits are produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

The PI74ALVTC16652 is a 16-bit bus transceiver and register designed for low 1.65V to 3.6V Vcc operation. It consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complementary Output Enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select Control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Circuitry used for Select Control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the levels on the Select Control or Output Enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-lops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are in the high-impedance state, each set of bus lines remains at its last level configuration.

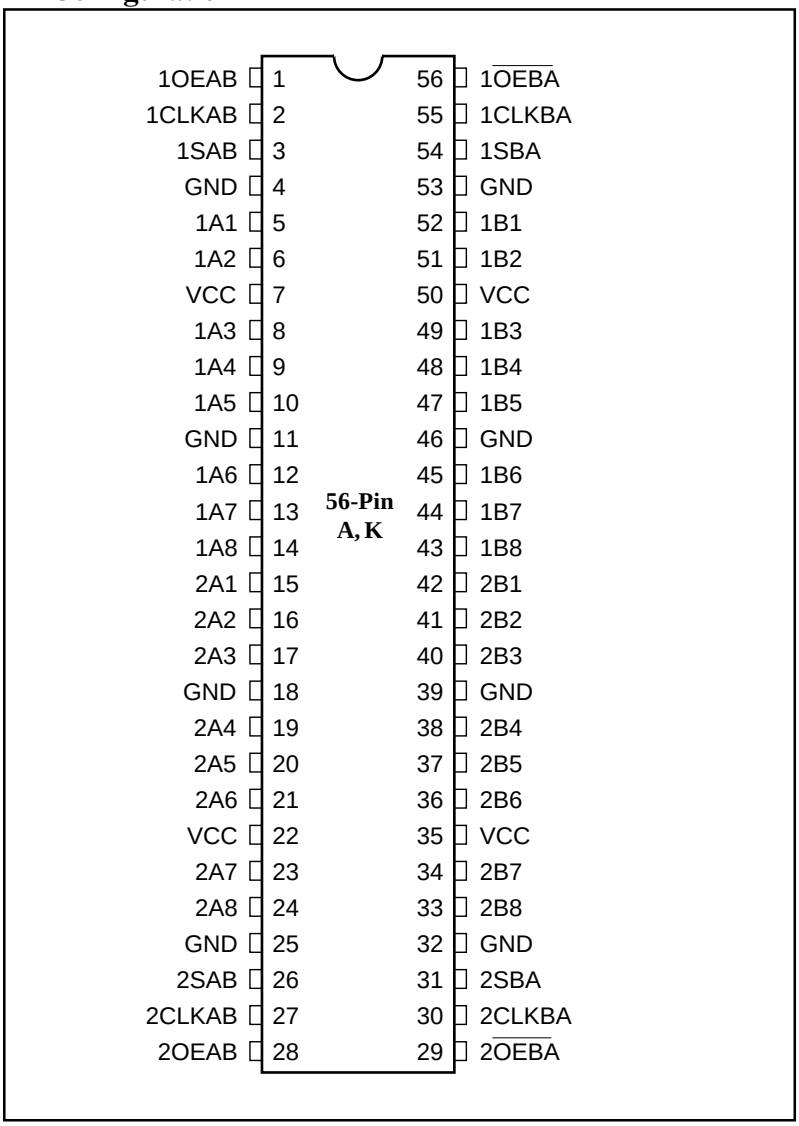
To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to Vcc through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking current sourcing capability of the driver.

The family offers both I/O Tolerant, which allows it to operate in mixed 1.65/3.6V systems, and "Bus Hold," which retains the data input's last state preventing "floating" inputs and eliminating the need for pullup/down resistors.

Product Pin Description

Pin Name	Description
OEAB	Output Enable Inputs (Active HIGH)
$\overline{\text{OEBA}}$	Output Enable Inputs (Active LOW)
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Select Control Inputs
xAx	Data Register A Inputs, Data Register B Outputs
xBx	Data Register B Inputs, Data Register A Outputs
GND	Ground
V_{CC}	Power

Pin Configuration



Truth Table[1]

Inputs						Data I/O*		Operation or Function
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1 - A8	B1 - B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified**	Store A, hold B
H	H	↑	↑	X**	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified**	Input	Hold A, store B
L	L	↑	↑	X	X**	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

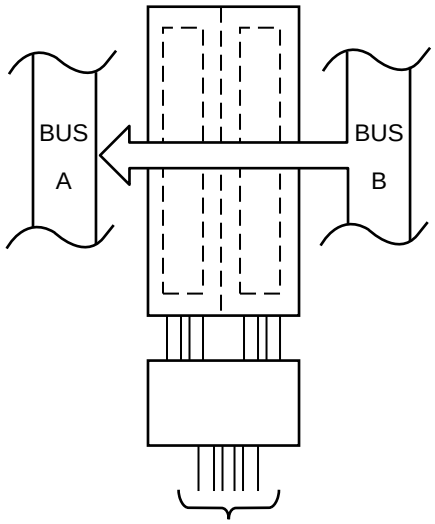
* The data output functions may be enabled or disabled by a varietyof level combinations at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

** Select control = L; clocks can occur simultaneously. Select control = H; to load both registers, clocks must be staggered.

Note:

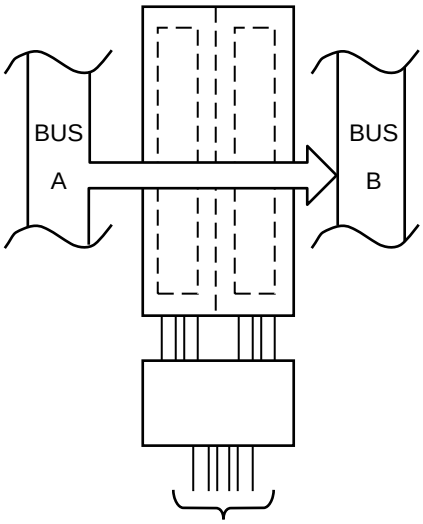
1. H = High Voltage Level, X = Don't Care, L = Low Voltage Level, ↑ = LOW-to-HIGH Transition

REAL-TIME TRANSFER
BUS B to A



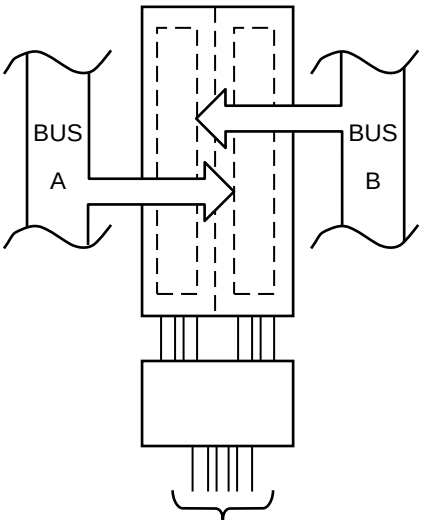
OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS A to B



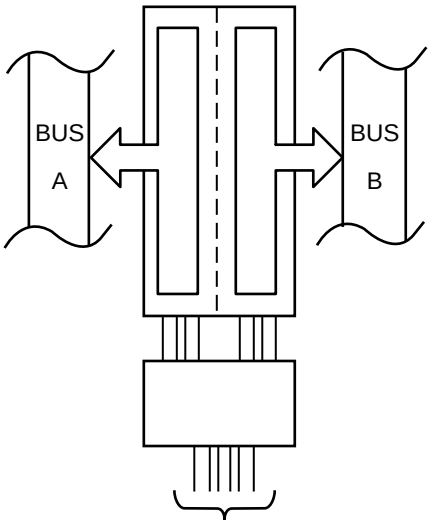
OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

STORAGE FROM
A,B, or A and B



OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED
DATA to A and/or B



OEAB	$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

Note:
1. Cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, V_{DD} ..... –0.5V to 4.6V
Input Voltage Range, V_I ..... –0.5V to 4.6V
Output Voltage Range, V_O (3-Stated) ..... –0.5V to 4.6V
Output Voltage Range, V_O[1] (Active) ..... –0.5V to V_{DD} +0.5V
DC Input Diode Current (I_{IK}) V_I < 0V ..... –50mA
DC Output Diode Current (I_{OK})
V_O < 0V ..... –50mA
V_O > V_{DD} ..... ±50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) ..... –64/128mA
DC V_{DD} or GND Current per Supply Pin (I_{CC} or GND) ..... ±100mA
Storage Temperature Range, T_{stg} ..... –65°C to 150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions[2]

			Min.	Max.	Units
V_{DD}	Supply voltage	Operating	1.65	3.6	V
		Data Retention Only	1.2	3.6	
V_{IH}	High-level input voltage	V_{DD} = 2.7V to 3.6V	2.0		
V_{IL}	Low-level input voltage	V_{DD} = 2.7V to 3.6V		0.8	
V_I	Input voltage		–0.3	3.6	
V_O	Output voltage	Active State	0	V_{DD}	
		Off State	0	3.6	
	Output current in I_{OH}/I_{OL}	V_{DD} = 3.0V to 3.6V V_{DD} = 3.0V to 3.6V V_{DD} = 2.3V to 2.7V V_{DD} = 1.65V to 1.95V		–32/64 ±24 ±18 ±6	mA
$\Delta t/\Delta v$	Input transistion rise or fall rate[3]		0	10	ns/V
T_A	Operating free-air temperature		–40	85	C

Notes:
1. Absolute maximum of I_O must be observed.
2. Unused control inputs must be held HIGH or LOW to prevent them from floating.
3 As measured between 0.8V and 2.0V, V_{DD}=3.0V.

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted)

DC Characteristics ($2.7V < V_{DD} \leq 3.6V$)

	Parameter	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	I_{IK} = –18mA	3.0			–1.2	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100µA	2.7 - 3.6	V_{DD} – 0.2			
		I_{OH} = –12mA	2.7	2.2			
		I_{OH} = –18mA	3.0	2.4			
		I_{OH} = –24mA		2.2			
		I_{OH} = –32mA		2.0			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100µA	2.7 - 3.6			0.2	
		I_{OL} = 12mA	2.7			0.4	
		I_{OL} = 18mA	3.0			0.4	
		I_{OL} = 24mA				0.45	
		I_{OL} = 32mA				0.5	
		I_{OL} = 64mA				0.75	
I_I	Input Leakage Current	$V_I = V_{DD}$, or GND	3.6			±5.0	µA
I_{OZ}	3-State Output Leakage	V_O = 3.6V	2.7			±10	
I_{OFF}	Power-OFF Leakage Current	V_I or $V_O \leq$ 3.6V	0			10	
I_{HOLD}	Bus Hold Current A or B Outputs	V_I = 0.8V	3.0	75			
		V_I = 2.0V		–75			
		V_I = 0 to 3.6V	3.6			±500	
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ or GND	2.7 - 3.6			50	
		$V_{DD} \leq (V_I, V_O) \leq$ 3.6V				±50	
ΔI_{DD}	Increase in I_{DD} per input	$V_{IH} = V_{DD}$ –0.6V, Other inputs at V_{DD} or GND				400	

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted; continued from previous page)

DC Characteristics ($2.3V \leq V_{DD} \leq 2.7V$)

Description	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	I_{IK} = –18mA	2.3			–1.2	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –100µA	2.3 -2.7	V_{DD}– 0.2			
		I_{OH} = –12mA	2.3	1.8			
		I_{OH} = –18mA		1.7			
V_{OL}	LOW Level Output Voltage	I_{OL} = 100µA	2.3 - 2.7			0.2	
		I_{OL} = 12mA	2.3			0.4	
		I_{OL} = 18mA				0.5	
		I_{OL} = 24mA				0.55	
I_I	Input Leakage Current	$V_I = V_{DD}$ or GND	2.7			±5.0	µA
I_{OZ}	3-State Output Leakage	V_O = 3.6V	2.3			±10	
I_{OFF}	Power-OFF Leakage Current	V_I or $V_O \leq 3.6V$	0			10	
I_{HOLD}(1)	Bus Hold Current A or B Outputs	V_I = 0.7V	2.5		90		µA
		V_I = 1.7V			–90		
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ or GND	2.3 - 2.7			40	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				±40	
ΔI_{DD}	Increase in I_{DD} per input	$V_{IH} = V_{DD}$ –0.6V, Inputs at V_{DD} or Gnd				400	

Note:

1. Not Guaranteed

Electrical Characteristics over Recommended Operating Free-Air Temperature Range

(unless otherwise noted; continued from previous page)

DC Characteristics ($1.65V \leq V_{DD} \leq 1.95V$)

Description	Parameters	Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Diode	$I_{IK} = -18mA$	1.65			–1.2	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100\mu A$	1.65-1.95	$V_{DD} - 0.2$			
		$I_{OH} = -6mA$	1.65	1.4			
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100\mu A$				0.2	
		$I_{OL} = 6mA$				0.3	
I_I	Input Leakage Current	$V_I = V_{DD}$ or GND	1.95			±5.0	μA
I_{OZ}	3-State Output Leakage	$V_O = 3.6V$	1.65			±10	
I_{OFF}	Power-OFF Leakage Current	$V_I = V_O \leq 3.6V$	0			10	
I_{HOLD}(1)	Bus Hold Current A or B Outputs	$V_I = 0.4$	1.65		50		
		$V_I = 1.3$			–50		
I_{DD}	Quiescent Supply Current	$V_I = V_{DD}$ or GND	1.65-1.95			20	
		$V_{DD} \leq (V_I, V_O) \leq 3.6V$				±20	
ΔI_{DD}	Increase in I_{DD} per input	$V_I = V_{DD} - 06V$, Other inputs at V_{DD} or Gnd				400	

Note:

1. Not Guaranteed

Timing Requirements (Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

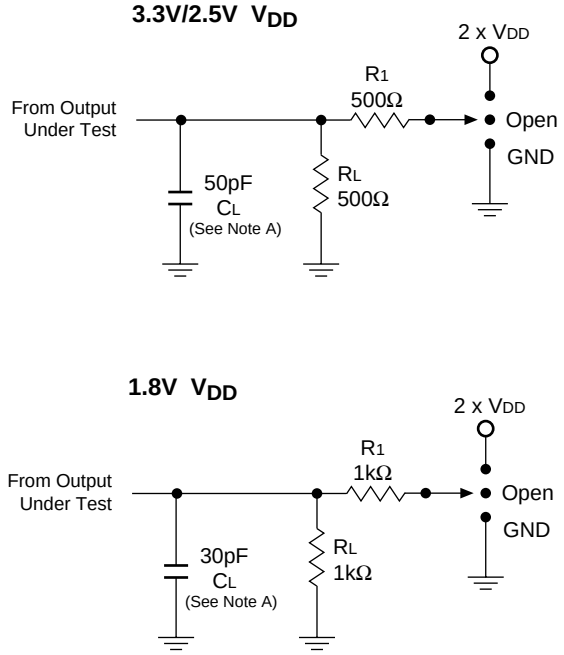
	V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
	Min	Max	Min	Max	Min	Max	
f_{clock} Clock Frequency		150		180		180	MHz
t_w Pulse duration, CLK high or low			3.0		3.0		ns
t_{su} Setup time, A before CLKAB↑, or B before CLKBA↑	2.5		2.0		1.6		
t_h Hold time, A after CLKAB↑, or B after CLKBA↑	0.0		0.0		0.5		

Switching Characteristics over recommended operating free-air temperature range
(unless otherwise noted, see Figures 1 thru 4)

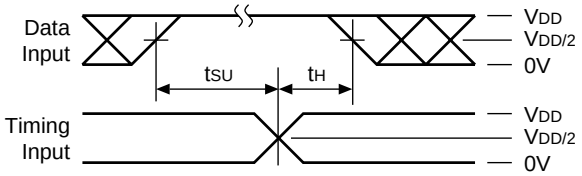
Parameters	From (Input)	To (Output)	V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{max}			150		180		180		MHz
t_{pd}	A or B	B or A	1.2	4.5	1.0	4.0	1.0	3.8	ns
	CLKAB or CLKBA	A or B	1.5	5.5	1.2	5.0	1.0	4.0	
	SAB or SBA	B or A	1.4	5.0	1.1	4.5	1.0	4.0	
t_{en}	$\overline{OE}$ or OE	A or B	1.4	5.0	1.6	5.0	1.6	4.0	
t_{dis}			1.5	5.5	2.0	5.0	2.0	4.0	

Test Circuits and Switching Waveforms

Parameter Measurement Information (V_{DD} = 1.65V - 3.6V)



Setup, Hold, and Release Timing



Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

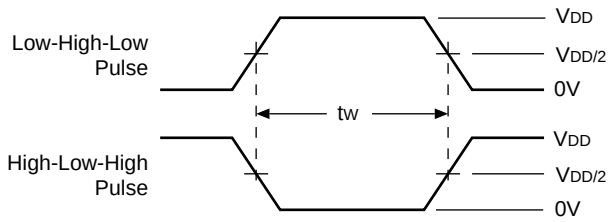
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns, ***measured from 10% to 90%, unless otherwise specified.***

D. The outputs are measured one at a time with one transition per measurement.

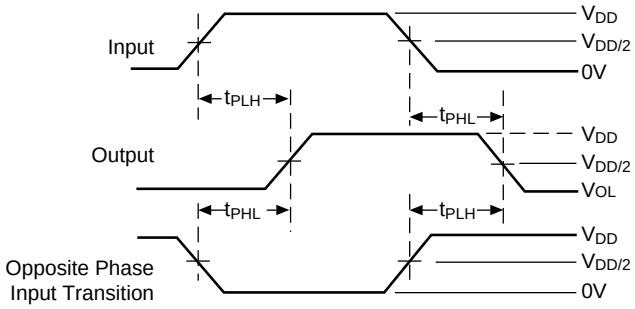
Switch Position

Test	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	2 x V_{DD}
t_{PHZ}/t_{PZH}	GND

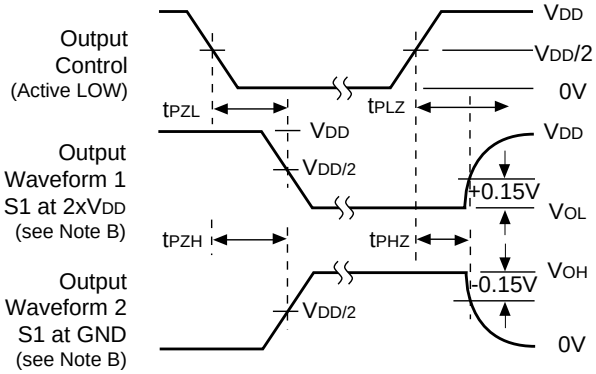
Pulse Width



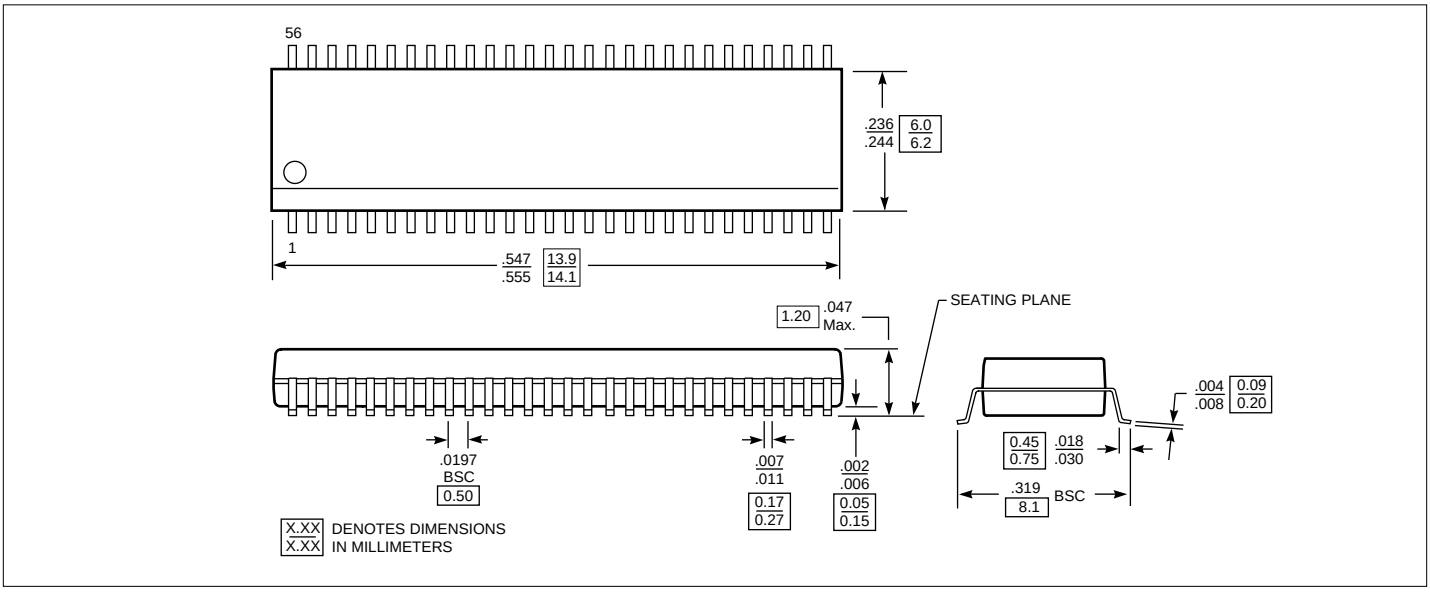
Propagation Delay



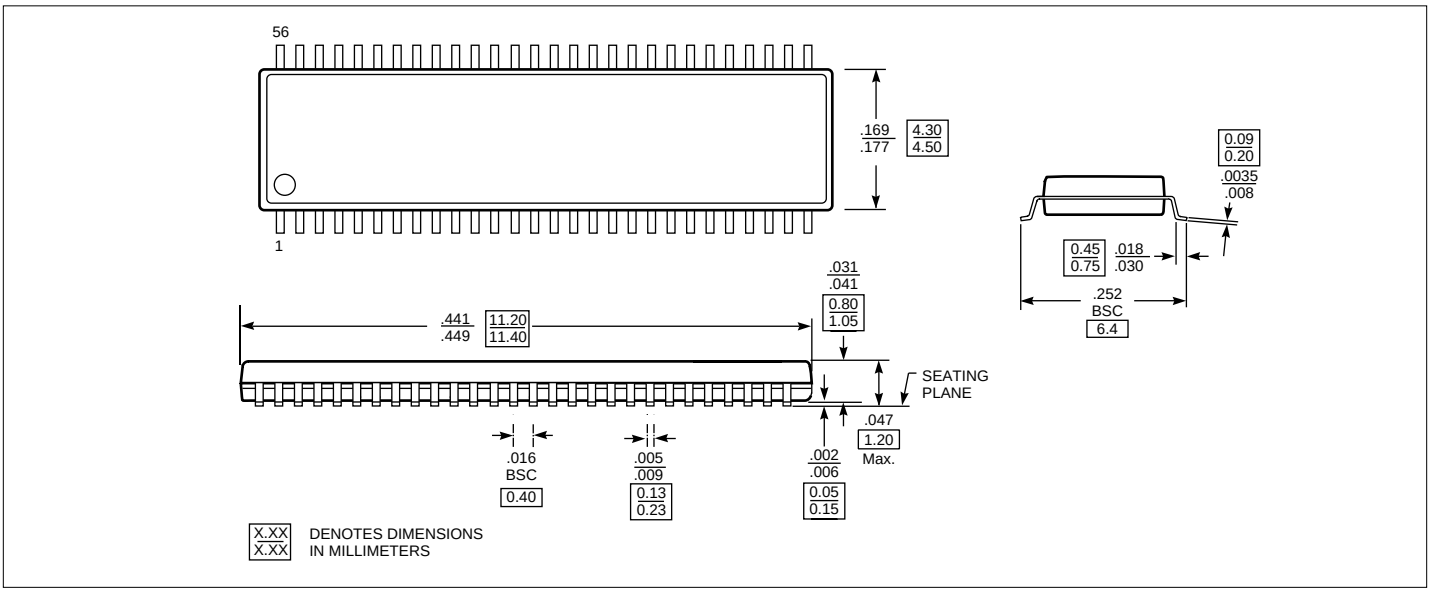
Enable Disable Timing



Packaging Mechanical: 56-pin TSSOP (A)



Packaging Mechanical: 56-pin TVSOP (K)



Ordering Information	Package - Pins
PI74ALVTC16652A	TSSOP - 56
PI74ALVTC16652K	TVSOP - 56

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