PI74ALVCH16835

18-Bit Universal Bus Driver with 3-STATE Outputs

Product Features

- PI74ALVCH16835 is designed for low voltage operation
- V_{CC} = 2.3V to 3.6V
- Hysteresis on all inputs
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) < 2.0V at V_{CC} = 3.3V, T_A = 25°C
- Bus Hold retains last active bus state during 3-STATE, eliminating the need for external pullup resistors
- Industrial operation at –40°C to +85°C
- Packages available:
  – 56-pin 240 mil wide plastic TSSOP (A)
  – 56-pin 300 mil wide plastic SSOP (V)
  – 56-pin 173 mil wide plastic TVSOP (K)

Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

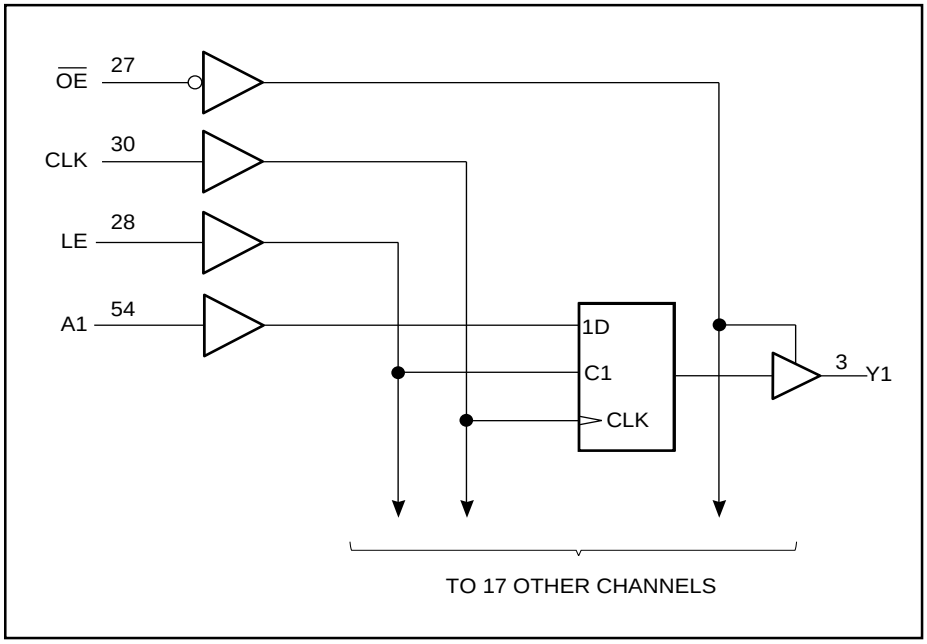
The 18-bit PI74ALVCH16835 universal bus driver is designed for 2.3V to 3.6V Vcc operation.

Data flow from A to Y is controlled by Output Enable ($\overline{OE}$). The device operates in the transparent mode when LE is HIGH. The A data is latched if CLK is held at a high or low logic level. If LE is LOW, the A-bus is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to Vcc through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

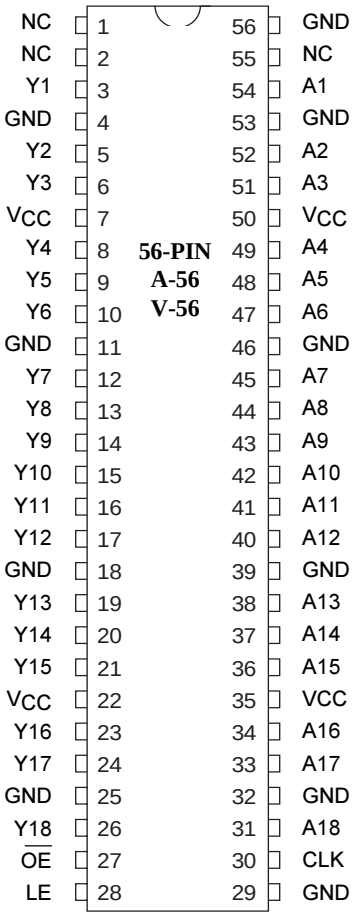
Logic Block Diagram



Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable
CLK	Clock Input
A	Data Input
Y	Data Output
GND	Ground
V_{CC}	Power

Product Pin Configuration



Truth Table[1]†

Inputs				Outputs
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_o[2]
L	L	L	X	Y_o[3]

Note:

1. H = High Signal Level
   L = Low Signal Level
   Z = High Impedance
   ↑ = Transition LOW-to-HIGH
   X= Irrelevant
2. Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low.
3. Output level before the indicated steady-state input conditions were established.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Input Voltage Range, V_{IN}	–0.5V to V_{CC} +0.5V
Output Voltage Range, V_{OUT}	–0.5V to V_{CC} +0.5V
DC Input Voltage	–0.5V to +5.0V
DC Output Current	100 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions(1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		2.3		3.6	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 2.7V to 3.6V	2.0			
V_{IL}	Input LOW Voltage	V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 2.7V to 3.6V			0.8	
V_{IN}	Input Voltage		0		V_{CC}	
V_{OUT}	Output Voltage		0		V_{CC}	
I_{OH}	High-level Output Current	V_{CC} = 2.3V			-12	mA
		V_{CC} = 2.7V			-12	
		V_{CC} = 3.0V			-24	
I_{OL}	Low-level Output Current	V_{CC} = 2.3V			12	
		V_{CC} = 2.7V			12	
		V_{CC} = 3.0V			24	
T_A	Operating Free-Air Temperature		-40		85	°C

Note:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 3.3V ± 10%)

Parameters	Test Conditions		V_{CC}[1]	Min.	Typ.[2]	Max.	Units
V_{OH}	I_{OH} = -100 µA		Min. to Max.	V_{CC} -0.2			V
	I_{OH} = -6 MA	V_{IH} = 1.7V	2.3V	2.0			
	I_{OH} = -12 mA	V_{IH} = 1.7V	2.3V	1.7			
		V_{IH} = 2.0V	2.7V	2.2			
		V_{IH} = 2.0V	3.0V	2.4			
	I_{OH} = -24 MA	V_{IH} = 2.0V	3.0V	2.0			
V_{OL}	I_{OL} = 100 µA		Min. to Max.			0.2	
	I_{OL} = 6 mA	V_{IL} = 0.7V	2.3V			0.4	
	I_{OL} = 12 MA	V_{IL} = 0.7V	2.3V			0.7	
		V_{IL} = 0.8V	2.7V			0.4	
	I_{OL} = 24 mA	V_{IL} = 0.8V	3.0V			0.55	
I_I	V_I = V_{CC} or GND		3.6V			±5	µA
I_I (Hold)[3]	V_I = 0.7V		2.3V	45			
	V_I = 1.7V			-45			
	V_I = 0.8V		3.0V	75			
	V_I = 2.0V			-75			
	V_I = 0 to 3.6V		3.6V			±500	
I_{OZ}[4]	V_O = V_{CC} or GND		3.6V			±10	
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6V			40	
ΔI_{CC}	One input at V_{CC} - 0.6V, Other inputs at V_{CC} or GND		3V to 3.6V			750	
C_I Control Inputs	V_I = V_{CC} or GND		3.3V		3.5		pF
Data Input	V_O = V_{CC} or GND		3.3V		6		
C_O Outputs	V_O = V_{CC} or GND		3.3V		7		

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Bus Hold maximum dynamic current required to switch the input from one state to another.
4. For I/O ports, the I_{OZ} includes the input leakage current.

Timing Requirements over Operating Range

Parameters	Description	V_{CC} = 2.5 V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3V ± 0.3V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLOCK}	Clock frequency	0	150	0	150	0	150	MHz
t_W Pulse Duration	LE high	3.3		3.3		3.3		ns
	CLK high or low	3.3		3.3		3.3		
t_{SU} Setup time	Data before CLK↑	2.2		2.1		1.7		
	Data before LE↓, CLK High	1.9		1.6		1.5		
	Data before LE↓, CLK Low	1.3		1.1		1		
t_H Hold time	Data after CLK↑	0.6		0.6		0.7		
	Data after LE↓, CLK High or Low	1.4		1.7		1.4		
$\Delta t/\Delta v$(1)	Input Transition Rise or Fall	0	10	0	10	0	10	ns/V

Note:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

Switching Characteristics Over Operating Range(1)

Parameters	From (INPUT)	To (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 2.7V		V_{CC} = 3.3 V ± 0.3V		Units
			Min.(2)	Max.	Min.(2)	Max.	Min.(2)	Max.	
f_{MAX}			150		150		150		MHz
t_{PD}	A	Y	1	4.2		4.2	1	3.6	ns
t_{PD}	LE	Y	1.3	5		4.9	1.3	4.2	
t_{PD}	CLK	Y	1.4	5.5		5.2	1.4	4.5	
t_{EN}	OE	Y	1.4	5.5		5.6	1.1	4.6	
t_{DIS}	OE	Y	1	4.5		4.3	1.3	3.9	

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Switching Characteristics, from 0ºC to 65ºC, CL = 50pF

Parameter	From (Input)	To (Output)	V_{CC} = 3.3V ± 0.15V		Units
			Min.	Max.	
t_{PD}	CLK	Y	1.7	4.5	ns

Operating Characteristics, T_A = 25ºC

Parameter		Test Conditions	V_{CC} = 2.5V ± 0.2V	V_{CC} = 3.3V ± 0.3V	Units
			Typical		
C_{PD} Power Dissipation Capacitance	Outputs Enabled	C_L = 50pF, f = 10 MHz	26	31	pF
	Outputs Disabled		12	14	