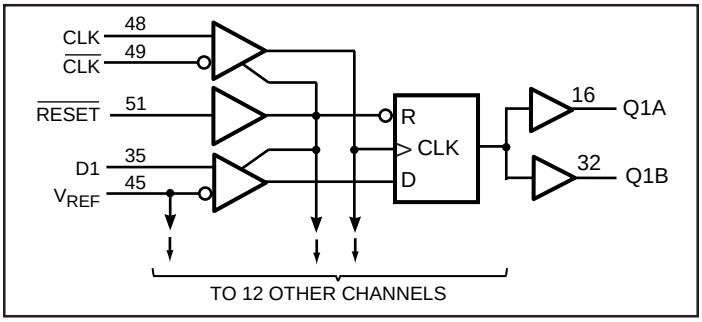
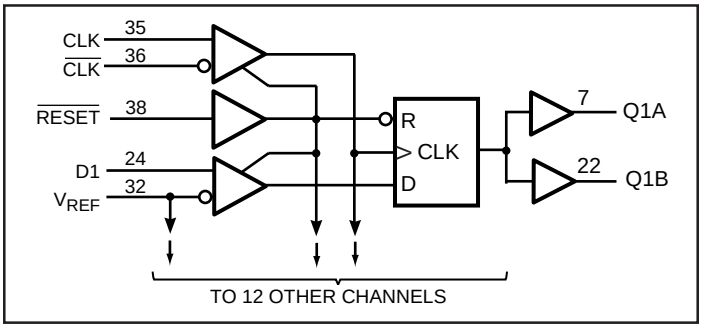
Product Features

- PI74 SSTV16859 is designed for low-voltage operation, $V_{DD} = V_{DDQ} = 2.3V$ to 2.7V
- Supports SSTL_2 Class II specifications on outputs
- All Inputs are SSTL_2 Compatible, except $\overline{RESET}$ which is LVCMOS.
- Designed for DDR Memory
- Flow-Through Architecture
- Packages (Lead-free packages are available):
  – 64-pin, 240-mil wide plastic TSSOP (A)
  – 56-contact, Plastic Very Thin Fine Pitch Quad Flat No Lead QFN (ZB)

Logic Block Diagram - TSSOP



Logic Block Diagram - QFN



Product Pin Description

Pin Name	Description
$\overline{RESET}$	Reset (Active Low) LVCMOS
CLK	Clock Input, Positive Differential Input
$\overline{CLK}$	Clock Input, Negative Differential Input
D	Data Input, D1-D13
Q	Data Output, Q1-Q13
GND	Ground
V_{DD}	Core Supply Voltage, 2.5V Nominal
V_{DDQ}	Output Supply Voltage, 2.5V Nominal
V_{REF}	Input Reference Voltage, 1.25V Nominal

Product Description

Pericom Semiconductor's PI74SSTV16859 logic circuit is produced using the Company's advanced 0.35 micron CMOS technology, achieving industry leading speed.

All inputs are compatible with the JEDEC standard for SSTL_2, except the LVCMOS reset ($\overline{RESET}$) input. All outputs are SSTL_2, Class II compatible.

The device operates from a differential clock (CLK and $\overline{CLK}$). Data registered at the crossing of CLK going HIGH, and $\overline{CLK}$ going LOW.

The PI74SSTV16859 supports low-power standby operation. When $\overline{RESET}$ is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is LOW, all registers are reset, and all outputs are forced LOW. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the LOW state during power up.

In the DDR DIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CLK and $\overline{CLK}$. Therefore, no timing relationship can be guaranteed between the two. When entering $\overline{RESET}$, the register will be cleared and the outputs will be driven LOW quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of $\overline{RESET}$, the register will become active quickly, relative to the time to enable the differential input receivers. When the data inputs are LOW, and the clock is stable, during the time from the LOW-to-HIGH transition of $\overline{RESET}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain LOW.

Pericom's PI74SSTV16859 is characterized for operation from 0°C to 70°C.

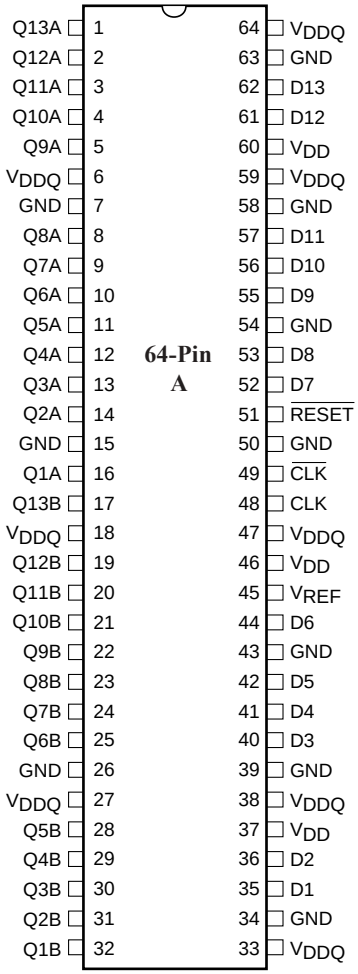
Truth Table[1]

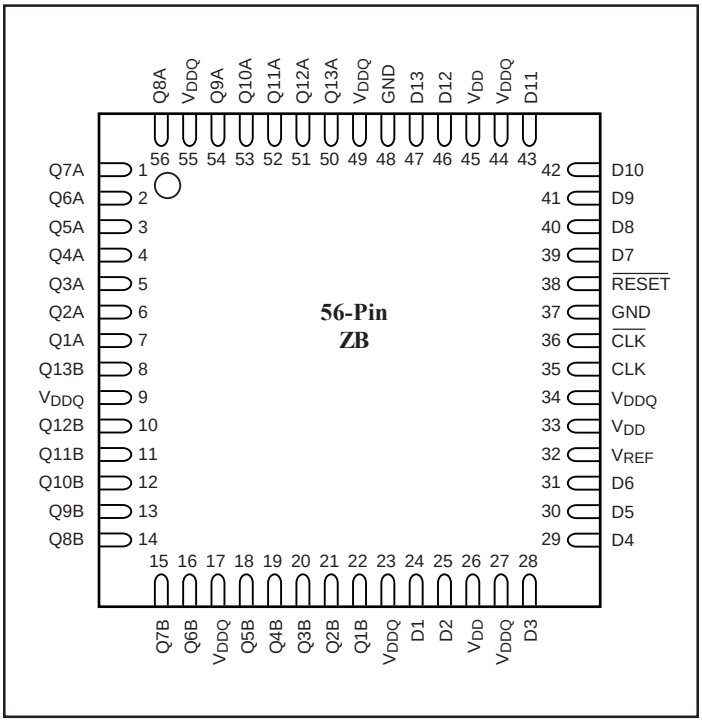
Inputs				Outputs
$\overline{RESET}$	CLK	$\overline{CLK}$	D	Q
L	X or Floating	X or Floating	X or Floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Qo[2]

Notes:

1. H = High Signal Level
   L = Low Signal Level
   ↑ = Transition LOW-to-HIGH
   ↓ = Transition HIGH-to-LOW
   X = Irrelevant or floating
2. Output level before the indicated steady state input conditions were established.

Product Pin Configurations





Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This value is limited to 3.6V Maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Symbol/ Conditions	Ratings	Units
Storage temperature	T_{stg}	–65 to 150	°C
Supply voltage	V_{DD} or V_{DDQ}	–0.5 to 3.6	V
Input voltage(1,2)	V_I	–0.5 to V_{DD} +0.5	V
Output voltage(1,2)	V_O	–0.5 to V_{DDQ} +0.5	V
Input clamp current	I_{IK}, V_I <0 or V_I >V_{DD}	±50	mA
Output clamp current	I_{OK}, V_O <0 or V_O >V_{DDQ}	±50	mA
Continuous output current	I_O, V_O = 0 to V_{DDQ}	±50	mA
V_{DD}, V_{DDQ} or GND current/pin	I_{DD}, I_{DDQ} or I_{GND}	±100	mA
Package Thermal Impedance(3)	θJ_A	55	°C/W

Recommended Operating Conditions(4)

Parameters	Description		Min.	Nom.	Max.	Units
V_{DD}	Supply Voltage		2.3	2.5	2.7	V
V_{DDQ}	I/O Supply Voltage		2.3	2.5	2.7	
V_{REF}	Reference Voltage V_{REF} = 0.5X V_{DDQ}		1.15	1.25	1.35	
V_{TT}	Termination Voltage		V_{REF} –0.04	V_{REF}	V_{REF} +0.04	
V_I	Input Voltage		0		V_{DD}	
V_{IH}	AC High -Level Input Voltage	Data Inputs	V_{REF} +310mV			
V_{IL}	AC Low -Level Input Voltage				V_{REF} – 310mV	
V_{IH}	DC High -Level Input Voltage		V_{REF} +150mV			
V_{IL}	DC Low -Level Input Voltage				V_{REF} –150mV	
V_{IH}	High -Level Input Voltage	$\overline{RESET}$	1.7			
V_{IL}	Low -Level Input Voltage				0.7	
V_{ICR}	Common-mode input range	CLK, $\overline{CLK}$	0.97		1.53	
V_{ID}	Differential Input Voltage		360			
I_{OH}	High-Level Output Current				–20	mA
I_{OL}	Low-Level Output Current				20	
T_A	Operating Free-Air Temperature		0		70	ºC

Note:
4. The $\overline{RESET}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

DC Electrical Characteristics

(Over the Operating Range, $T_A = 0°C$ to $+70°C$, $V_{DD} = 2.5V \pm 200mV$, $V_{DDQ} = 2.5V \pm 200mV$)

Parameters		Test Conditions	V_{DD}	Min.	Typ.	Max.	Units
V_{IK}		I_I = –18mA	2.3V			– 1.2	V
V_{OH}		I_{OH} = –100µA	2.3V- 2.7V	V_{DD}– 0.2			
		I_{OH}= –16mA	2.3V	1.95			
V_{OL}		I_{OL} =100µA	2.3V- 2.7V			0.2	
		I_{OH} =16mA	2.3V			0.35	
I_I	All Inputs	$V_I = V_{DD}$ or GND	2.7V			±5	µA
I_{DD}	Standby (Static)	$\overline{RESET}$ = GND	2.7V			10	
	Operating (Static)	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$				40	mA
I_{DDD}	Dynamic Operating clock only	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle			30		µA/ clock MHz
	Dynamic Operating per each data input	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle			10		µA/ clock MHz data input
r_{OH}	Output High	I_O= –20mA	2.3 to 2.7V	7		20	ohm
r_{OL}	Output Low	I_O= 20mA					
$r_{O(\Delta)}$	r_{OH}, r_{OL} each seperate bit	I_O= 20mA, TA = 25°C	2.5V			6	
C_I	Data Inputs	$V_I = V_{REF} \pm 350mV$		2.5	3	3.5	pF
	CLK and $\overline{CLK}$	V_{ICR}= 1.25V, $V_{I(PP)}$ = 360mV					
	$\overline{RESET}$	$V_I = V_{DD}$ or GND			3		

Timing Requirements (over recommended operating free-air temperature range, unless otherwise noted)

			V_{DD} = 2.5V ±0.2V		Units
			Min.	Max.	
f_{clock}	Clock frequency			200	MHz
t_W	Pulse Duration, CLK, $\overline{CLK}$ high or low		2.5		ns
t_{act}	Differential Inputs active time, data inputs must be low after $\overline{RESET}$ high.		22		ns
t_{inact}	Differential Inputs inactive time, data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ Low.				ns
t_{su}	Setup time, fast slew rate(5,7)	Data before CLK↑, $\overline{CLK}$↓	0.75		ns
	Setup time, slow slew rate(6,7)		0.9		ns
t_h	Hold time, fast slew rate(5,7)	Data after CLK↑, $\overline{CLK}$↓	0.75		ns
	Hold time, slow slew rate(6,7)		0.9		ns

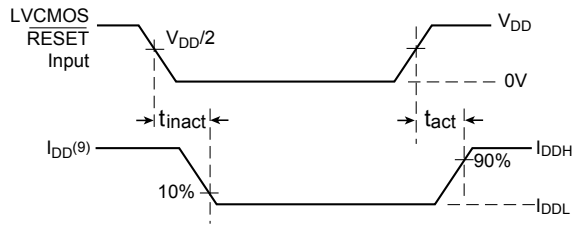
Notes: 5. For data signal input slew rate ≥1V/ns.
6. For data signal input slew rate ≥0.5V/ns and <1V/ns.
7. CLK, $\overline{CLK}$ signals input slew rates are ≥1V/ns.

Switching characteristics

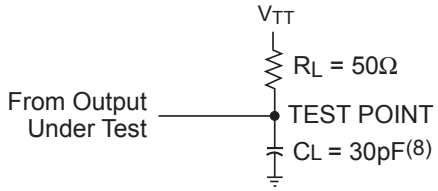
Over recommended operating free-air temperature range, unless otherwise noted. (See test circuits and switching waveforms).

Parameter	From (Input)	To (Output)	V_{DD} = 2.5V ±0.2V			Units
			Min.	Typ.	Max.	
f_{max}			200			MHz
t_{pd}	CLK, $\overline{CLK}$	Q	1.1		2.8	ns
t_{phl}	$\overline{RESET}$	Q			5.0	ns

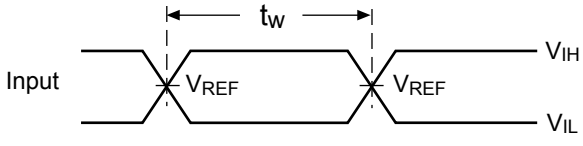
Test Circuit and Switching Waveforms



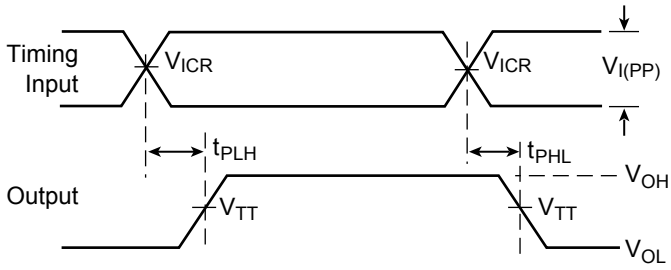
Voltage and Current Waveforms
Input Active and Inactive Times



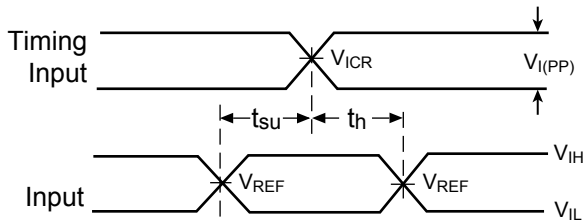
Load Circuit



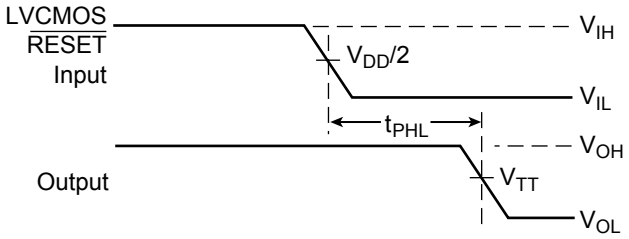
Voltage Waveforms - Pulse Duration



Voltage Waveforms - Propagation Delay Times



Voltage Waveforms - Setup and Hold Times



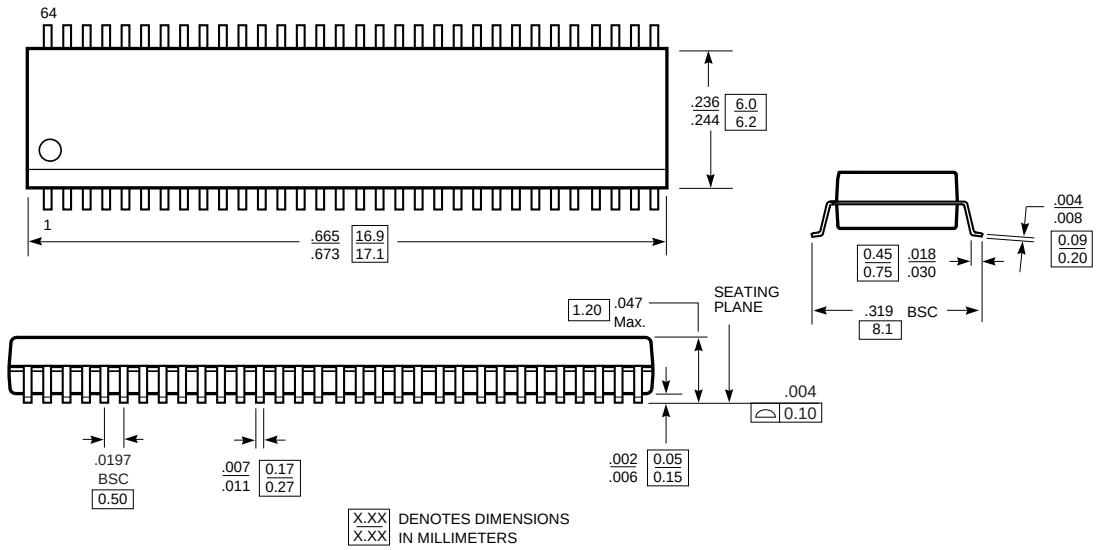
Voltage Waveforms - Propagation Delay Times

Parameter Measurement Information (V_{DD} = 2.5V ±0.2V)

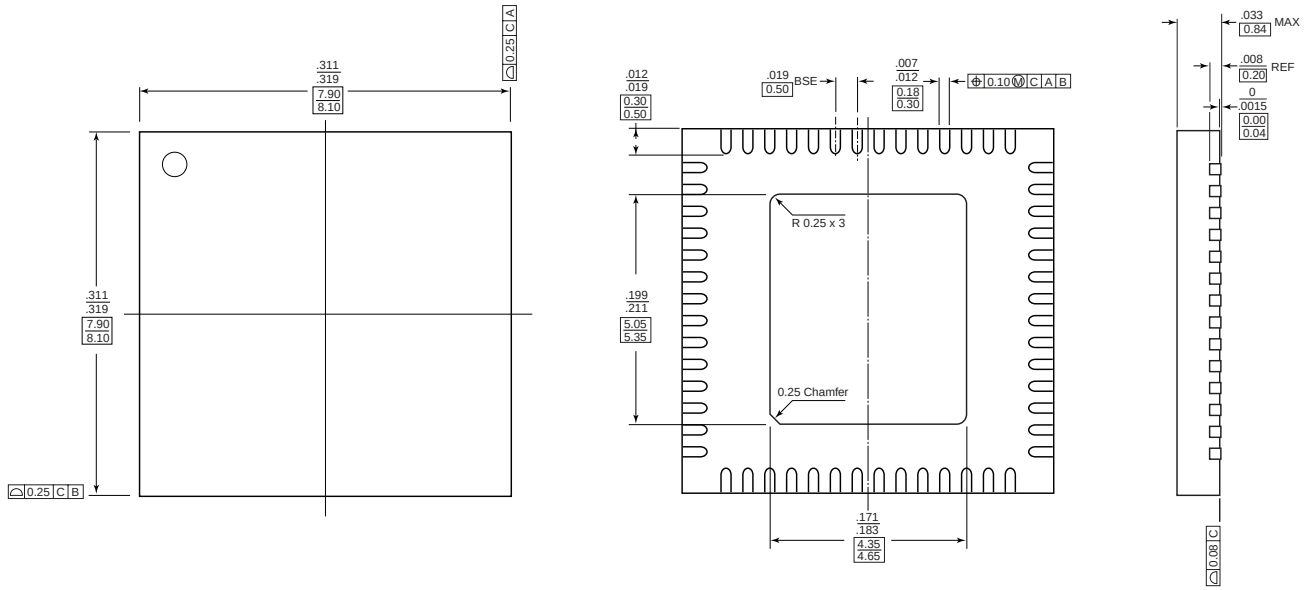
Notes:

8. C_L includes probe and jig capacitance.
9. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA.
10. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 ohms. Input slew rate = 1V/ns ±20% (unless otherwise specified).
11. The outputs are measured one at a time with one transition per measurement.
12. $V_{TT} = V_{REF} = V_{DDQ}/2$
13. $V_{IH} = V_{REF} + 350mV$ (ac voltage levels) for SSTL inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
14. $V_{IL} = V_{REF} + 350mV$ (ac voltage levels) for SSTL inputs. V_{IL} = GND for LVCMOS input.
15. t_{PLH} and t_{PHL} are the same as t_{pd}.

64-Pin TSSOP (A) Package



56-Contact QFN (ZB) Package



Notes:
1. Controlling dimensions in millimeters
2. Ref: JEDEC MO-220 variation VLLD-2

Ordering Information

Ordering Code	Package Type	Temperature Range
PI74SSTV16859A	64-Pin TSSOP	0°C to 70°C
PI74SSTV16859AE	Pb-free, 64-Pin TSSOP	
PI74SSTV16859ZB	56-contact QFN	
PI74SSTV16859ZBE	Pb-free, 56-contact QFN	