

Product Features:

Common Features:

- PI74FCT16511 and PI74FCT162511 are high-speed, low power devices with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Typical $t_{sk(o)}$ (Output Skew) < 250 ps, clocked mode
- Extended range of $-40^{\circ}C$ to $+85^{\circ}C$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide TSSOP (A)
 - 56-pin 300 mil wide SSOP (V)

PI74FCT16511T Features:

- High output drive: $I_{OH} = -32$ mA; $I_{OL} = 64$ mA
- Power off disable outputs permit “live insertion”
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}C$

PI74FCT162511T Features:

- High output drive: $I_{OL}/I_{OH} = 24$ mA
- Open drain parity error allows wire-OR
- Typical V_{OLP} (Output Ground Bounce) < 1.0V at $V_{CC} = 5V$, $T_A = 25^{\circ}C$
- Balanced output drivers: ± 24 mA
- Series current limiting resistors

Fast CMOS 16-Bit Registered/Latched Transceiver With Parity

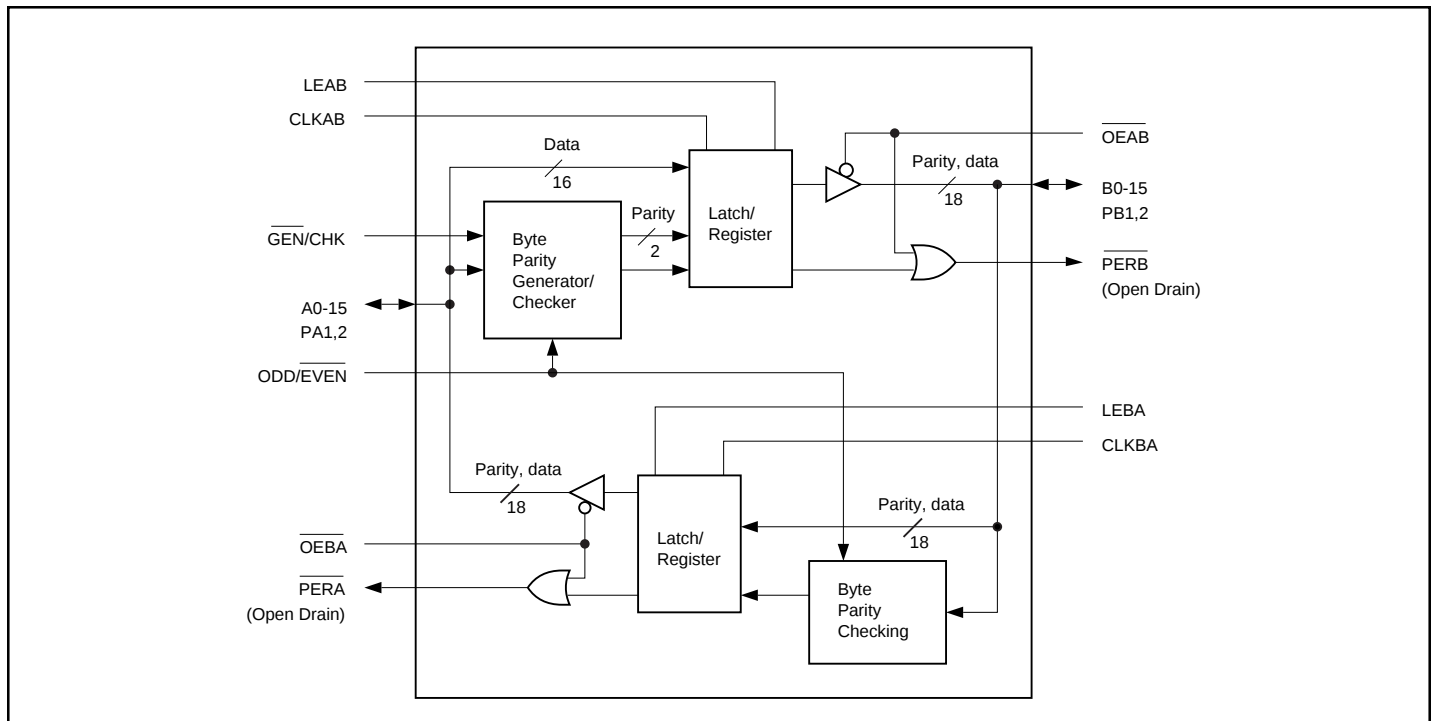
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

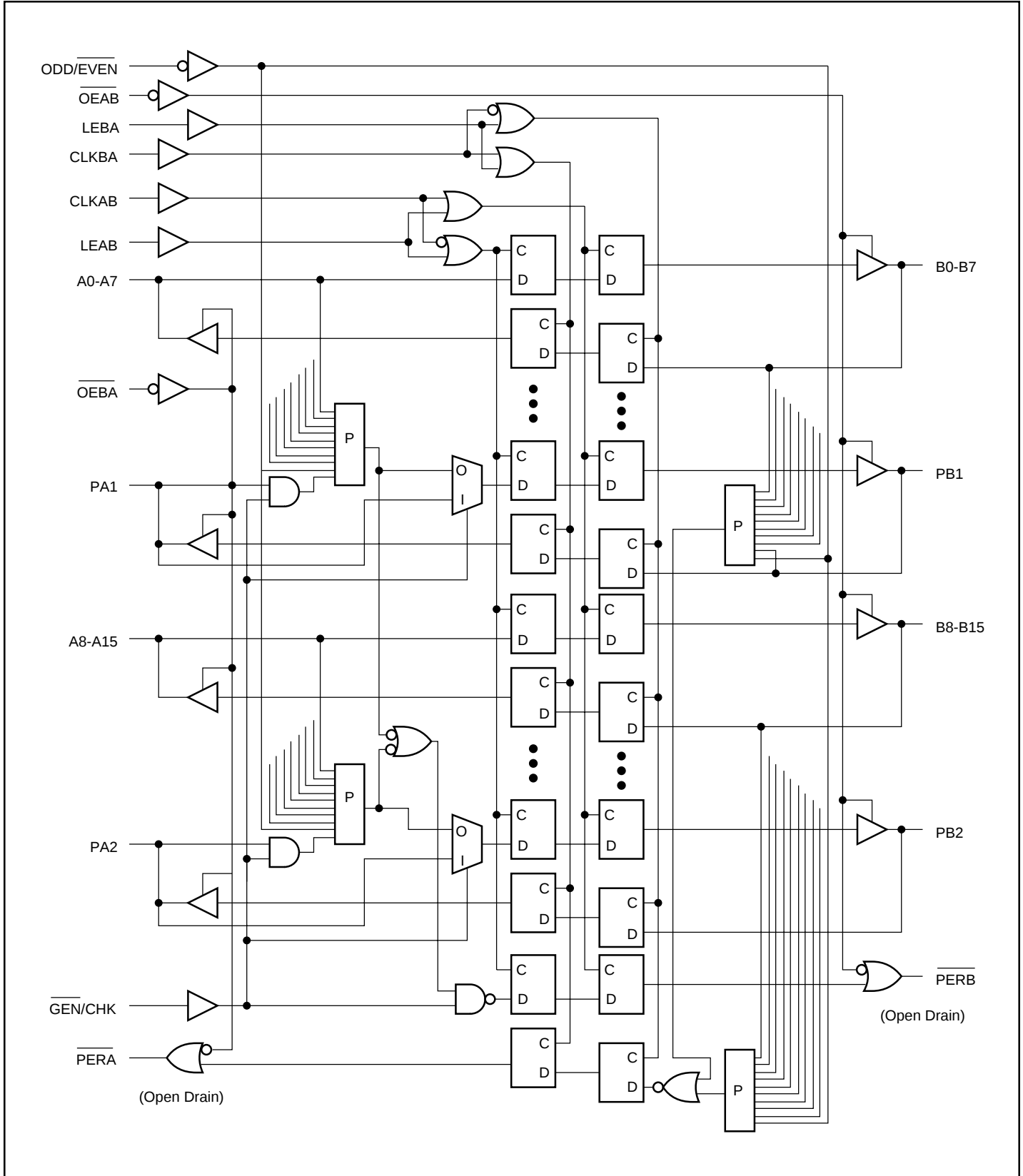
The PI74FCT16511T and PI74FCT162511T are high-speed, low-power 16-bit registered/latched transceiver with parity which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched or clocked modes. It has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. One error flag for each direction (A-to-B or B-to-A) exists to indicate an error for either byte in either direction. The parity error flags which are open drain outputs, can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. To disable the error flag during combinational transitions, a designer can disable the parity error flag by the $\overline{OE_{xx}}$ control pins.

The operation in A-to-B direction is controlled by LEAB, CLKAB and $\overline{OEAB}$ control pins, and the operation in B-to-A direction is controlled by LEBA, CLKBA and $\overline{OEBA}$ control pins. $\overline{GEN}/CHK$ is used to select the operation of A-to-B direction, while B-to-A direction is always in checking mode. The ODD/ $\overline{EVEN}$ select is common between the two directions. Independent operation can be achieved between the two directions by using the corresponding control lines except for the ODD/ $\overline{EVEN}$ control.

Simplified Logic Block Diagram



Logic Block Diagram



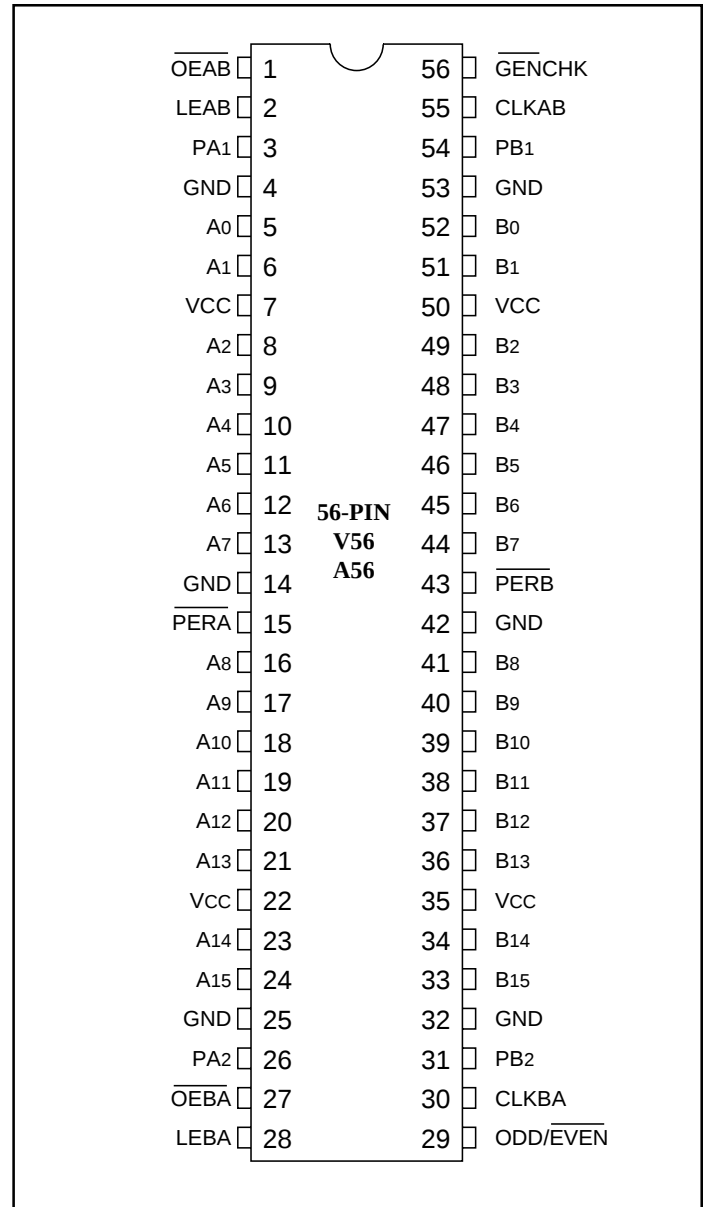
Product Pin Description

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{PERA}$	Parity Error (Open Drain) on A Outputs
$\overline{PERB}$	Parity Error (Open Drain) on B Outputs
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or B-to-A 3-State Outputs
ODD/EVEN ⁽¹⁾	Parity Mode Selection Input
$\overline{GEN/CHK}$ ⁽¹⁾	A-to-B Port Generate or Check Mode Input
PAx ⁽²⁾	A-to-B Parity Input, B-to-A Parity Output
PBx	B-to-A Parity Input, A-to-B Parity Output
GND	Ground
VCC	Power

NOTES:

1. ODD/EVEN and $\overline{GEN/CHK}$ should be tied to VCC or GND with no resistor for optimum results.
2. The PAx pin input is internally disabled during parity generation. This means that when generating parity in the A-to-B direction, there is no need to add a pull-up resistor to guarantee state. The pin will still function properly as the parity output for the B-to-A direction.

Product Pin Configuration



Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	5.5	8.0	pF
C _O	Open Drain Capacitance	V _{OUT} = 0V	4.5	6.0	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

Truth Table^(1,2)

Inputs				Output Buffers
OEAB	LEAB	CLKAB	A _x	B _x
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B ⁽³⁾
L	L	H	X	B ⁽⁴⁾

NOTES:

- H = High Voltage Level
L = Low Voltage Level
X = Don't Care or Irrelevant
Z = High Impedance
↑ = LOW-to-HIGH Transition
- A-to-B data flow is shown. B-to-A flow control is the same, except using OEBA, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, assuming CLKAB was HIGH before LEAB went LOW.

Truth Table (Parity Generation) (1, 2, 3, 4, 5)

A0 - A7, Total Number of Inputs that are high	ODD/EVEN	PB1
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:

- Conditions shown are for $\overline{\text{GEN/CHK}} = \text{L}$, $\overline{\text{OEAB}} = \text{L}$, $\overline{\text{OEBA}} = \text{H}$.
- A-to-B parity generation is shown. B-to-A can check parity while A-to-B is performing generation. B-to-A will not generate parity.
- The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
- Conditions shown are for the byte A0-A7. The byte A8-A15 is similar but will output the parity on PB2.
- The error flag $\overline{\text{PERB}}$ will remain in a high state during parity generation.

Truth Table (Parity Checking) (1, 2, 3, 4)

A0 - A7 and PA1 ⁽⁵⁾ , Total Number of Inputs that are high	ODD/EVEN	PERB
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H ⁽⁶⁾
0, 2, 4, 6 or 8	L	H ⁽⁶⁾
0, 2, 4, 6 or 8	H	L

NOTES:

- Conditions shown are for $\overline{\text{GEN/CHK}} = \text{H}$, $\overline{\text{OEAB}} = \text{L}$, $\overline{\text{OEBA}} = \text{H}$.
- A-to-B parity checking is shown. B-to-A parity checking is same but uses $\overline{\text{OEBA}} = \text{L}$, $\overline{\text{OEAB}} = \text{H}$ and errors will be indicated on PERA.
- In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors. (PB1 = PA1)
- The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
- Conditions shown are for the byte A0-A7 and PA1. The byte A8-A15 and PA2 is same.
- The parity error flag $\overline{\text{PERB}}$ is a combined flag for both bytes A0-A7 and A8-A15. If a parity error occurs on either byte $\overline{\text{PERB}}$ will go low.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level			0.8	V
I _{IH}	Input HIGH Current (Input pins) (I/O pins)	V _{CC} = Max. V _{IN} = V _{CC}			1 –1	μA
I _{IL}	Input LOW Current (Input pins) (I/O pins)	V _{CC} = Max. V _{IN} = GND			1 –1	μA
I _{OZH}	High Impedance	V _{CC} = Max. V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{OUT} = 0.5V			–1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = –18 mA		–0.7	–1.2	V
I _{OS}	Short Circuit Current (I/O pins)	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND	–80	–140	–225	mA
I _O	Output Drive Current (I/O pins)	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V	–50		–180	mA
I _{OFF}	Output Leakage Current (Open Drain)	V _{CC} = Max., V _{OUT} = 4.5V			±100	μA
V _H	Input Hysteresis			100		mV

PI74FCT16511T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}				V
		I _{OH} = –3.0 mA	2.5	3.5		
		I _{OH} = –15.0 mA	2.4	3.5		
		I _{OH} = –32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.2	0.55	V
		I _{OL} = 64 mA				
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V	—	—	±100	μA

PI74FCT162511T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}				V
		I _{OH} = –24.0 mA	2.4	3.3		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}		0.3	0.55	V
		I _{OL} = 24 mA				
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾	–60	–115	–150	mA

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
ICCL, ICCH, ICCZ	Quiescent Power Supply Current	VCC = Max.	VIN = GND or VCC		0.1	500	μA
ΔICC	Supply Current per Input @ TTL HIGH	VCC = Max.	VIN = 3.4V ⁽³⁾		0.5	1.5	mA
ICCD	Supply Current per Input per MHz ⁽⁴⁾	VCC = Max., Outputs Open OEAB = GND OEBA = VCC One Bit Toggling 50% Duty Cycle	VIN = VCC VIN = GND		75	120	μA/MHz
IC	Total Power Supply Current ⁽⁶⁾	VCC = Max., Outputs Open fCP = 10 MHz (CLKAB) 50% Duty Cycle LEAB = OEAB = GND OEBA = VCC fi = 5 MHz One Bit Toggling	VIN = VCC VIN = GND		0.8	1.7 ⁽⁵⁾	mA
			VIN = 3.4V VIN = GND		1.3	3.2 ⁽⁵⁾	
		VCC = Max., Outputs Open fCP = 10 MHz (CLKAB) 50% Duty Cycle LEAB = OEAB = GND OEBA = VCC fi = 2.5 MHz 18 Bits Toggling	VIN = VCC VIN = GND		3.8	6.5 ⁽⁵⁾	
			VIN = 3.4V VIN = GND		9.0	21.8 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
- IC = IQUIESCENT + IINPUTS + IDYNAMIC
IC = ICC + ΔICC DHNT + ICCD (fCP/2 + fiNi)
ICC = Quiescent Current
ΔICC = Power Supply Current for a TTL High Input (VIN = 3.4V)
DH = Duty Cycle for TTL Inputs High
NT = Number of TTL Inputs at DH
ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
fCP = Clock Frequency for Register Devices (Zero for Non-Register Devices)
fi = Input Frequency
Ni = Number of Inputs at fi
All currents are in milliamps and all frequencies are in megahertz.

16511T/162511T Switching Characteristics over Operating Range (Propagation Delays)

Parameters	Description	Conditions ⁽¹⁾	16511/162511T		162511AT		Unit
			Com.		Com.		
			Min	Max	Min	Max	
tPLH tPHL	Propagation Delay PAx to PBx	CL = 50 pF RL = 500Ω	1.5	6.5	1.5	5.7	ns
tPLH tPHL	Propagation Delay Ax to Bx or Bx to Ax, PBx to PAx		1.5	6.5	1.5	5.0	ns
tPLH tPHL	Propagation Delay Ax to PBx		1.5	9.0	1.5	7.5	ns
tPLH ⁽³⁾ tPHL	Propagation Delay Ax to $\overline{\text{PERB}}$, PAx to $\overline{\text{PERB}}$		1.5	10.5	1.5	9.0	
			1.5	9.5	1.5	8.0	ns
tPLH ⁽³⁾ tPHL	Propagation Delay Bx to $\overline{\text{PERA}}$, PBx to $\overline{\text{PERA}}$		1.5	10.5	1.5	9.0	ns
			1.5	9.5	1.5	8.0	
tPLH tPHL	Propagation Delay LEBA to Ax and PAx LEAB to Bx and PBx		1.5	6.0	1.5	5.6	ns
tPLH ⁽³⁾ tPHL	Propagation Delay LEBA to $\overline{\text{PERA}}$, LEAB to $\overline{\text{PERB}}$		1.5	7.5	1.5	7.0	ns
			1.5	6.5	1.5	6.0	
tPLH tPHL	Propagation Delay CLKBA to Ax and PAx CLKAB to Bx and PBx		1.5	6.0	1.5	5.6	ns
tPLH ⁽³⁾ tPHL	Propagation Delay CLKBA to $\overline{\text{PERA}}$ CLKAB to $\overline{\text{PERB}}$		1.5	7.5	1.5	7.0	ns
			1.5	6.5	1.5	6.0	
tPZH tPZL	Output Enable Time $\overline{\text{OEBA}}$ to Ax and PAx $\overline{\text{OEAB}}$ to Bx and PBx		1.5	7.0	1.5	6.0	ns
tPHZ tPLZ	Output Disable Time ⁽⁴⁾ $\overline{\text{OEBA}}$ to Ax and PAx $\overline{\text{OEAB}}$ to Bx and PBx		1.5	7.0	1.5	5.6	ns
tPLZ ⁽³⁾ tPZL	Parity ERROR Enable $\overline{\text{OEBA}}$ to $\overline{\text{PERA}}$, $\overline{\text{OEAB}}$ to $\overline{\text{PERB}}$		1.5	6.0	1.5	6.0	ns
		1.5	6.0	1.5	6.0		
tPLH tPHL	ODD/ $\overline{\text{EVEN}}$ to $\overline{\text{PERB}}$	1.5	10.0	1.5	10.0	ns	
		1.5	10.0	1.5	10.0		
tPLH tPHL	ODD/ $\overline{\text{EVEN}}$ to PBx	1.5	10.0	1.5	10.0	ns	

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. On Open Drain Outputs t_{PLH} is measured up to V_{OUT} = V_{OL} + 0.3V.
4. This parameter is guaranteed but not production tested.

PI74FCT16511T/162511T Switching Characteristics over Operating Range (Setup Times)

Parameters	Description	Conditions ^(1,3)			16511/162511T		162511AT		Unit
					Com.		Com.		
					Min.	Max.	Min.	Max.	
tsu	Setup Time HIGH or LOW Ax to CLKAB	$\overline{\text{GEN}}/\text{CHK LOW}$	PBx valid	CL = 50 pF RL = 500Ω	6.5	—	4	—	ns
			PBx not valid		3	—	3	—	ns
		$\overline{\text{GEN}}/\text{CHK HIGH}$	PERB valid		6.5	—	4	—	ns
			PERB not valid		3	—	3	—	ns
tsu	Setup Time PAx to CLKAB	$\overline{\text{GEN}}/\text{CHK HIGH}$	PERB valid		6.5	—	4	—	ns
			PERB not valid		3	—	3	—	ns
tsu	Setup Time Bx to CLKBA PBx to CLKBA		PERA valid		6.5	—	4	—	ns
			PERA not valid		3	—	3	—	ns
tsu	Setup Time Ax to LEAB	CLKAB LOW	PBx valid		6.5	—	3.5	—	ns
		$\overline{\text{GEN}}/\text{CHK LOW}$	PBx not valid		3	—	3	—	ns
		CLKAB LOW	PERB valid		6.5	—	3.5	—	ns
		$\overline{\text{GEN}}/\text{CHK HIGH}$	PERB not valid		3	—	3	—	ns
		CLKAB HIGH	PBx valid	6.5	—	3.5	—	ns	
		$\overline{\text{GEN}}/\text{CHK LOW}$	PBx not valid	3	—	3	—	ns	
		CLKAB HIGH	PERB valid	6.5	—	3.5	—	ns	
		$\overline{\text{GEN}}/\text{CHK HIGH}$	PERB not valid	3	—	3	—	ns	
tsu	Setup Time PAx to LEAB	CLKAB LOW	PERB valid	6.5	—	3.5	—	ns	
		$\overline{\text{GEN}}/\text{CHK HIGH}$	PERB not valid	3	—	3	—	ns	
		CLKAB HIGH	PERB valid	6.5	—	3.5	—	ns	
		$\overline{\text{GEN}}/\text{CHK HIGH}$	PERB not valid	3	—	3	—	ns	
tsu	Setup Time Bx to LEBA PBx to LEBA	CLKBA LOW	PERA valid	6.5	—	3.5	—	ns	
			PERA not valid	3	—	3	—	ns	
		CLKAB HIGH	PERA valid	6.5	—	3.5	—	ns	
			PERA not valid	3	—	3	—	ns	

CL = 50 pF
RL = 500Ω

PI74FCT16511T/162511T Switching Characteristics over Operating Range (Hold Times)

Parameters	Description	Conditions ⁽¹⁾	16511/162511T		16511/162511AT		Unit
			Com.		Com.		
			Min.	Max.	Min.	Max.	
t _H	Hold Time HIGH or LOW A _x to LEAB, B _x to LEBA	C _L = 50 pF R _L = 500Ω	1	—	1	—	ns
t _H	Hold Time HIGH or LOW P _{Ax} to LEAB		1	—	1	—	ns
t _H	Hold Time HIGH or LOW P _{Bx} to LEBA		1	—	1	—	ns
t _H	Hold Time A _x to CLKAB, P _{Ax} to CLKAB		1	—	1	—	ns
t _H	Hold Time B _x to CLKBA, P _{Bx} to CLKBA		1	—	1	—	ns
t _w	LEAB or LEBA Pulse Width HIGH ⁽²⁾		3	—	3	—	ns
t _w	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽²⁾		3	—	3	—	ns

Notes:

1. See test circuit and wave forms.
2. This parameter is guaranteed but not production tested.
3. “Not valid” means the setup time indicated is not sufficient to assure proper functioning of this output; however, the set-up time indicated will assure proper functioning of the A-to-B or B-to-A port respective to the indicated direction.

Pericom Semiconductor Corporation

2380 Bering Drive • San Jose, CA 95131 • 1-800-435-2336 • Fax (408) 435-1100 • <http://www.pericom.com>