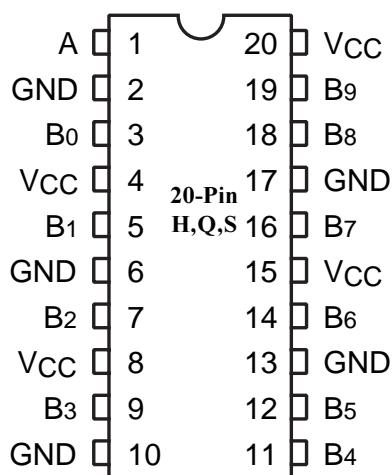


Features

- Low skew:<200ps
- Fast switching frequency>133 MHz
- Fast output rise/fall time < 1.5ns
- Low propagation delay < 2.5ns
- Low input capacitance < 6.0pF
- 5V I/O Tolerant input
- Rail-to-Rail CMOS outputs
- Industrial Temperature: -40°C to +85°C
- 3.3V±10% operation
- Packages available:
 - 20-pin 300mil wide SOIC (S)
 - 20-pin 150mil wide QSOP (Q)
 - 20-pin 209mil wide SSOP (H)

Product Pin Configuration



Product Pin Description

Pin Name	Description
A	Input
B ₀ -B ₉	Outputs
GND	Ground
V _{CC}	Power

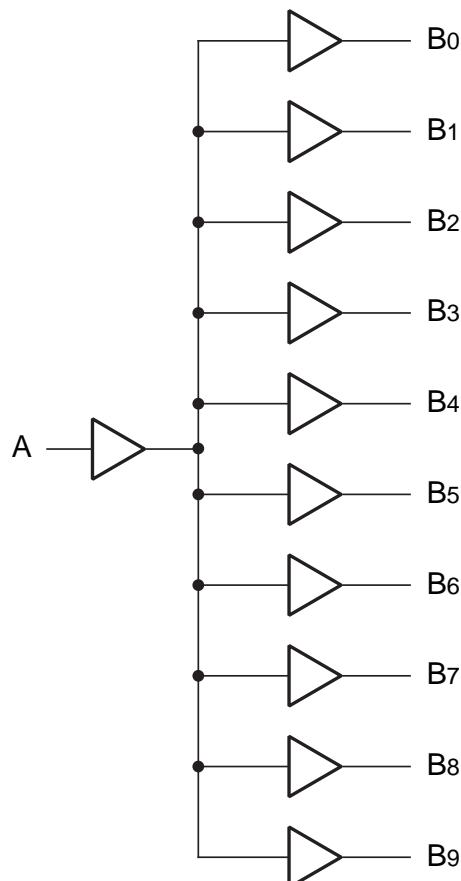
Description

Pericom Semiconductor's PI49FCT series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving speeds up to 133 MHz, low-power dissipation, and output skew less than 250ps.

The PI49FCT32807 is a 3.3V very low-skew clock buffer that produces ten outputs from a single low-capacitance input. Excellent output signals to power and ground ratio minimize power and ground noise, and also improves output performance.

The PI49FCT32807 integrates series damping resistors on all outputs.

Logic Block Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range)

Symbol	Description	Test Conditions ⁽¹⁾		Min.	Typ.	Max.	Units
V _{OH}	Output HIGH voltage	V _{CC} =3V V _{IN} =V _{IH} or V _{IL}	I _{OH} = -8mA	2.4	3.0	—	V
V _{OL}	Output LOW voltage	V _{CC} =3V V _{IN} =V _{IH} or V _{IL}	I _{OL} = 12mA	—	0.4	0.5	
V _{IH}	Input HIGH voltage	Guaranteed Logic HIGH Level (Input Pins)		2.0	—	5.5	
V _{IL}	Input LOW voltage	Guaranteed Logic LOW Level (Input Pins)		-0.5	—	0.8	
I _{IH}	Input HIGH current	V _{CC} = 3.6V	V _{IN} = 3.6V	—	—	1	μA
I _{IL}	Input LOW current	V _{CC} = 3.6V	V _{IN} = 0V	—	—	-1	
V _{IK}	Clamp diode voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OH}	Output HIGH current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽⁵⁾		-25	-45	-80	mA
I _{OL}	Output LOW current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽⁵⁾		25	45	90	
I _{OS}	Short circuit current ⁽⁵⁾	V _{CC} = Max., V _{OUT} = GND ⁽⁵⁾		-50	-100	-180	
V _H	Input Hysteresis			—	150	—	mV
R _S	Input Hysteresis			—	22	—	Ohm

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. V_{OH} = V_{CC} - 0.6V at rated current.
4. This parameter is determined by device characterization but is not production tested.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max.	V _{IN} =GND or V _{CC}	—	0.1	30	μA
ΔI _{CC}	Supply Current per Inputs @ TTL HIGH	V _{CC} =Max.	V _{IN} =V _{CC} −0.6V ⁽³⁾	—	47	300	μA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} =Max., Outputs Open Per Output Toggling 50% Duty Cycle	V _{IN} =V _{CC} V _{IN} =GND	—	0.08	0.16	mA/MHz

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC}=3.3V, +25°C ambient.
3. Per TTL driven input (V_{IN}=V_{CC}−0.6V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.

Capacitance (T_A=25°C, f=1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} =0V	3.0	4	pF
C _{OUT}	Output Capacitance	V _{OUT} =0V		6	pF

Notes:

1. This parameter is determined by device characterization but is not production tested.

Maximum Switching Characteristics (Over operating range)

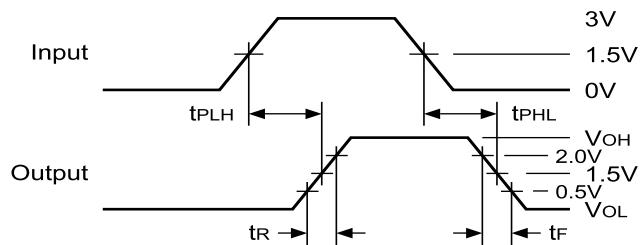
Symbol	Description	Condition	Max.	Units
t _{PLH} t _{PHL}	Propagation Delay A to B ⁽³⁾	C _L =15pF 0.8V –2.0V CL=15pF	2.5	ns
t _{R/t_F}	Rise/Fall Time ⁽²⁾		1.5	
t _{SK(p)}	Pulse Skew (same pkg) ^(1,2)		0.35	
t _{SK(o)}	Output Skew (same pkg.) ^(1,2)		0.20	
t _{SK(t)}	Output Skew (different pkg.) ^(1,2)		0.55	
F _{IN}	Input Frequency ^(1,2)		133	MHz

Notes:

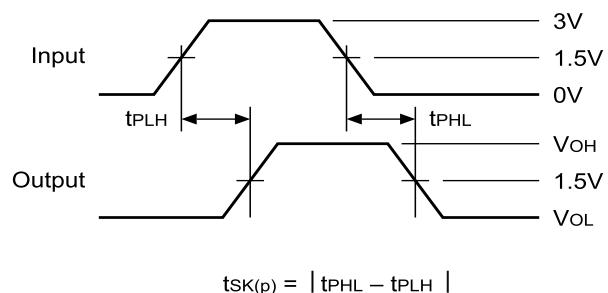
1. Other loading condition is described on page 4, "Test Circuits for All Outputs."
2. These parameters are guaranteed by design.
3. Minimum propagation delay of 1.5ns is guaranteed by design.

SWITCHING WAVEFORMS

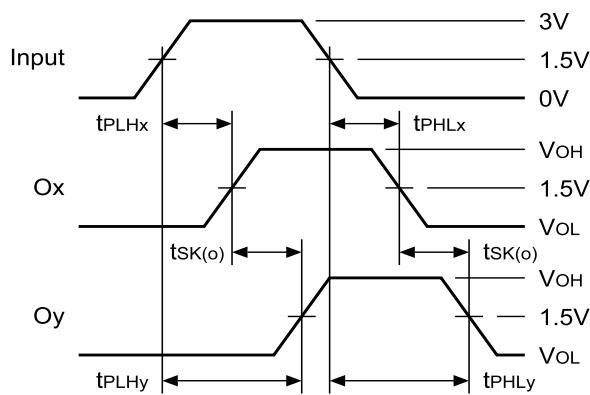
Propagation Delay



Pulse Skew – $t_{SK(p)}$

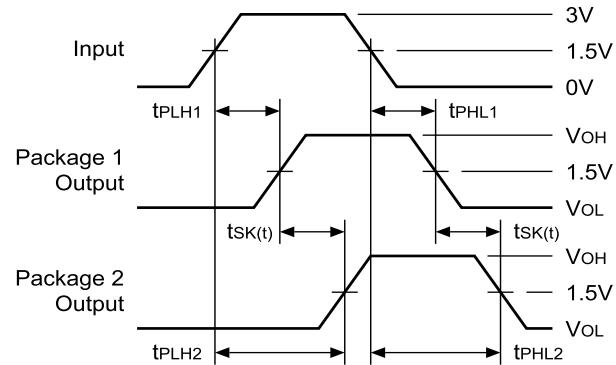


Output Skew – $t_{SK(o)}$



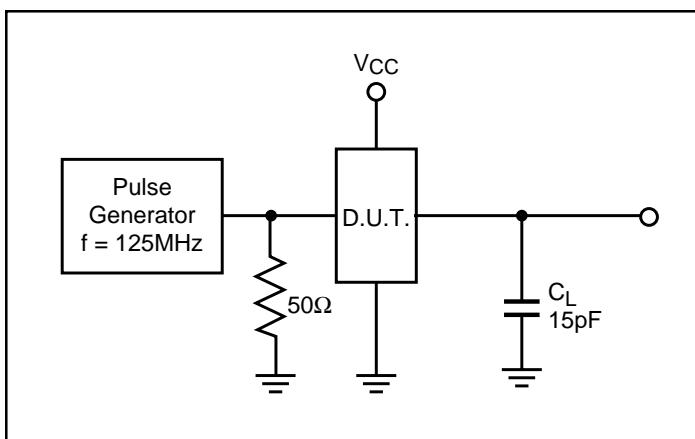
$$t_{SK(o)} = |t_{PLHy} - t_{PLHx}| \text{ or } |t_{PHLy} - t_{PHLx}|$$

Package Skew – $t_{SK(t)}$



$$t_{SK(t)} = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

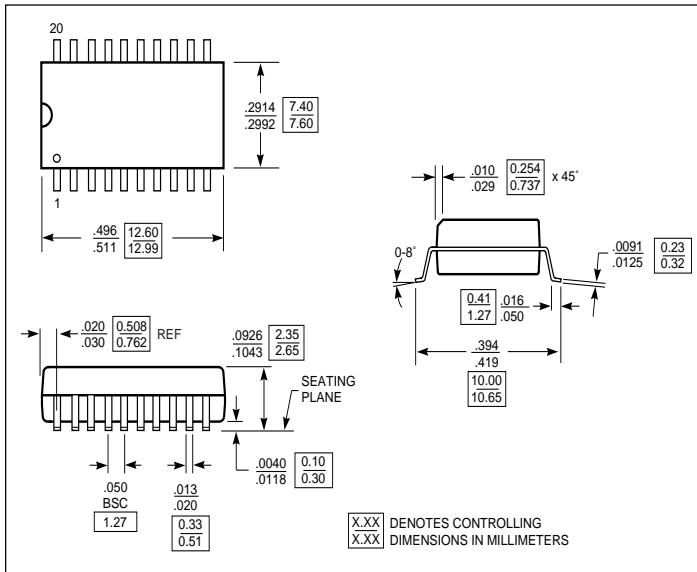
Test Circuits for All Outputs



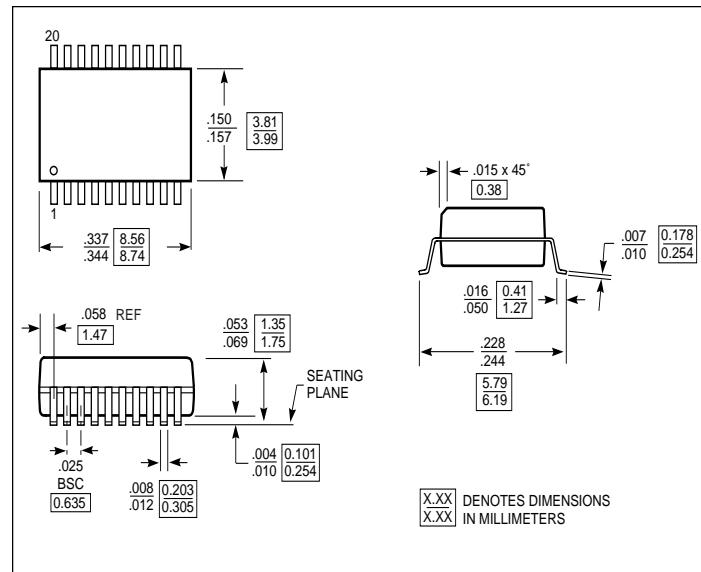
Ordering Information

Ordering Code	Package Type
PI49FCT32807S	300mil SOIC
PI49FCT32807Q	150mil QSOP
PI49FCT32807H	209mil SSOP

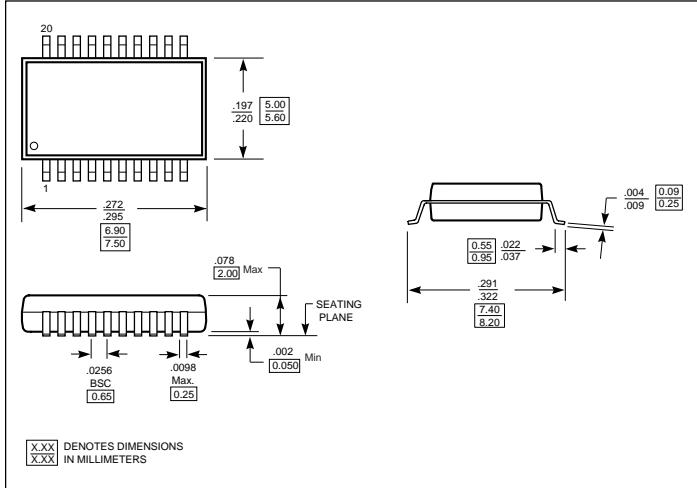
20-pin SOIC Package (S20)



20-pin QSOP Package (Q20)



20-pin SSOP Package (H20)



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