

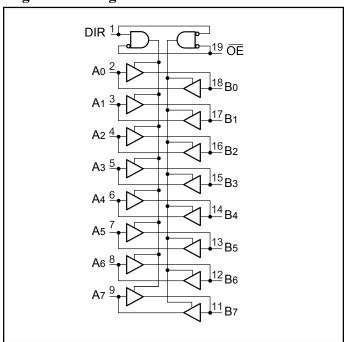


3.3V 8-Bit Bi-Directional Transceiver with 3-State Outputs

Product Features

- Advanced low power CMOS design for 2.7V to 3.6V V_{CC} operation
- Supports 5V input/output tolerance in mixed signal mode operation
- Function compatible with LVT family of products
- Balanced ±24mA output drive
- Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC}=3.3V, $T_A=25$ °C
- I_{off} and Power Up/Down 3-State support live insertion
- Latch-up performance exceeds 200mA Per JESD78
- ESD protection exceeds JESD 22
 - -2000V Human-Body Model (A114-B)
 - 200V Machine Model (A115-A)
- Packages (Pb-free available):
 - 20-pin 209-mil wide plastic SSOP (H)
 - -20-pin 173-mil wide plastic TSSOP(L)
 - 20-pin 300-mil wide plastic SOIC (S)

Logic Block Diagram



Product Description

Pericom Semiconductor's PI74LVTC series of logic circuits are produced using the Company's advanced CMOS technology, achieving industry leading speed.

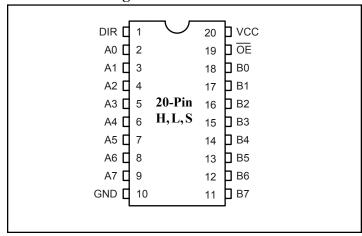
The PI74LVTC245 is a non-inverting 8-bit Bidirectional Transceiver designed for low-voltage 2.7V to 3.6V V_{CC} operation, with the capability of interfacing to the 5V system environment. This tranceiver is designed for asynchronous two-way communication between data buses. The direction control input pin (DIR) determines the direction of the dataflow from the A bus to the B bus or from the B bus to the A bus. The output enable (\overline{OE}) input, when HIGH, disables both A and B ports by placing them in HIGHZ condition.

When Vcc is between 0 to 1.5V during power up or power down, the outputs of the device are in the high-impedance state. To ensure the high-impedance state above 1.5V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

The device fully supports live-insertion with its I_{off} and power-up/ down 3-state. The Ioff circuitry disables the outputs when the power is off, preventing the backflow of damaging current through the device. Power-up/down 3-state places the outputs in the high-impedance state during power up or power down, preventing driver conflict.

Product Pin Configuration

1



07/01/03 PS8691



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Notes:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

- 1. Input negative-voltage and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. This value is limited to 6.5 maximum
- 3. The package thermal impedance is calculated in accordance with JESD 51.

Truth Table⁽⁴⁾

Inpu	Outputs	
OE	DIR	
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	X	Z

Notes:

- 4. H = High Signal Level
 - L = Low Signal Level
 - X = Don't Care or Irrelevant
 - Z = High Impedance

Product Pin Description

Pin Name	Description		
ŌE	3-State Output Enable Inputs (Active LOW)		
DIR	Direction Control Input		
xAx	Side A Inputs or 3-State Outputs		
xBx	Side B Inputs or 3-State Outputs		
GND	Ground		
Vcc	Power		

2

07/01/03



$\textbf{Recommended Operating Conditions}^{(5)}$

		Min.	Max.	Units	
V _{CC} Supply Voltage	Operating	2.7	3.6		
V _{IH} High-level Input Voltage	$V_{CC} = 2.7V \text{ to } 3.6V$	2.0			
V _{IL} Low-level Input Voltage	$V_{CC} = 2.7V \text{ to } 3.6V$		0.8]	
V _I Input Voltage		0	5.5	V	
V _O Output Voltage	High or Low State	0	V _{CC}		
	3-State	0	5.5		
	$V_{\rm CC} = 2.7 V$		- 12		
I _{OH} High-level output current	$V_{\rm CC} = 3.0 \text{V to } 3.6 \text{V}$		- 24	1 .	
	$V_{\rm CC} = 2.7 V$		12	- mA	
I _{OL} Low-level output current	$V_{CC} = 3.0 \text{V to } 3.6 \text{V}$		24		
$\Delta t/\Delta V$ Input transition rise or fall rate			6	ns/V	
$\Delta t/\Delta V_{CC}$ Power-up ramp rate		150		μs/V	
T _A Operating free-air temperature	'	- 40	85	°C	

Notes:

^{5.} All unused inputs must be held at V_{CC} or GND to ensure proper device operation.



DC Electrical Characteristics (Over the Operating Range, $T_A = -40$ °C to +85 °C)

Paramete- rs	Descr	iption		Test Conditions		Min.	Max.	Units	
V _{IK}	Clamp Diode	Voltage	$V_{CC} = 2.7V$	$I_I = -18\text{mA}$			-1.2V		
			$V_{CC} = 2.7 \text{V to } 3.6 \text{V}$	$I_{OH} = -100 \mu A$		V _{CC} -0.2V			
	Output High V	oltogo	$V_{CC} = 2.7V$	$I_{OH} = -12 \text{mA}$		2.2			
V _{OH}	Output High V	onage	$V_{CC} = 3V$	$I_{OH} = -12 \text{mA}$		2.4			
			νω-3 ν	I_{OH} = -24mA		2.2		V	
			$V_{CC} = 2.7 \text{V to } 3.6 \text{V}$	I_{OL} = 100 μ A			0.2		
V _{OL}	Output Low V	oltage	$V_{CC} = 2.7V$	I_{OL} = 12mA			0.4		
VOL	Output Low V	olage	$V_{CC} = 3V$	I_{OL} = 12mA			0.4		
			νω-3 ν	$I_{OL}=24mA$			0.55		
	Control Inputs		$V_{\rm CC} = 0$ V to 3.6V	$V_{\rm I} = 0 \text{V to } 5.5 \text{V}$			±5		
I_{I}	I _I Leakage Current	eakage		$V_I = 5.5V$					
				$V_{\rm I} = V_{\rm CC}$			±5		
				$V_{\rm I} = {\rm GND}$					
I _{OFF}	Power Off Ou Current	tput Leakage	$V_{CC} = 0V$	$V_{\rm I}$ or $V_{\rm O}$ = 0V to 5.5V			±5		
Iozpu	Power-Up 3-S	State Current	$V_{CC} = 0V$ to 1.5V	$V_O = 0.5V$ to 5.5V, $\overline{OE} = \text{don't care}$			±5	μA	
IOZPD	Power-Down Current	3-State	$V_{\rm CC}$ = 1.5V to 0V	$V_O = 0.5V$ to 5.5V, $\overline{OE} = \text{don't care}$			±5		
Loc	Quiescent Power Supply		Quiescent Power Supply	$V_{CC} = 2.7V \text{ to } 3.6V$	$V_I = V_{CC}$ or GND	$I_{O} = 0$		100	
Icc	Current		V(C - 2.7 V 10 3.0 V	$3.6V \le V_I \le 5.5V^{(7)}$	10-0				
ΔI_{CC}	Increase in Icc		$V_{CC} = 3.0 \text{V to } 3.6 \text{V}$	One input at V_{CC} - 0.6 $V^{(8)}$ Other inputs at V_{CC} or GN			500		

Notes:

- 6. For I/O ports, Input Leakage Current (I_I) includes the 3-state Output Leakage Current. Unused pins are at V_{CC} or GND.
- 7. This applies in the disabled state only.
- 8. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

4



Capacitance

Parameters	Description	Test Conditions	Тур. (9)	Units
C_{IN}	Control Input Capacitance	$V_{CC} = 3.3V$, $V_I = V_{CC}$ or GND	3.3	
C_{IO}	Input/Output Capacitance	$V_{CC} = 3.3V$, $V_O = V_{CC}$ or GND	7.8	pF
C_{PD}	Power Dissipation Capacitance (10)	$V_{CC} = 3.3V$, $V_{I} = 0$ or V_{CC} , $f=10$ MHz	33	

Notes:

- 9. All typical values are measured at $V_{CC} = 3.3V$, $T_A = 25$ °C.
- 10. C_{PD} is defined as the value of the internal equivalent capacitance withic is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle, C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN})+(I_{CC}\text{static})$.

Switching Characteristics Over Operating Range

				$V_{CC} = 3$.	3V ±0.3V	V _{CC} :	= 2.7V	
Parameters	Parameters Description		To (Output)	$C_L = 50 pF, R_L = 500 Ohm$		$C_L = 50 pF, R_L = 500 Ohm$		Units
				Min	Max.	Min.	Max.	
t _{PLH}	Propagation Dalay	A or B	B or A	1.0	5.4	1.0	5.8	
t _{PHL}	Propagation Delay	AUID	D OI A	1.0	5.4	1.0	5.8	
t _{PZH}	Output Enable Time	ŌĒ	Ē A or B	1.0	7.0	1.0	7.9	
t _{PZL}	Output Enable Time			1.0	7.0	1.0	7.9	ns
t _{PHZ}	0 ((P. 11 T. OF		A D	1.0	5.4	1.0	5.8	
t _{PLZ}	Output Disable Time	ŌĒ	A or B	1.0	5.4	1.0	5.8	
t _{SK(O)}	Output to Output Skew ⁽¹¹⁾				0.5			

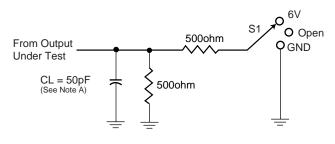
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Notes:

11. Skew between any two outputs, switching in the same direction.

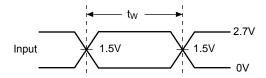


PARAMETER MEASUREMENT INFORMATION V_{CC} = 2.7V and 3.3V ±0.3V

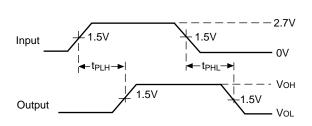


Test	S1
tplh/tphl	Open
tplz/tpzl	6V
tphz/tpzh	GND

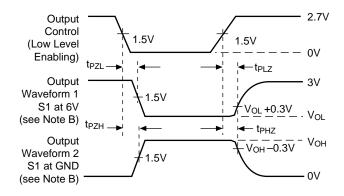
Load Circuit



Voltage Waveforms Pulse Duration



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input impulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50$ ohm, $t_R \leq 2.5$ ns, $t_F \leq 2.5$ ns.

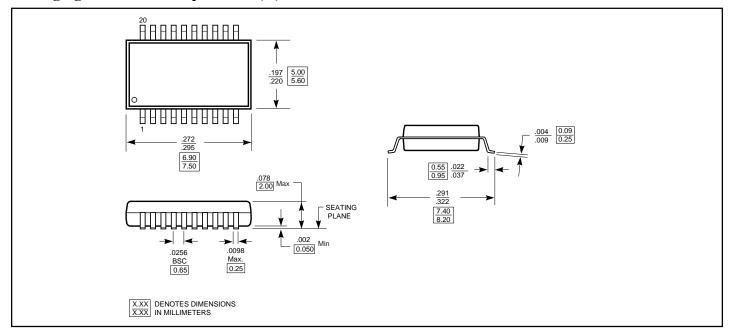
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D. The outputs are measured one at a time with one transition per measurement.

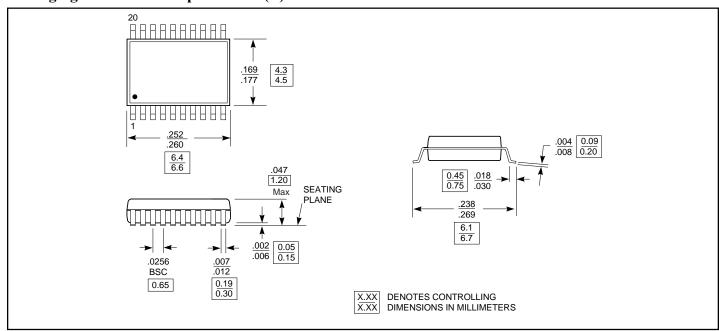
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Packaging Mechanical: 20-pin SSOP (H)

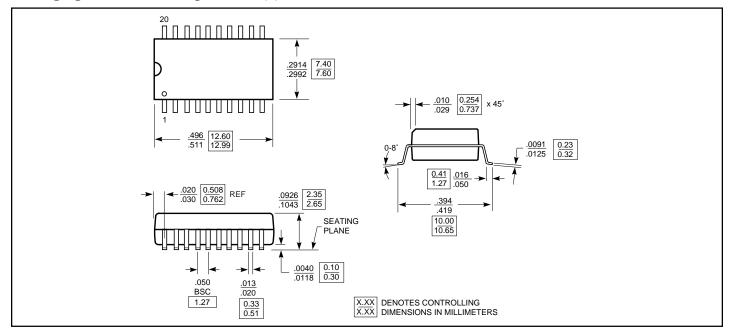


Packaging Mechanical: 20-pin TSSOP(L)





Packaging Mechanical: 20-pin SOIC (S)



Ordering Information

Ordering Data	Description
PI74LVTC245H	20-pin, 209-mil wide plastic SSOP
PI74LVTC245L	20-pin, 173-mil wide plastic TSSOP
PI74LVTC245S	20-pin, 300-mil wide plastic SOIC

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/mechanicals.php

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8 PS8691 07/01/03