PI6C3Q991A, PI6C3Q993A

3.3V Programmable Skew PLL Clock Driver

SuperClock®

Features

- PI6C3Q99X family provides following products:
  PI6C3Q991A: 32-pin PLCC version
  PI6C3Q993A: 28-pin QSOP version
- Inputs are 5V Tolerant
- 4 pairs of programmable skew outputs
- Low skew: 200ps same pair; 250ps all outputs
- Selectable positive or negative edge synchronization:
  Excellent for DSP applications
- Synchronous output enable
- Input frequency: 3.75 MHz to 110 MHz
- Output frequency: 15 MHz to 110 MHz
- 2x, 4x, 1/2, and 1/4 outputs
- 3 skew grades:
  PI6C3Q99x: t_{SKEW0}<750ps
  PI6C3Q99x-5: t_{SKEW0}<500ps
  PI6C3Q99x-2: t_{SKEW0}<250ps
- 3-level inputs for skew and PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 12mA balanced drive outputs
- Low Jitter: < 200ps peak-to-peak
- Industrial temperature range
- Pin-to-pin compatible with IDT QS5V991A and QS5V993A
- Available in 32-pin PLCC and 28-pin QSOP

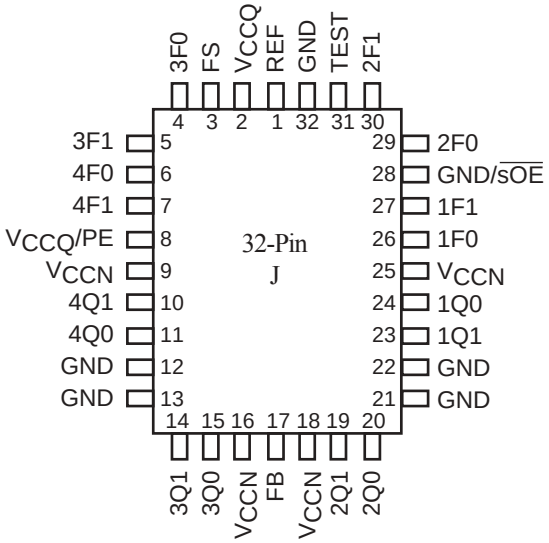
Description

The PI6C3Q99X family, a high-fanout 3.3V PLL-based clock driver, is intended for high-performance computing and data-communication applications. A key feature of the programmable skew is the ability of outputs to lead or lag the REF input signal. The PI6C3Q991A has 8 programmable skew outputs in 4 banks of 2, while the PI6C3Q993A has 6 programmable skew outputs and 2 zero skew outputs. Skew is controlled by 3-level input signals that may be hard-wired to appropriate HIGH-MID-LOW levels.

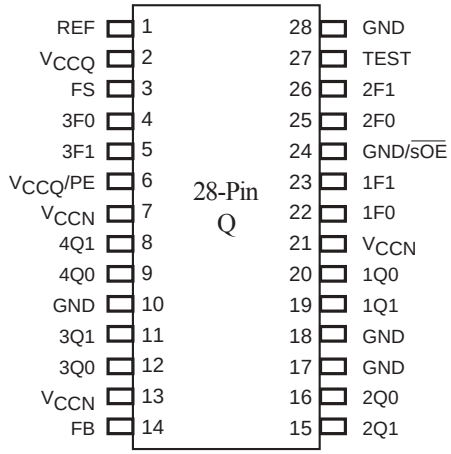
When the GND/$\overline{sOE}$ pin is held LOW, all the outputs are synchronously enabled. However, if GND/$\overline{sOE}$ is held HIGH, all outputs except 3Q0 and 3Q1 are synchronously disabled. Furthermore, when the V_{CCQ}/PE is held HIGH, all outputs are synchronized with the positive edge of the REF clock input. When V_{CCQ} /PE is held LOW, all outputs are synchronized with the negative edge of REF. Both devices have LVTTL outputs with 12mA balanced drive outputs.

Pin Configurations

PI6C3Q991A



PI6C3Q993A



Logic Block Diagrams

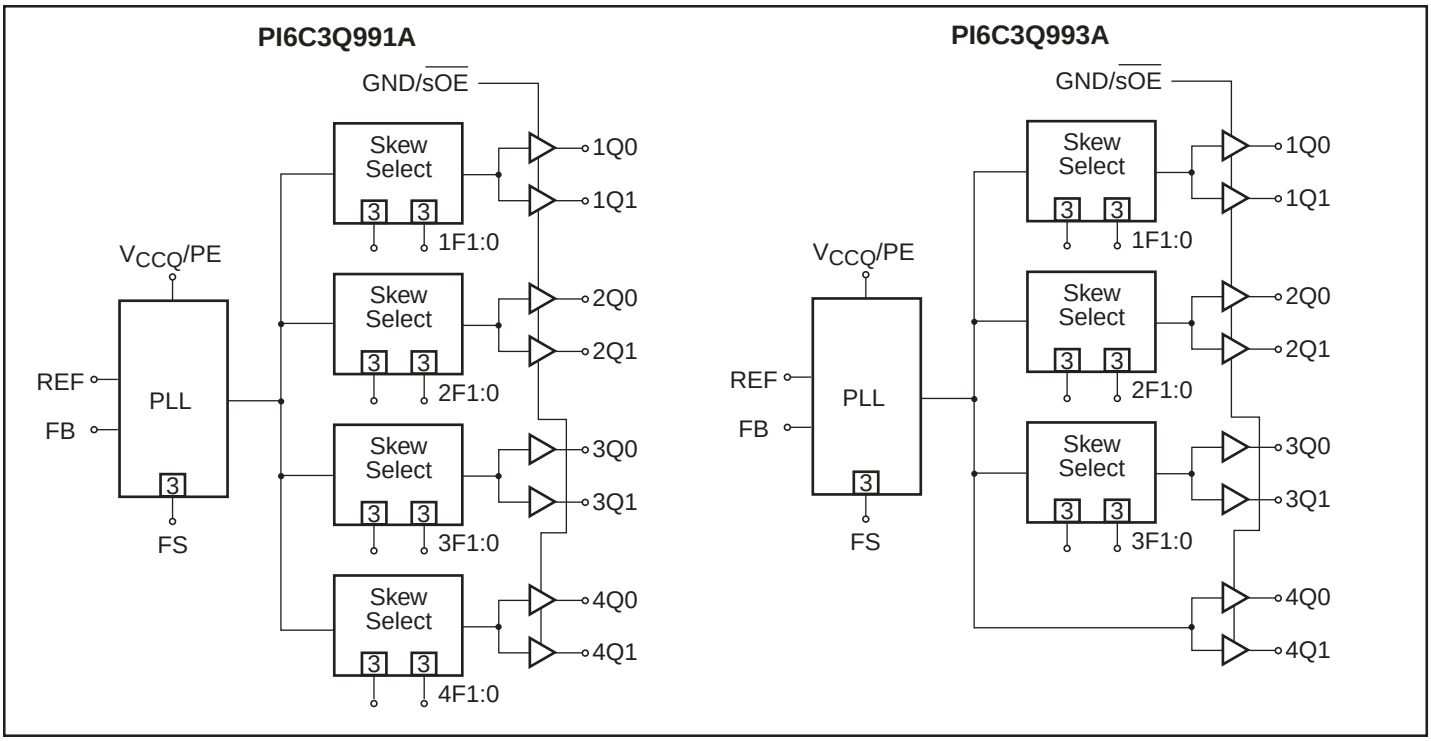


Table 1. Pin Descriptions

Pin Name	Type	Functional Description
REF	IN	Reference Clock input
FB	IN	Feedback Input
TEST(1)	IN	When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Skew selections (see table 3) remain in effect. Set LOW for normal operation.
GND/$\overline{sOE}$(1)	IN	Synchronous Output Enable. When HIGH, it stops clock outputs (except 3Q0 and 3Q1) in a LOW state - 3Q0 or 3Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and GND/$\overline{sOE}$ is HIGH, the nF [1:0] pins act as output disable controls for individual banks when nF [1:0] = LL. Set GND/$\overline{sOE}$ LOW for normal operation.
V_{CCQ}/ PE	IN	Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock.
nF [1:0]	IN	3-level inputs for selecting 1of 9 skew taps or frequency range.
FS	IN	Selects appropriate oscillator circuit based on anticipated frequency range. See table 2
nQ [1:0]	OUT	4 output banks of 2 outputs, with programmable skew. On the PI6C3Q993A 4Q1:0 are fixed zero skew outputs.
V_{CCN}	PWR	Power supply for output buffers
V_{CCQ}	PWR	Power supply for phase locked loop and other internal circuitry
GND	PWR	Ground

Note:
1. When TEST = MID and GND/$\overline{sOE}$ = HIGH, PLL remains active with nF[1:0] =LL functioning as an output disable control for individual output banks. Skew selections (see Table 3) remain in effect unless nF[1:0] = LL.

Programmable Skew

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit t_U which is of the order of a nanosecond (see Table 2). There are 9 skew configurations available for each output pair. These configurations are choosen by the nF1:0 control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Skew Selection Table (Table 3) shows how to select specific skew taps by using the nF1:0 control pins.

External Feedback

By providing external feedback, the PI6C3Q99x family gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the V_{CO}. Phase differences cause the V_{CO} of the PLL to adjust upwards or downwards accordingly. An internal loop filter moderates the response of the V_{CO} to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

Table 2. PLL Programmable Skew Range and Resolution Table

	FS = LOW	FS = MID	FS = HIGH	Comments
Timing unit calculation (t_U)	$1/(44xF_{NOM})$	$1/(26xF_{NOM})$	$1/(16xF_{NOM})$	
V_{CO} frequency range (F_{NOM})(2,3)	15 to 35 MHz	25 to 60 MHz	40 to 110 MHz	
Skew adjustment range(4) Max. adjustment	±9.09ns ±49° ±14%	±9.23ns ±83° ±23%	±9.38ns ±135° ±37%	ns Phase degrees % of cycle time
Example 1, F_{NOM} = 15 MHz	t_U = 1.52ns			
Example 2, F_{NOM} = 25 MHz	t_U = 0.91ns	t_U = 1.54ns		
Example 3, F_{NOM} = 30 MHz	t_U = 0.76ns	t_U = 1.28ns		
Example 4, F_{NOM} = 40 MHz		t_U = 0.96ns	t_U = 1.56ns	
Example 5, F_{NOM} = 50 MHz		t_U = 0.77ns	t_U = 1.25ns	
Example 6, F_{NOM} = 80 MHz			t_U = 0.78ns	

Notes:

2. The device may be operated outside recommended frequency ranges without damage, but functional operation is not guaranteed. Selecting the appropriate FS value based on input frequency range allows the PLL to operate in its 'sweet spot' where jitter is lowest.
3. The level to be set on FS is determined by the nominal operating frequency of the V_{CO} and Time Unit Generator. The V_{CO} frequency always appears at 1Q1:0, 2Q1:0, and the higher outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be the same as the V_{CO} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be 1/2 or 1/4 the V_{CO} frequency when the part is configured for a frequency multiplication by using a divided output as the FB input.
4. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a $4t_U$ skewed output is used for feedback, all other outputs will be skewed $-4t_U$ in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to output pairs 3 and 4 where $\pm 6t_U$ skew adjustment is possible and at the lowest F_{NOM} value.

Table 3. Skew Selection Table for Output Pairs

nF1:0	Skew (Pair #1, #2)	Skew (Pair #3)	Skew (Pair #4)(5)
LL(6)	$-4t_U$	Divide by 2	Divide by 2*
LM	$-3t_U$	$-6t_U$	$-6t_U$
LH	$-2t_U$	$-4t_U$	$-4t_U$
ML	$-1t_U$	$-2t_U$	$-2t_U$
MM	Zero skew	Zero skew	Zero skew
MH	$+1t_U$	$+2t_U$	$+2t_U$
HL	$+2t_U$	$+4t_U$	$+4t_U$
HM	$+3t_U$	$+6t_U$	$+6t_U$
HH	$+4t_U$	Divide by 4*	Inverted(7)

Notes:
5. Programmable skew on pair #4 is not applicable for the PI6C3Q993A.
6. LL disables outputs if TEST = MID and GND/s$\overline{OE}$ = HIGH.
7. When pair #4 is set to HH (inverted), GND/s$\overline{OE}$ disables pair #4 HIGH when V_{CCQ}/PE = HIGH, GND/s$\overline{OE}$ disables pair #4 LOW when V_{CCQ}/PE = LOW.

* The rising edge of 3Qx and 4Qx are not aligned only when both 3F1 : 0 = HH (divide by 4) and 4F1 : 0 = LL (divide by 2) are selected. This is not applicable for PI6C3Q993A.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
Input Voltage	–0.5V to 7.0V
Maximum Power Dissipation at T_A = 85°C, PLCC	0.80 watts
QSOP	0.66 watts
TSTG Storage Temperature	–65°C to 150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings arestress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5. Recommended Operating Range

Symbol	Description	PI6C3Q991A/PI6C3Q993A PI6C3Q99A-5/PI6C3Q993A-5 (Industrial)		PI6C3Q991A/PI6C3Q993A PI6C3Q991A-2/PI6C3Q993A-2 PI6C3Q991A-5/PI6C3Q993A-5 (Commercial)		Units
		Min.	Max.	Min.	Max.	
V_{CC}	Power Supply Voltage	3.0	3.6	3.0	3.6	V
T_A	Ambient Operating Temperature	–40	85	0	70	°C

Table 6. DC Characteristics Over Operating Range

Symbol	Parameter	Test Condition	Min.	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB inputs only)	2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, FB inputs only)	–0.5	0.8	
V_{IHH}	Input HIGH Voltage(8)	3-Level Inputs Only	V_{CC} –0.6		
V_{IMM}	Input MID Voltage(8)	3-Level Inputs Only	$V_{CC}/2$ –0.3	$V_{CC}/2$ +0.3	
V_{ILL}	Input LOW Voltage(8)	3-Level Inputs Only		0.6	
$\lvert I_{IN} \rvert$	Input Leakage Current (REF, FB inputs only)	$V_{IN} = V_{CC}$ or GND, V_{CC} = Max.		5	µA
$\lvert I_3 \rvert$	3-Level Input DC Current (TEST, FS, nF1:0)	$V_{IN} = V_{CC}$ HIGH Level $V_{IN} = V_{CC}/2$ MID Level V_{IN} = GND LOW Level		200 50 200	
$\lvert I_{PU} \rvert$	Input Pull-Up Current (V_{CCQ}/PE)	V_{CC} = Max., V_{IN} = GND		100	
$\lvert I_{PD} \rvert$	Input Pull-Down Current (GND/$\overline{sOE}$)	V_{CC} = Max., $V_{IN} = V_{CC}$		100	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –12mA	2.2		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12mA		0.55	

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Condition	Typ.	Max.	Units
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., TEST = Mid., REF = LOW, GND/$\overline{sOE}$ = LOW, All outputs unloaded	8.0	15	mA
ΔI_{CCN}	Power Supply Current per Input HIGH(9)	V_{CC} = Max., V_{IN} = 3.0V	1.0		µA
I_{CCD}	Dynamic Power Supply Current per Output(9)	V_{CC} = Max., C_L = 0pF	55	125	µA/ MHz
I_C	Total Power Supply Current(9)	V_{CC} = 3.3V, F_{REF} = 20 MHz, C_L = 160pF(10)	29		mA
I_C	Total Power Supply Current(9)	V_{CC} = 3.3V, F_{REF} = 33 MHz, C_L = 160pF(10)	42		
I_C	Total Power Supply Current(9)	V_{CC} = 3.3V, F_{REF} = 66 MHz, C_L = 160pF(10)	76		

Notes:

8. These inputs are normally wired to V_{CC} , GND, or unconnected. Internal termination resistors bias unconnected inputs to $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
9. Guaranteed by characterization but not production tested.
10. For 8 outputs each loaded with 20pF.

Table 8. Capacitance (T_A = 25°C, f = 1 MHz, V_{IN} = 0V)

	QSOP		PLCC		Units
	Typ.	Max.	Typ.	Max.	
C_{IN}	4	6	5	7	pF

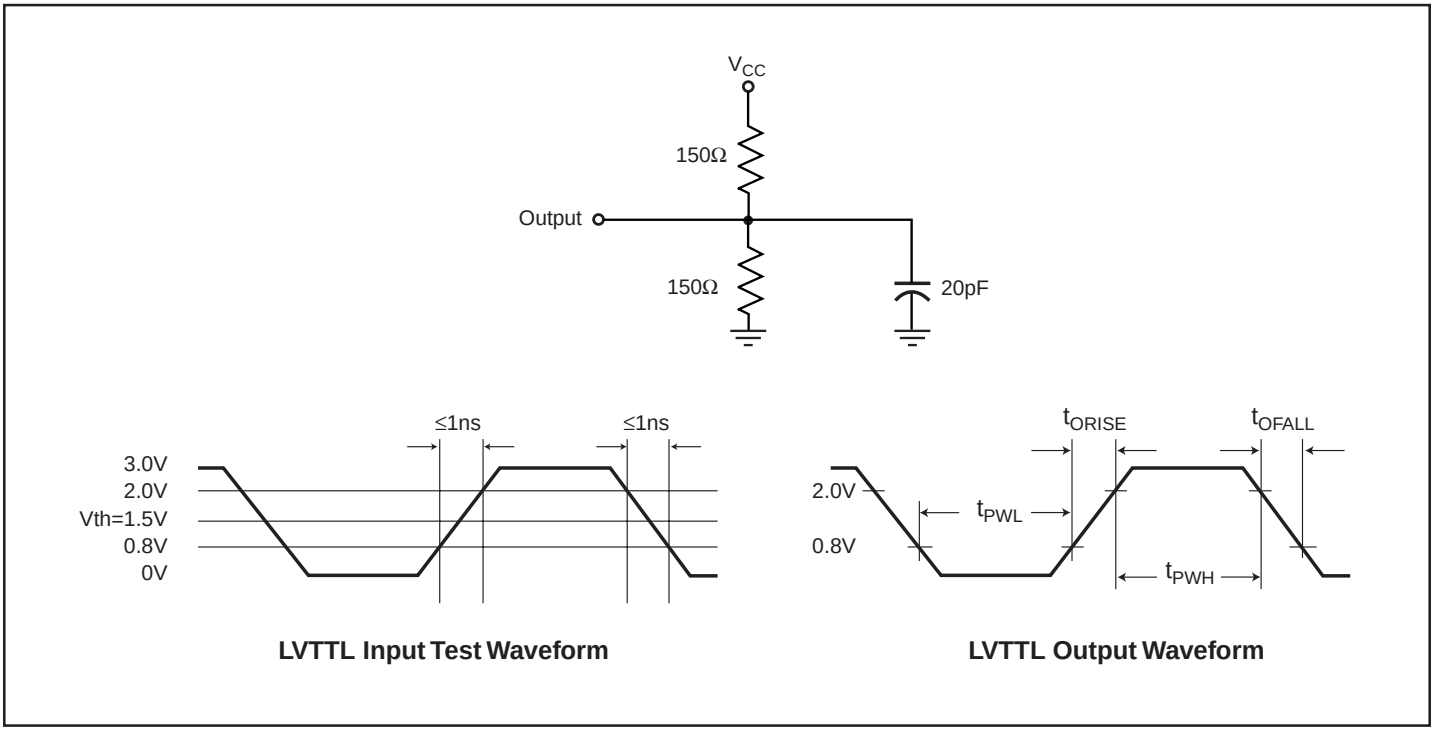


Figure 1. AC Test Loads and Waveforms

Table 9. Switching Characteristics Over Operating Range

Symbol	Description		PI6C3Q991A-2 PI6C3Q993A-2			PI6C3Q991A-5 PI6C3Q993A-5			PI6C3Q991A PI6C3Q993A			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
F_{NOM}	V_{CO} frequency range		see Table 2			see Table 2			see Table 2			
t_{RPWH}	REF pulse width HIGH(21)		3.0			3.0			3.0			ns
t_{RPWL}	REF pulse width LOW(21)		3.0			3.0			3.0			
t_U	Programmable skew time unit		see Table 3			see Table 3			see Table 3			
t_{SKEWPR}	Zero output matched-pair skew (xQ0, xQ1)(11,12,13)			0.05	0.20		0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero output skew (all outputs) C_L = 0pF(11,14)			0.1	0.25		0.25	0.5		0.3	0.75	
t_{SKEW1}	Output skew (rise-rise, fall-fall, same class outputs)(11,15)			0.25	0.50		0.6	0.7		0.6	1.0	
t_{SKEW2}	Output skew (rise-fall, nominal-inverted, divided-divided(11,15)			0.30	1.2		0.5	1.2		1.0	1.5	
t_{SKEW3}	Output skew (rise-rise, fall-fall, different class outputs)(11,15)			0.25	0.50		0.5	0.7		0.7	1.2	
t_{SKEW4}	Output skew (rise-fall, nominal-divided, divided inverted(11,15)			0.50	0.90		0.5	1.0		1.2	1.7	
t_{DEV}	Device-to-device skew(11,12,16)				0.75			1.25			1.65	
t_{PD}	REF input to FB propagation delay(11,18)		–0.25	0	0.25	–0.5	0	0.5	–0.7	0	0.7	
t_{ODCV}	Output duty cycle varation from 50%(11)		–1.2	0	1.2	–1.2	0	1.2	–1.2	0	1.2	
t_{PWH}	Output HIGH time deviation from 50%(11,19)				2.0			2.5			3.0	
t_{PWL}	Output LOW time deviation from 50%(11,20)				1.5			3.0			3.5	
t_{ORISE}	Output rise time(11)		0.15	1.0	1.5	0.15	1.0	1.5	0.15	1.5	2.5	
t_{OFALL}	Output fall time(11)		0.15	1.0	1.5	0.15	1.0	1.5	0.15	1.5	2.5	
t_{LOCK}	PLL lock time(11,17)				0.5			0.5			0.5	ms
t_{JR}	Cycle-to-cycle output jitter(II)	RMS			25			40			40	ps
		Peak-to-peak			200			200			200	

Notes:

11. All timing tolerances apply for $F_{NOM} \geq 25$MHz. Guaranteed by design and characterization, not subject to 100% production testing.
12. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
13. t_{SKEWPR} is the skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.
14. t_{SKEW0} is the skew between outputs when they are selected for $0t_U$.
15. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
16. t_{DEV} is output-to-output skew between any two devices operating under the same conditions (V_{CC} , ambient temperature, air flow, etc.)
17. t_{LOCK} is time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable & within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
18. t_{PD} is measured with REF input rise and fall times (from 0.8V to 2.0V) of 1.0ns.
19. Measured at 2.0V.
20. Measured at 0.8V.
21. Refer to Table10 for more detail.

Table 10. Input Timing Requirements(22)

Symbol	Description	Min.	Max.	Units
t_R, t_F	Maximum input rise and fall times, 0.8V to 2.0V		10	ns/V
t_{PWC}	Input clock pulse, HIGH or LOW	3		ns
D_H	Input duty cycle	10	90	%

Notes:

22. Input timing requirements are guaranteed by design but not tested. Where pulse width implied by D_H is less than t_{PWC} limit, t_{PWC} limit applies.

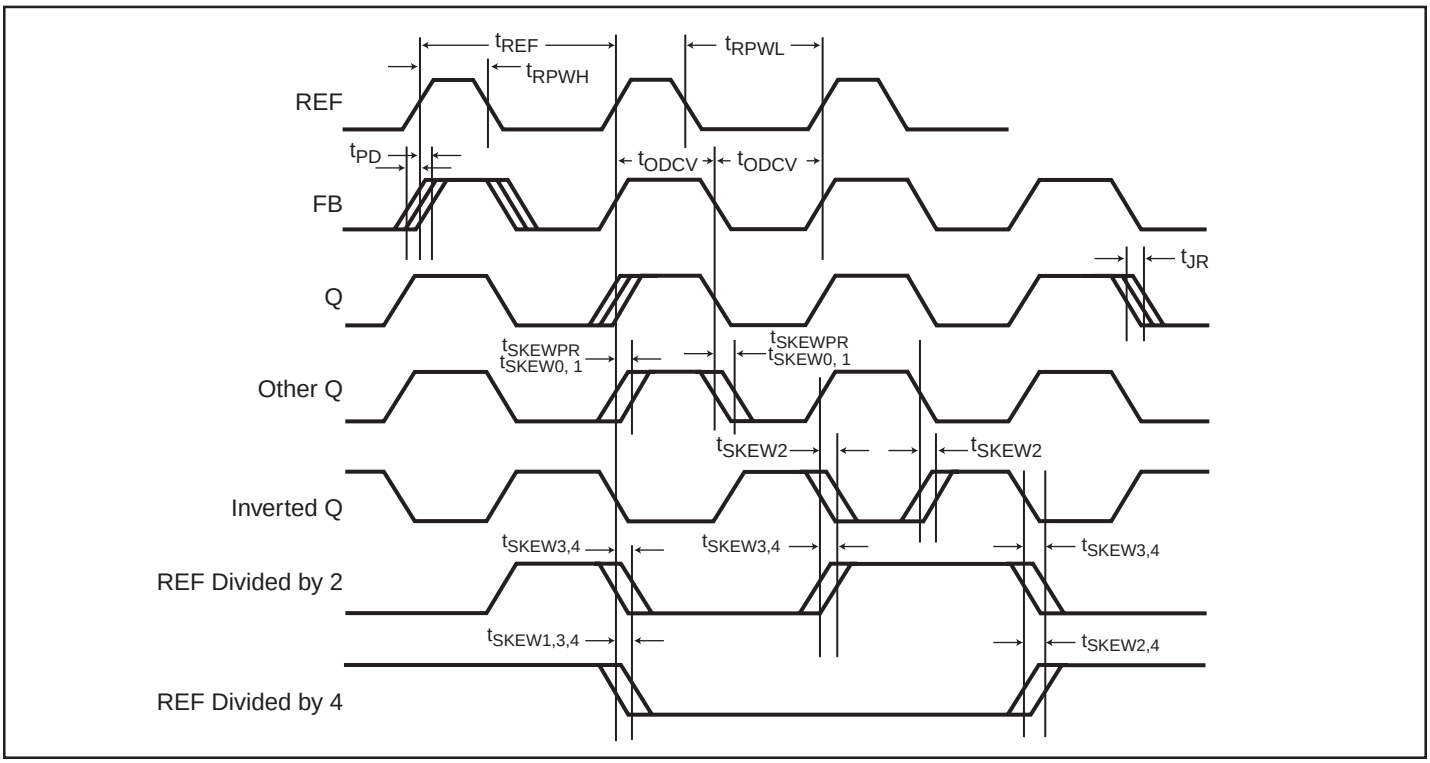


Figure 2. AC Timing Diagram

Notes:

V_{CCQ}/PE: The AC timing diagram above applies to V_{CCQ}/PE=V_{CC}. For V_{CCQ}/PE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 20pF and terminated with 75ohms to V_{CC}/2.

t_{SKEWPR}: The skew between a pair of outputs (xQ0 and xQ1) when all eight outputs are selected for $0t_U$.

t_{SKEW0}: The skew between outputs when they are selected for 0t U.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.

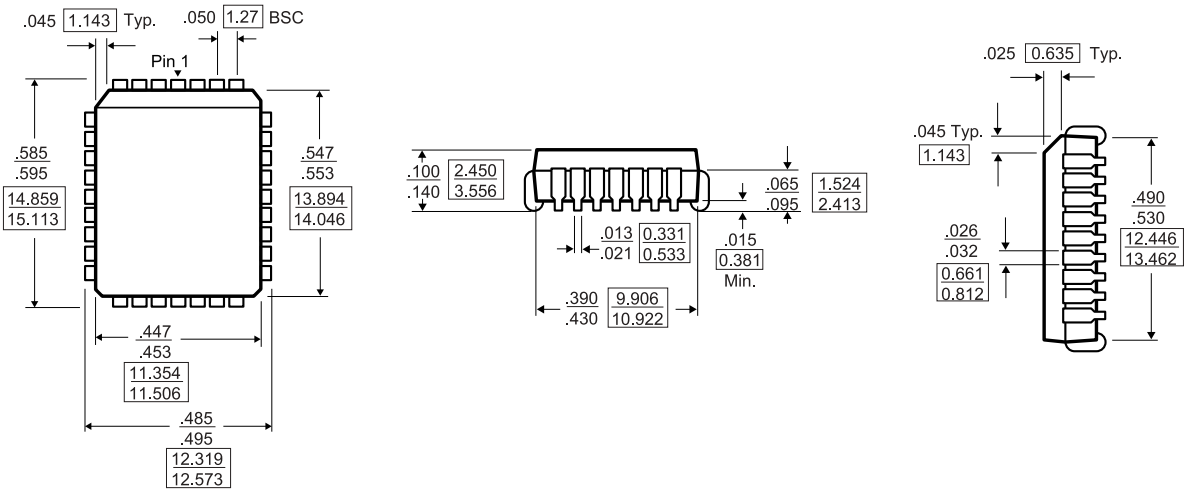
t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

t_{PWH} is measured at 2.0V.

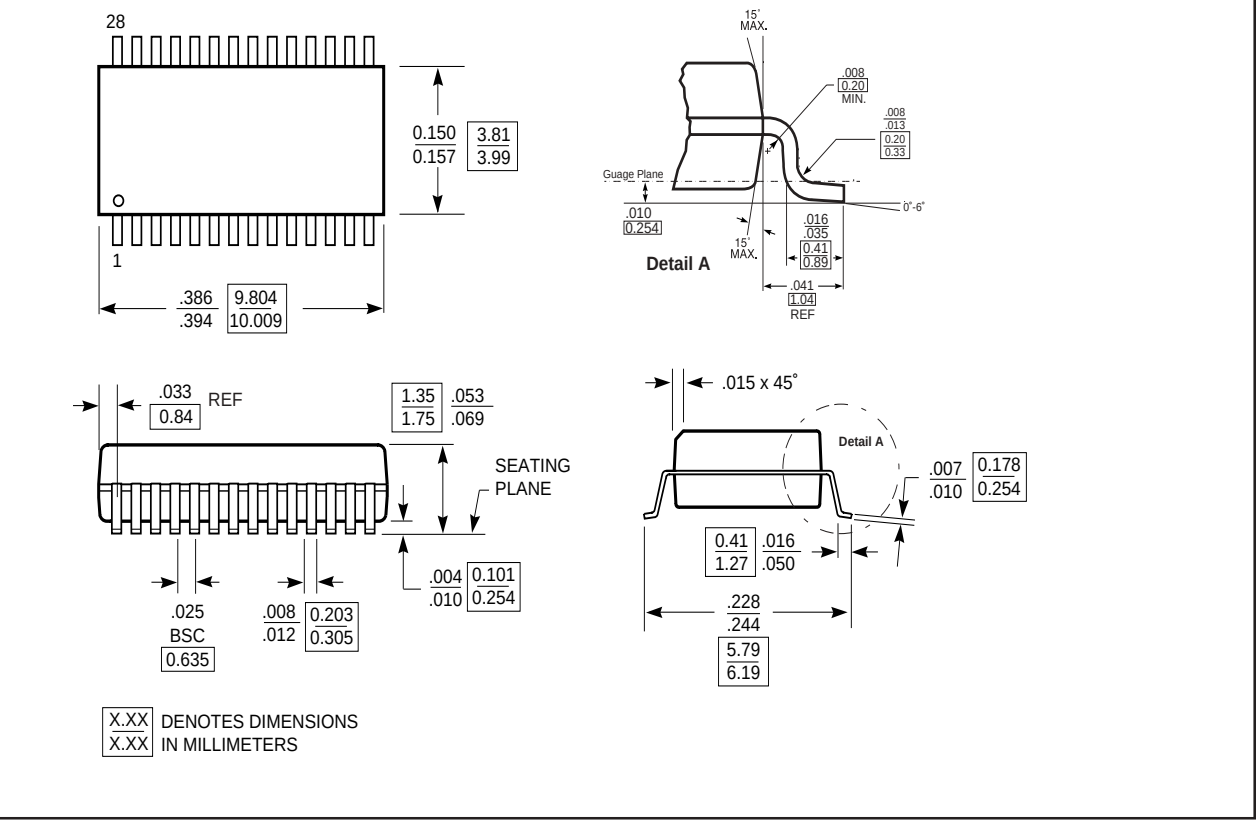
t_{PWL} is measured at 0.8V.

t_{ORISE} & t_{OFALL} are measured between 0.8V and 2.0V.

32-Pin PLCC Package Diagram



28-Pin QSOP Package Diagram



Ordering Information

Ordering Code	Package Code	Package Type	Operating Range
PI6C3Q991AJ	J32	32-Pin PLCC	Commercial
PI6C3Q991A-2J	J32	32-Pin PLCC	
PI6C3Q991A-5J	J32	32-Pin PLCC	
PI6C3Q991A-IJ	J32	32-Pin PLCC	Industrial
PI6C3Q991A-5IJ	J32	32-Pin PLCC	
PI6C3Q993AQ	Q28	28-Pin QSOP	Commercial
PI6C3Q993A-2Q	Q28	28-Pin QSOP	
PI6C3Q993A-5Q	Q28	28-Pin QSOP	
PI6C3Q993A-IQ	Q28	28-Pin QSOP	Industrial
PI6C3Q993A-5IQ	Q28	28-Pin QSOP	