2.5V, 10-Bit, 2-Port 266 MHz DDR Bus Switch

Product Features

- Used in x8 DDR Memory Module
- Near zero propagation delay
- 20-ohm switches connect inputs to outputs
- Fast Switching Speed –3ns (max.)
- Low Off Capacitance (3pF)
- Pull-down on B output
- Packages available:
  – 24-pin 150 mil wide plastic QSOP (Q)
  – 24-pin 173 mil wide plastic TSSOP (L)

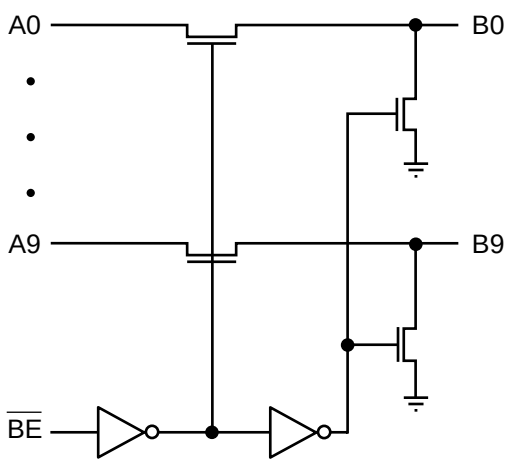
Product Description

Pericom Semiconductor's PI2BV series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry leading performance.

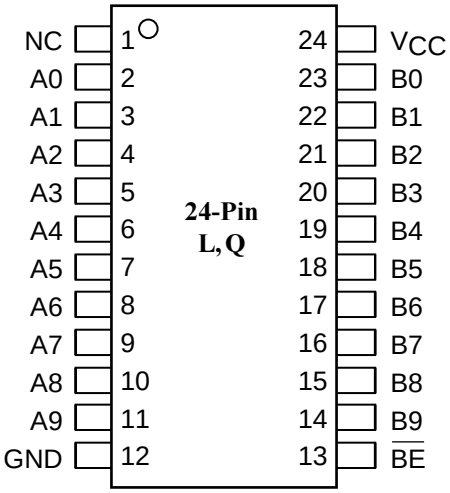
The PI2BV3867 is a 10-bit, 2.5 volt two-port bus switch designed with a low ON resistance allowing inputs to be connected directly to outputs. The bus switch creates no additional propagational delay or additional ground bounce noise. The switches are turned ON by the Bus Enable ($\overline{BE}$) input signal.

The PI2BV3867 switch is intended for 266 MHz DDR (x8) Memory Module Applications.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin Name	Description
$\overline{BE}$	Bus Enable Input (Active LOW)
A0–9	Bus A
B0–9	Bus B
GND	Ground
V_{CC}	Power

Truth Table[1]

Function	$\overline{BE}$	A0–A9
Disconnect	H	Hi-Z
Connect	L	B0–9

Notes:
H = High Voltage Level
L = Low Voltage Level
Hi-Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
DC Input Voltage	–0.5V to +4.6V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = 0°C to +85°C, V_{CC} = 2.3V to 2.7V)

Parameters	Description	Test Conditions(1)	Min.	Typ(2)	Max.	Units
V_{IH}	Input HIGH Voltage ($\overline{BE}$)	Guaranteed Logic HIGH Level	1.6		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage ($\overline{BE}$)	Guaranteed Logic LOW Level	–0.3		0.9	
I_I	Input Current	V_{CC} = Max., V_{IN} = V_{CC} or GND			±10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA			–1.2	V
R_{ON}	Switch ON Resistance(4)	V_{CC} = Min., V_{IN} = 0.9V, I_{ON} = 20mA		17	33	Ω
		V_{CC} = Min., V_{IN} = 1.6V, I_{ON} = 15mA		22	30	
R_{PD}	Pull-Down Resistance(5)	$V_{BIAS(B\text{-}Ports)}$ = 2.5V, I_{OZH} ≤ 250µA	10			kΩ

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters(4)	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	3	pF
C_{OFF}(A)	A Capacitance, Switch OFF		3	
C_{ON}(A/B)	A/B Capacitance, Switch ON		7	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 2.5V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
4. This parameter is determined by device characterization but is not production tested.
5. Pull-down resistance is measured with the switch OFF and calculated by $V_{BIAS(B\text{-}Ports)}/I_{OZH}$.

Power Supply Characteristics

Parameters	Description	Test Conditions(1)	Min.	Typ(2)	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = V_{CC} or GND		–	10	µA

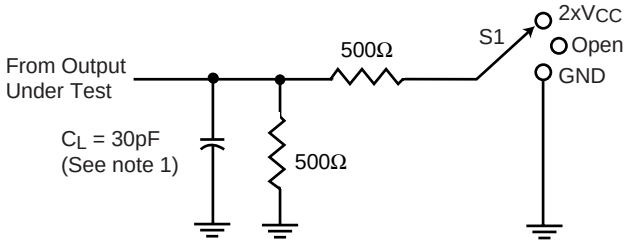
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 2.5V, +25°C ambient.
3. Per LVTTL driven input (control input only); A and B pins do not contribute to I_{CC}.

Switching Characteristics over Operating Range

Parameters	Description	Conditions[2,3]	PI2BV3867 Com. Min.	PI2BV3867 Com. Max.	Units
t_{PLH} t_{PHL}	Propagation Delay[2,3] Ax to Bx, Bx to Ax	C_L = 30pF, R_L = 500 ohms		1	ns
t_{PZH} t_{PZL}	Bus Enable Time BE to Ax or Bx		1	3	
			1	3.5	
t_{PHZ} t_{PLZ}	Bus Disable Time BE to Ax or Bx		1	3	
			1	3.8	

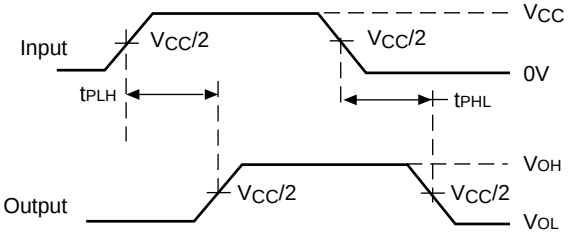
Notes:
1. See test circuit and waveforms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and load capacitance. The time constant for the switch alone is of the order of 1ns for 50pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the switch's driving side and its interaction with the load on the driven side.

Parameter Measurements

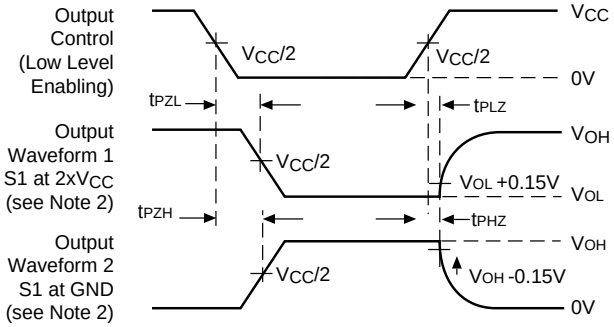


LOAD CIRCUIT

Test	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	$2xV_{CC}$
t_{PHZ}/t_{PZH}	GND



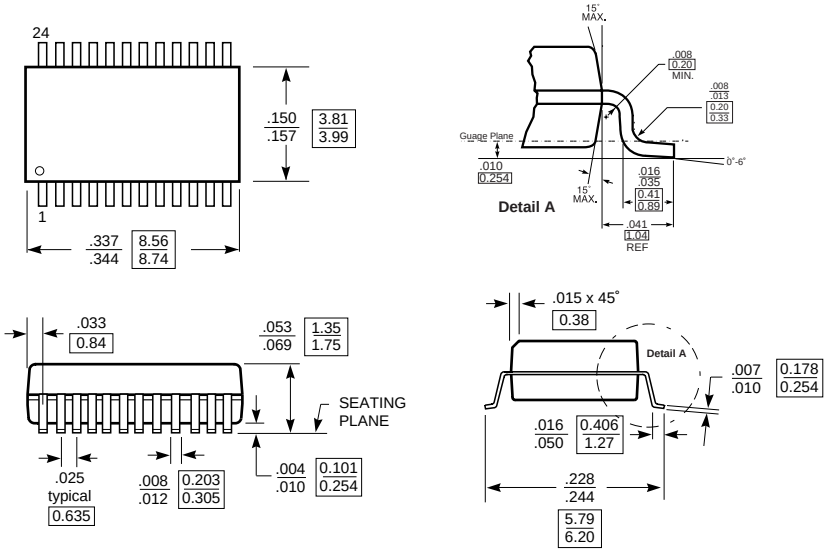
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



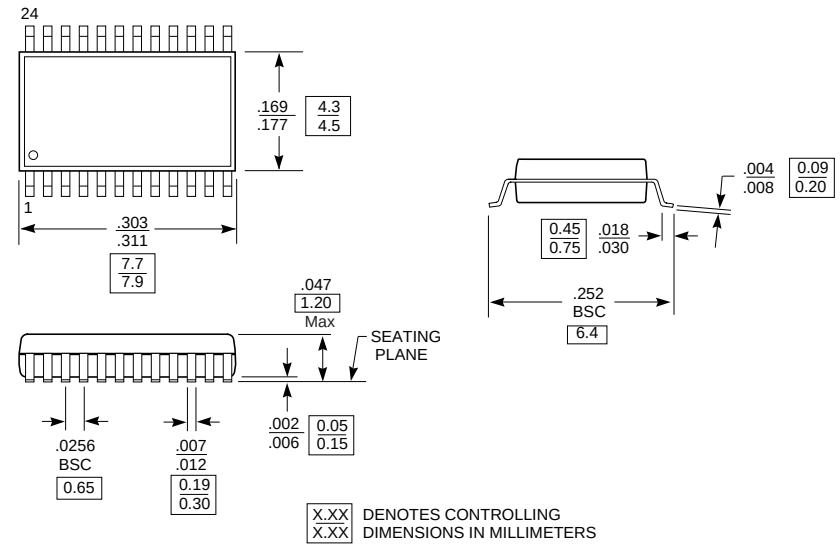
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

Notes:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR<10MHz, Z_O = 50 ohms, $t_R \le 2$ns, $t_F \le 2$ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{DIS}.
6. t_{PZL} and t_{PZH} are the same as t_{EN}.
7. t_{PLH} and t_{PHL} are the same as t_{PD}.

24-pin QSOP (Q) Package



24-pin TSSOP (L) Package



Ordering Information

Part	Pin-Package	Temperature
PI2BV3867Q	24 - QSOP(Q)	0°C to +85°C
PI2BV3867L	24 - TSSOP(L)	

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