



PI6CV857L

PLL Clock Driver for 2.5V DDR-SDRAM Memory

Product Features

- PLL clock distribution optimized for Double Data Rate SDRAM applications.
- Distributes one differential clock input pair to ten differential clock output pairs.
- Inputs (CLK, $\overline{\text{CLK}}$) and (FBIN, $\overline{\text{FBIN}}$): SSTL_2
- Input PWRDWN: LVCMOS
- Outputs (Yx, $\overline{\text{Yx}}$), (FBOU, $\overline{\text{FBOU}}$): SSTL_2
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the clock input.
- Operates at $\text{AV}_{\text{DD}} = 2.5\text{V}$ for core circuit and internal PLL, and $\text{V}_{\text{DDQ}} = 2.5\text{V}$ for differential output drivers
- Available Packages: Plastic 48-pin TSSOP, TVSOP

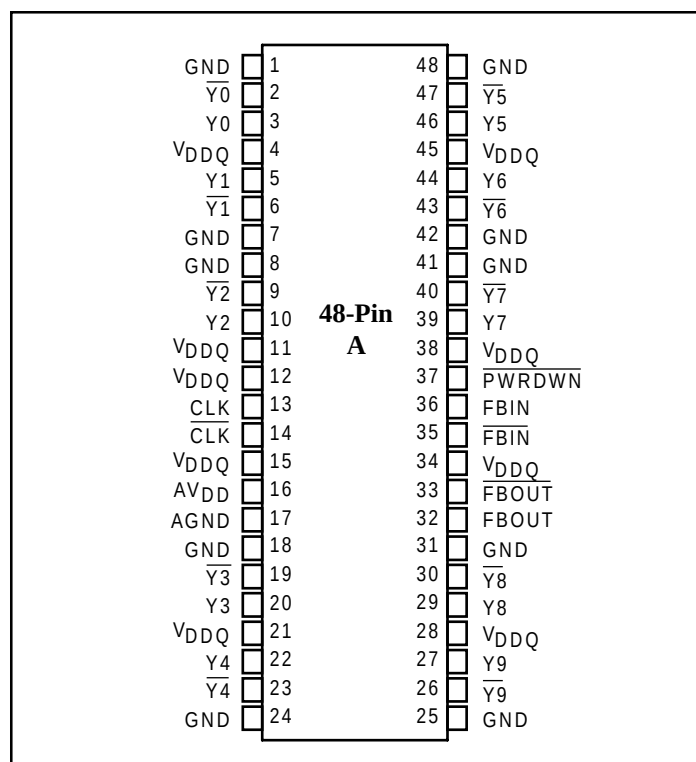
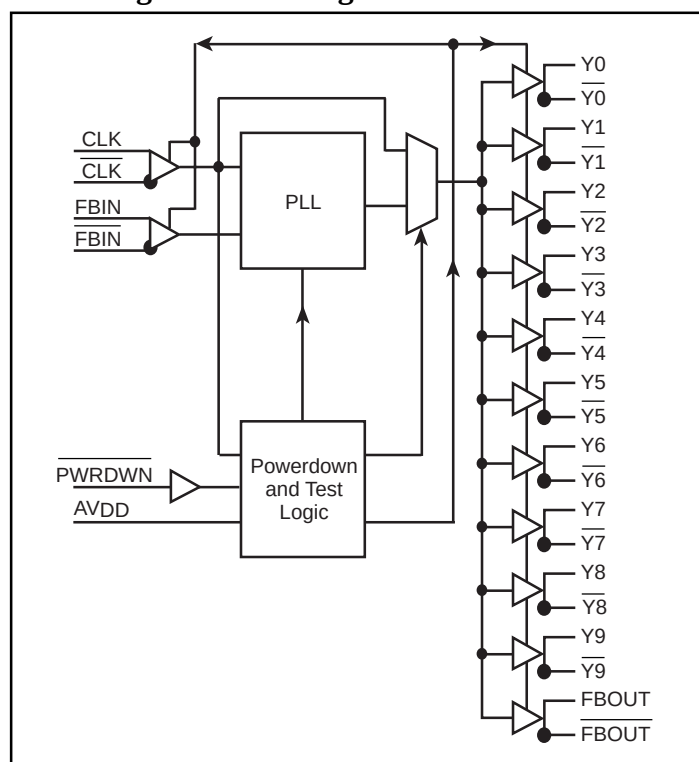
Product Description

PI6CV857L PLL clock device is developed for registered DDR DIMM applications. This PLL Clock Buffer is designed for 2.5 V_{DDQ} and 2.5V AV_{DD} operation and differential data input and output levels. The device is a zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{\text{Y}}[0:9]$) and one differential pair feedback clock outputs (FBOU, $\overline{\text{FBOU}}$). The clock outputs are controlled by the input clocks (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the 2.5V LVCMOS input (PWRDWN) and the Analog Power input (AV_{DD}). When input PWRDWN is low while power is applied, the input receivers are disabled, the PLL is turned off and the differential clock outputs are 3-stated. When the AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes.

When the input frequency falls below a suggested detection frequency that is below the operating frequency of the PLL, the device will enter a low power mode. An input frequency detection circuit will detect the low frequency condition and perform the same low power features as when the PWRDWN input is low.

The PLL in the PI6CV857L clock driver uses the input clocks (CLK, $\overline{\text{CLK}}$) and the feedback clocks (FBIN, $\overline{\text{FBIN}}$) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], $\overline{\text{Y}}[0:9]$). The PI6CV857L is also able to track Spread Spectrum Clocking for reduced EMI.

Block Diagram/Pin Configuration



Pinout Table

Pin Name	Pin No.	I/O Type	Description
CLK CLK	13 14	I	Reference Clock input
Y _x	3,5,10,20,22,27,29,39,44,46	O	Clock outputs.
$\overline{Y_x}$	2,6,9,19,23,26,30,40,43,47		Complement Clock outputs.
FBOU _T FBOU _T	32 33		Feedback output, and Complement Feedback Output
FBIN FBIN	36 35	I	Feedback Input, and Complement Feedback Input
$\overline{PWRDWN}$	37		Power down and output disable for all Y _x and $\overline{Y_x}$ outputs. When $\overline{PWRDWN} = 0$, the part is powered down and the differential clock outputs are disabled to a 3-state. When $\overline{PWRDWN} = 1$, all differential clock outputs are enabled and run at the same frequency as CLK.
V _{DDQ}	4,11,12,15,21,28,34,38,45		Power Supply for I/O.
AV _{DD}	16	Power	Analog /core power supply. AV _{DD} can be used to bypass the PLL for testing purposes. When AV _{DD} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	17	Ground	Analog/core ground. Provides the ground reference for the analog/core circuitry
GND	1,7,8,18,24,25,31,41,42,48		Ground

Function Table

Inputs				Outputs				PLL
AV _{DD}	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOU _T	$\overline{FBOU_T}$	
GND	H	L	H	L	H	L	H	Bypassed/off
GND	H	H	L	H	L	H	L	Bypassed/off
X	L	L	H	Z	Z	Z	Z	off
X	L	H	L	Z	Z	Z	Z	off
2.5V(nom)	H	L	H	L	H	L	H	on
2.5V(nom)	H	H	L	H	L	H	L	on
2.5V(nom)	X	<20 MHz ⁽¹⁾		Z	Z	Z	Z	off

Notes: For testing and power saving purposes, PI6CV857L will power down if the frequency of the reference inputs CLK, $\overline{CLK}$ is well below the operating frequency range. The maximum power down clock frequency is below 20 MHz. For example, PI6CV857L will be powered down when the CLK, $\overline{CLK}$ stop running.

Z = High impedance

X = Don't care

Absolute Maximum Ratings (Over operating free-air temperature range)

Symbol	Parameter	Min.	Max.	Units
V _{DDQ} , AV _{DD}	I/O supply voltage range and analog/core supply voltage range	− 0.5	3.6	V
V _I	Input voltage range	− 0.5	V _{DDQ} +0.5	
V _O	Output voltage range	− 0.5		
I _{IK}	Input Clamp Current	− 50	50	mA
I _{OK}	Output Clamp Current	− 50	50	
I _O	Continuous output Current	− 50	50	
I _{O(PWR)}	Continuous current through each V _{DD} , V _{DDQ} , or GND	− 100	100	
T _{stg}	Storage temperature	− 65	150	°C

Note: Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Specifications
Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units
AV_{DD}	Analog/core supply voltage	2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	
V_{IL}	Low-level input voltage for $\overline{PWRDWN}$ pin	-0.3		0.7	
V_{IH}	High-level input voltage for $\overline{PWRDWN}$ pin	1.7		$V_{DDQ} + 0.3$	
V_I	Input Voltage	0		V_{DDQ}	
I_{OH}	High-level output current	-		12	mA
I_{OL}	Low-level output current	-		-12	
V_{IX}	Input differential-pair crossing voltage	$(V_{DDQ}/2) - 0.2$		$(V_{DDQ}/2) + 0.2$	V
V_{OX}	Output differential-pair crossing voltage at the DRAM clock input	$(V_{DDQ}/2) - 0.15$		$(V_{DDQ}/2) + 0.15$	
V_{IN}	Input voltage level	-0.3		$V_{DDQ} + 0.3$	
V_{ID}	Input differential voltage between CLK and $\overline{CLK}$	0.36		$V_{DDQ} + 0.6$	
V_{OD}	Output differential voltage between $Y[n]$ & $\overline{Y[n]}$ and $FBOUT$ & $\overline{FBOUT}$	0.7		$V_{DDQ} + 0.6$	
T_A	Operating free air temperature	0		70	°C

Timing Requirements (Over recommended operating free-air temperature)

Symbol	Description	AVDD, VDDQ = 2.5V ±0.2V		Units
		Min.	Max.	
f _{CK}	Operating clock frequency ^(1,2)	60	170	MHz
	Application clock frequency ⁽³⁾	95	170	
t _{DC}	Input clock duty cycle	40	60	%
t _{STAB}	PLL stabilization time after powerup		100	µs

Notes:

1. The PLL is able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL is able to lock, but in which the clock is not required to meet the other timing parameters. (Used for low-speed debug).
3. Application clock frequency indicates a range over which the PLL meets all of the timing parameters.

Electrical Characteristics

Parameter		Test Conditions	A _{VDD} , V _{DDQ}	Min.	Typ.	Max.	Units
V _{IK}	All inputs	I _I = −18mA	2.3V			−1.2	V
V _{OH}	High output voltage	I _{OH} = −100μA	2.3 to 2.7V	VDDQ− 0.1			
		I _{OH} = −12mA	2.3V	1.7			
V _{OL}	Low output voltage	I _{OL} = 100μA	2.3 to 2.7V			0.1	
		I _{OL} = 12mA	2.3V			0.6	
I _I	CLK, FBIN	V _I = V _{DDQ} or GND	2.7V			±10	μA
	$\overline{\text{PWRDWN}}$	V _I = V _{DDQ} or GND					
I _{DDQ}	Dynamic supply current of V _{DDQ}	V _{DD} = 2.7V				300	mA
	Static supply current	CLK & $\overline{\text{CLK}}$ <20 MHz or $\overline{\text{PWRDWN}}$ = Low ⁽⁴⁾				100	μA
I _{ADD}	Dynamic supply current of A _{VDD}	V _{DD} = 2.7V					12
	Static supply current	CLK & $\overline{\text{CLK}}$ <20 MHz or $\overline{\text{PWRDWN}}$ = Low ⁽⁴⁾				100	μA
C _I	CLK and $\overline{\text{CLK}}$	V _I = V _{DDQ} or GND	2.5V	2.0		3.5	pF
	FBIN and $\overline{\text{FBIN}}$						
C _{I(Δ)}	CLK and CLK	V _I = V _{DDQ} or GND	2.5V	−0.25		0.25	
	FBIN and FBIN						
ΔC _I	Part to Part input Capacitance Variation ⁽⁵⁾	V _I = V _{DDQ} or GND	2.5V			1	

Note:

4. The maximum power-down clock frequency is below 20 MHz.
5. Guaranteed by design, but not production tested.

AC Specifications

Switching characteristics over recommended operating free-air temperature range (unless otherwise noted)(See Figure 1 & 2)

Parameter	Description	Diagram	AV _{CC} , V _{DDQ} = 2.5V ±0.2V			Units
			Min.	Nom.	Max	
tjit(cc)	Cycle-to-cycle jitter	see Figure 3	−75		75	ps
t(θ)	Static phase offset ⁽¹⁾	see Figure 4	−50	0	50	
tsk(o)	Output clock skew	see Figure 5			100	
tjit(per)	Period jitter	see Figure 6	−75		75	
tjit(hper)	Half-period jitter	see Figure 7	−100		100	
tsl(i)	Input clock slew rate ⁽²⁾	see Figure 8	1.0		4.0	V/ns
tsl(o)	Output clock slew rate ⁽²⁾	see Figure 8	1.0		2.0	
The PLL on the PI6CV857L is capable of meeting all the above parameters while supporting SSC synthesizers with the following parameters ⁽³⁾ .						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		−0.50	%
	PLL loop bandwidth		2			MHz
	Phase angle				−0.031	degrees

Notes:

1. Static Phase offset does not include Jitter.
2. The slew rate is determined from the IBIS model with test load shown in Figure1.
3. The SSC requirements meet the Intel PC100 SDRAM Registered DIMM specification.

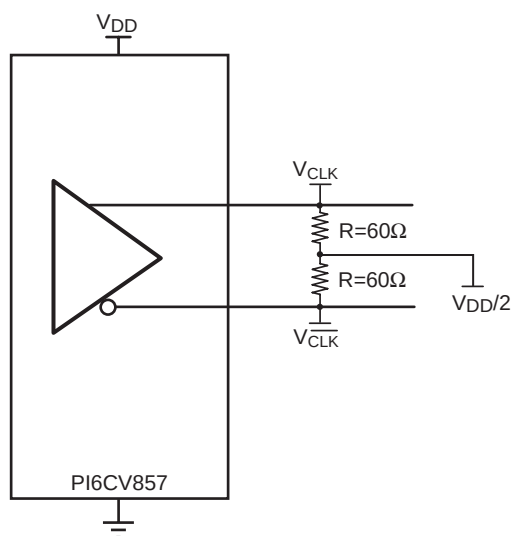


Figure 1. IBIS Model Output Load

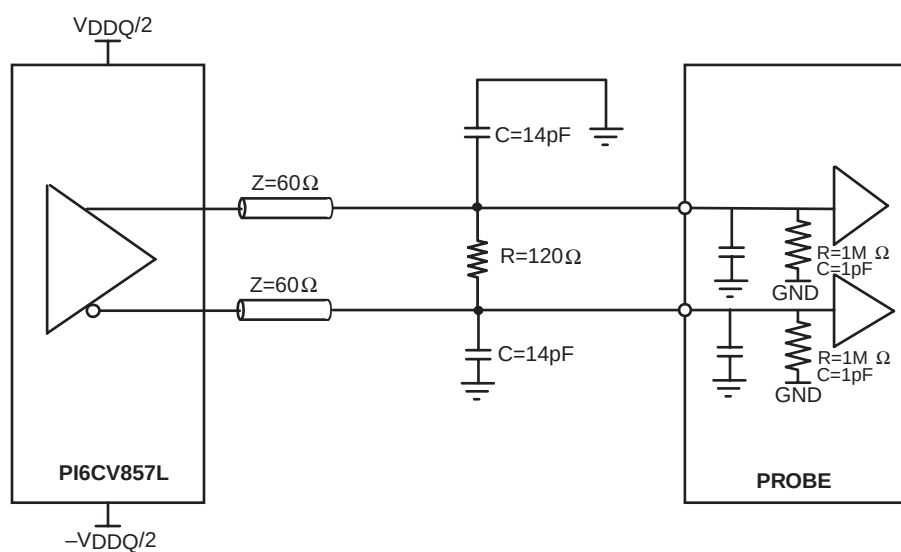


Figure 2. Output Load Test Circuit

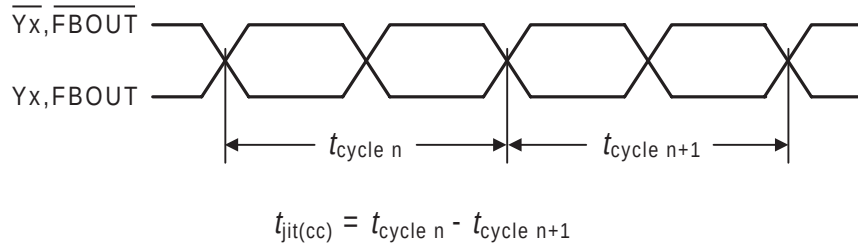


Figure 3. Cycle-to-Cycle Jitter

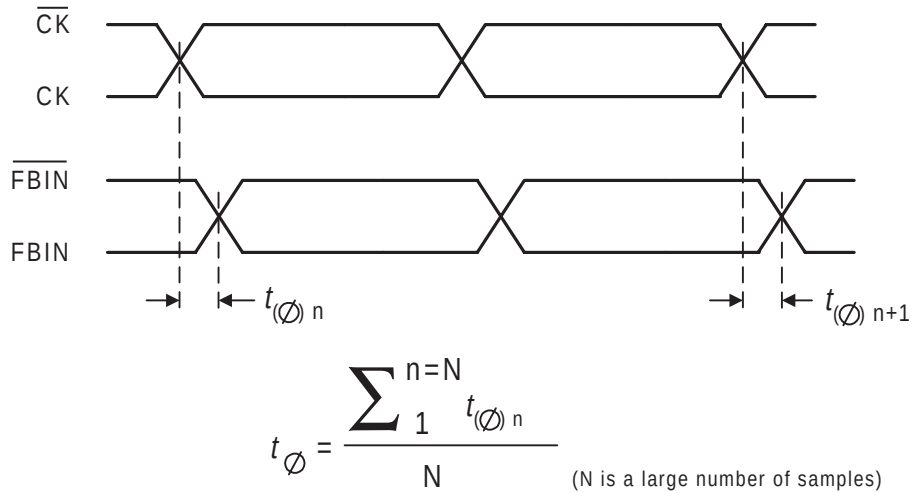


Figure 4. Static Phase Offset

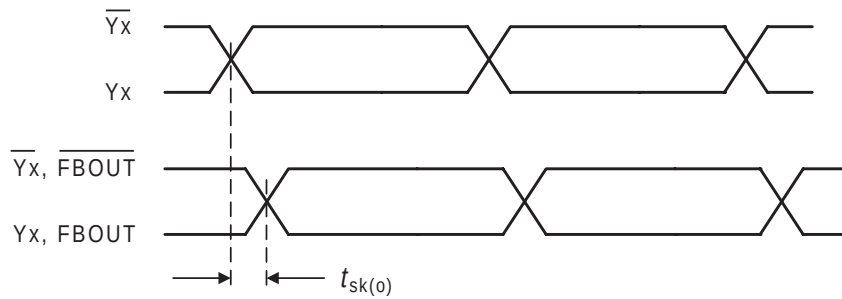


Figure 5. Output Skew

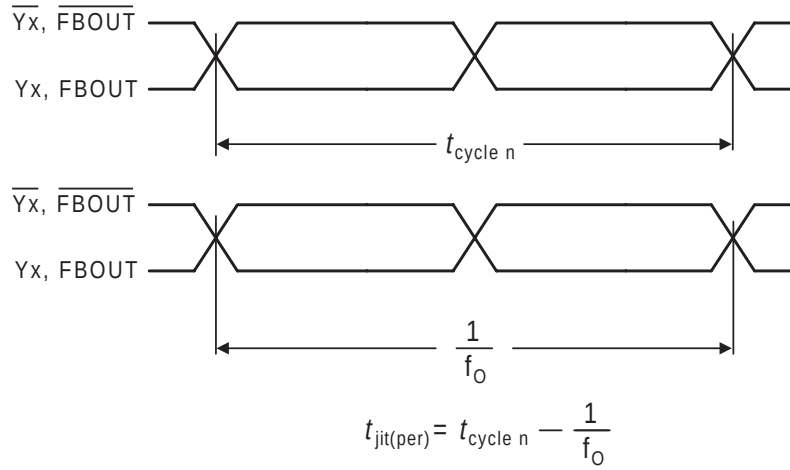


Figure 6. Period Jitter

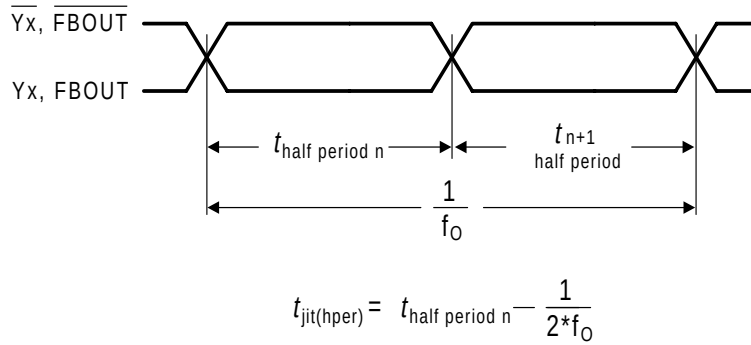


Figure 7. Half-Period Jitter

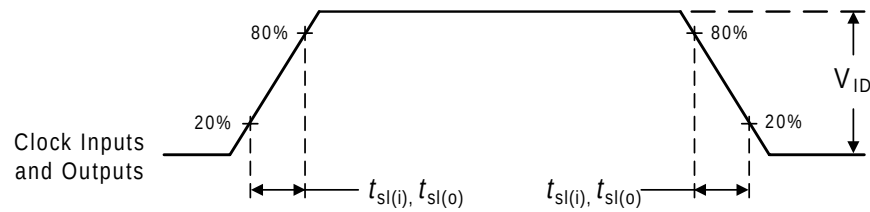
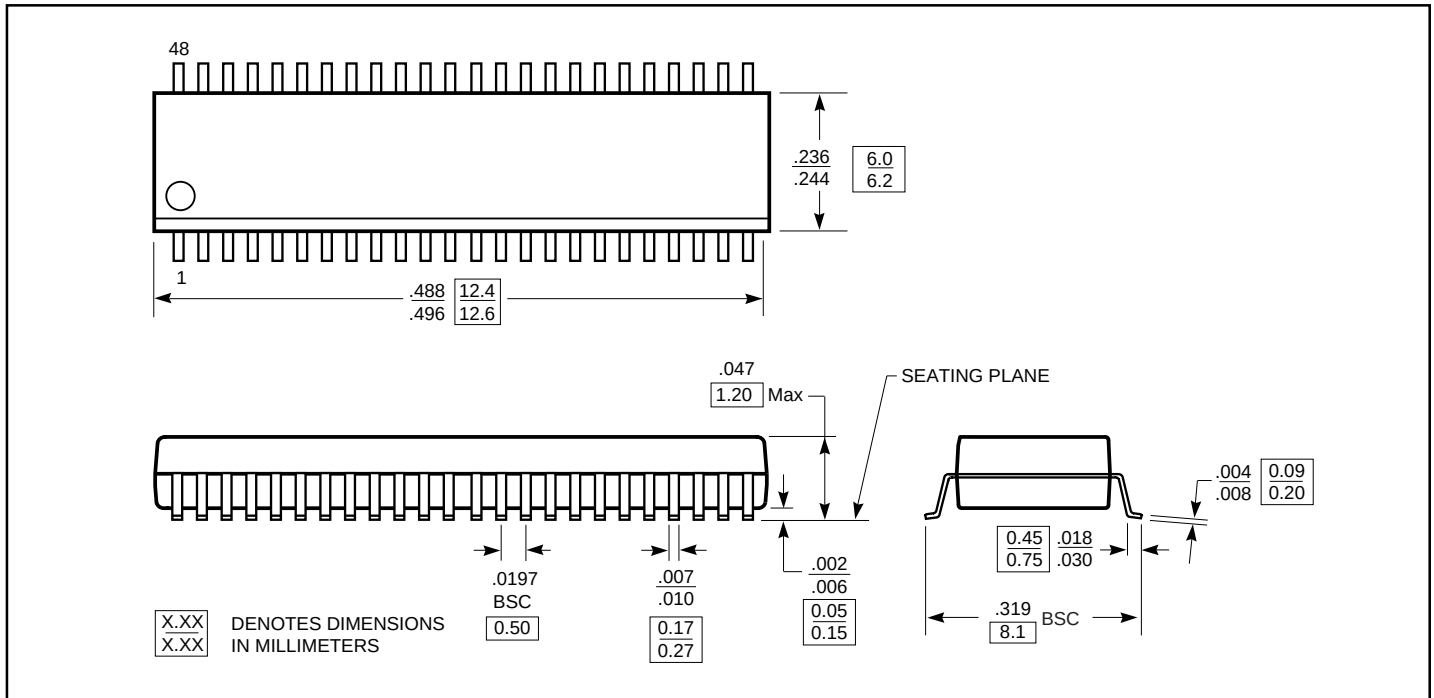
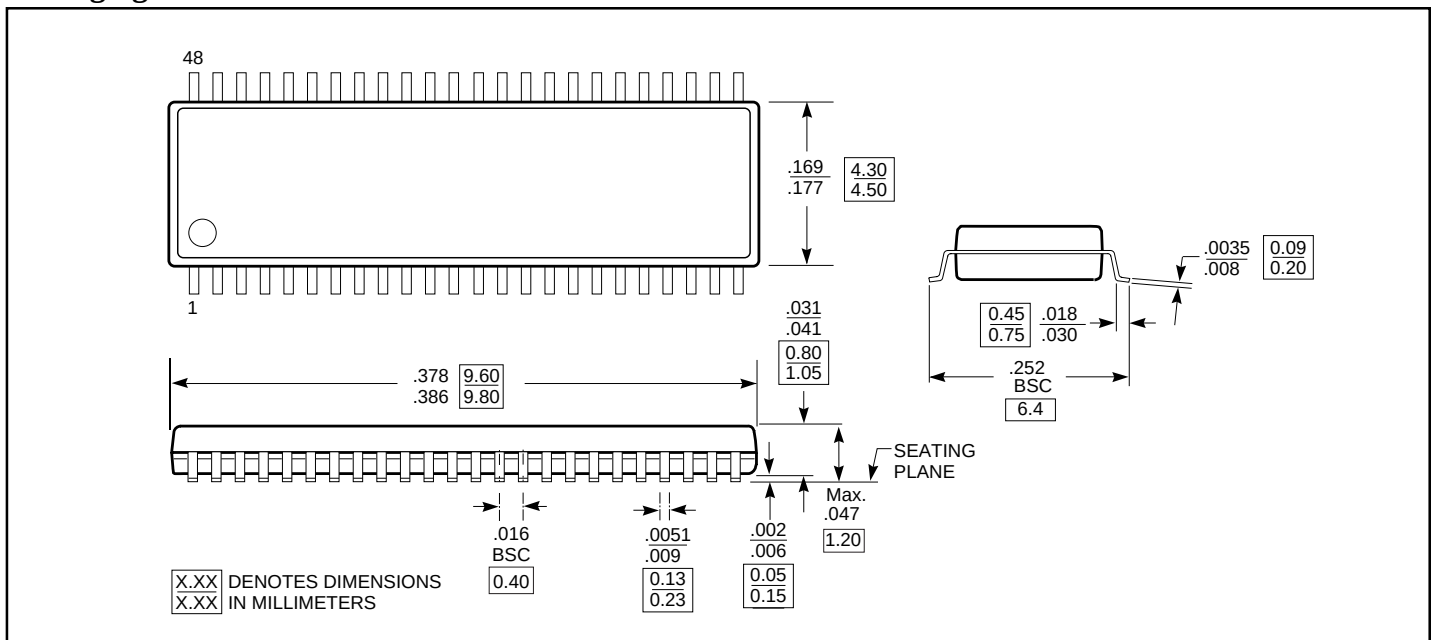


Figure 8. Input and Output Slew Rates

Packaging Mechanical: 48-Pin TSSOP

Packaging Mechanical: 48-Pin TVSOP

Ordering Information

Ordering Code	Package Name	Package Type
PI6CV857LA	A48	48-pin, 240-mil wide TSSOP
PI6CV857LK	K48	48-pin, 173-mil wide TVSOP