PERICOM®

PI5A3159

SOTINY™ 1-Ohm Low-Voltage SPDT Analog Switch

Product Features

- CMOS Technology for Bus and Analog Applications
- SOTINY Package Technology: 6-pin, SOT-23 and TDFN
- Low ON-Resistance: 2-ohms at 3.0V
- Wide V_{CC} Range: +1.8V to +5.5V
- Low Power Consumption : 5µW
- Rail-to-Rail switching throughout Signal Range
- Fast Switching Speed: 30ns max. at 5V
- High Off Isolation: –57dB at 10MHz
- –57dB (1 MHz) Crosstalk Rejection Reduces Signal Distortion
- Break-Before-Make Switching
- Extended Industrial Temperature Range: –40°C to 85°C
- Low ON-Resistance Replacement for NC7SB3157
- Packages: 6-pin SOT-23 (T), and 6-pin TDFN-6 (ZC)

Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals

Pin Description

Pin Number	Name	Description
1	B1	Data Port
2	GND	Ground
3	B0	Data Port (Normally Closed)
4	A	Common Output/Data Port
5	V_{CC}	Positive Power Supply
6	S	Logic Control

Logic Function Table

Logic Input (S)	Function
0	B_0 Connected to A
1	B_1 Connected to A

Description

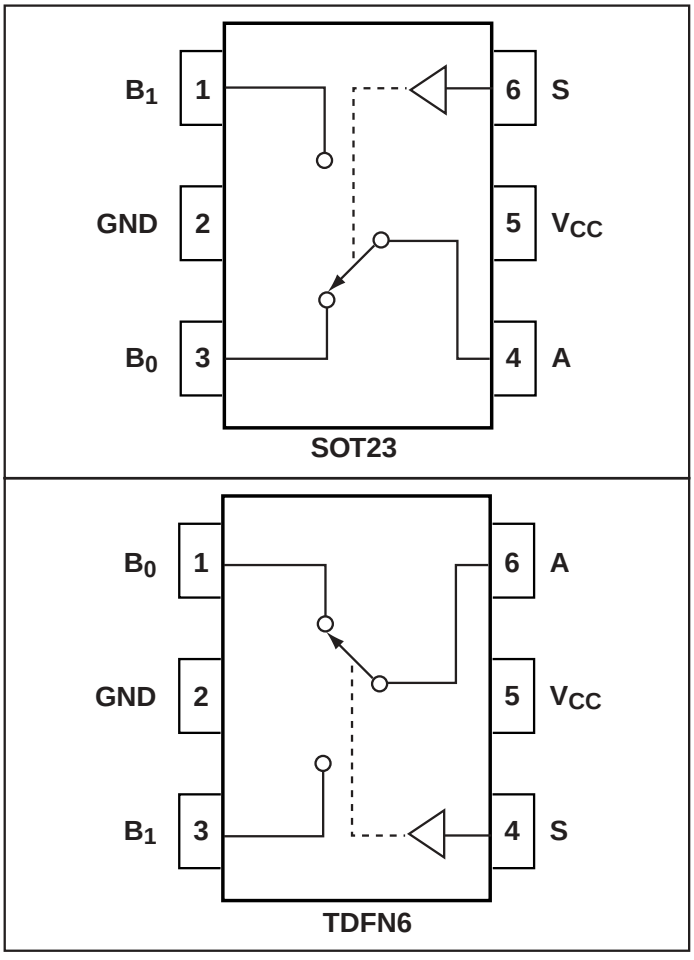
The PI5A3159 is a high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, 1.8V to 5.5V, the PI5A3159 has a maximum ON-Resistance of 4-ohms at 1.8V, 2.4-ohms at 2.3V & 1-ohms at 4.5V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

Control input, S, tolerates input drive signals up to 5.5V, independent of supply voltage.

PI5A3159 is a low On-Resistance replacement for the PI5A3157 and NC7SB3157.

Connection Diagrams



Absolute Maximum Ratings

Voltages Referenced to GND
V+ ..... –0.5V to +5.5V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... –0.5V to V_+ +0.3V
or 30mA, whichever occurs first

Current (any terminal) ..... ±200mA

Peak Current, COM, NO, NC
(Pulsed at 1ms, 10% duty cycle) ..... ±400mA

Thermal Information

Continuous Power Dissipation

SOT23-6 (derate 7.1mW/ºC above +70ºC) 0.5W

Storage Temperature ..... –65ºC to +150ºC

Lead Temperature (soldering, 10s) ..... +300ºC

Note:

1. Signals on NC, NO, COM, or IN exceeding V+ or Gnd are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +5V Supply

(V+ = +5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Switch							
Analog Signal Range (3,4)	V_{ANALOG}		Full	0		V+	V
On Resistance	R_{ON}	V+ = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = +2.5V	25		0.70	0.90	ohm
			Full			1.1	
On-Resistance Match Between Channels(5)	ΔR_{ON}		25		0.03	0.05	
			Full			0.10	
On-Resistance Flatness(6)	$R_{FLAT(ON)}$	V+ = 4.5V, I_{COM} = -30mA, V_{NO} or V_{NC} = 1V, 1.5V, 2.5V	25		0.08	0.12	
			Full			0.15	
NO or NC Off Leakage Current(7)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0V V_{NO} or V_{NC} = 4.5V	25	2	0.01	2	nA
			Full	–20		20	
COM On Leakage Current(7)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = +4.5V V_{NO} or V_{NC} = +4.5V	25	–4		4	
			Full	–40	0.3	40	

Electrical Specifications - Single +5V Supply (continued)

(V+ = +5V ± 10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Switch							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	2.4			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel				0.8	
Input Current with Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		–1	0.005	1	µA
Input Current with Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		–1	0.005	1	
Dynamic							
Turn-On-Time	t_{ON}	V_{CC} = 5V, Figure 1	25		20	35	ns
			Full		–	40	
Turn-Off-Time	t_{OFF}		25		15	20	
			Full		–	35	
Break-Before-Make	t_{BBM}	Figure 3	25	1	12	14.5	
			Full	1	17.5		
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0ohm, Figure 2	25		40		pC
Off Isolation	OIRR	R_L = 50ohms, f = 1MHz, Figure 4			–57		dB
CrossTalk(9)	X_{TALK}	R_L = 50ohms, f = 1MHz, Figure 5			–57		
NC or NO Capacitance	$C_{NC/NO(OFF)}$	f = 1MHz, Figure 6			42		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 6			83		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 7			130		
Supply							
Power-Supply Range	V+		Full	1.8		5.5	V
Positive Supply Current	I+	V+ = 5.5V, VIN = 0V or V+ All Channels on or off			0.5	0.1	µA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. Device is NOT guaranteed to function per the datasheet specification outside of 0 to V+ range.
5. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
6. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.
7. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
8. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 4.
9. Between any two switches. See Figure 5.

Electrical Specifications - Single +3.3V Supply

(V+ = +3.3V ± 10%, GND = 0V, V_{INH} = 2.0V, V_{INL} = 0.6V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ =3V, I_{COM} = –24mA V_{NO} or V_{NC} = 2.0V	25		1.4	1.8	Ohm
			Full			2.2	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ =3.3V, I_{COM} = –24mA V_{NO} or V_{NC} = 0.8V, 2.0V	25		0.04	0.05	
			Full		0.11		
On-Resistance Flatness	$R_{FLAT(ON)}$		25		0.17	0.2	
			Full		0.25		
Dynamic							
Turn-On-Time	t_{ON}	V_{CC} = 5V, Figure 1	25		30	40	ns
			Full		–	55	
Turn-Off-Time	t_{OFF}		25		20	25	
			Full			40	
Break-Before-Make	t_{BBM}	Figure 3	25	1	21	29	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		30		pC
Supply							
Positive Supply Current	I+	V+ = 3.6V, VIN =0V or V+ All Channels on or off	Full		0.5	1	µA
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	2			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel	Full			0.6	
Input High Current	I_{INH}	V_{IN} = 2.4V, all others = 0.8V	Full	–1		1	µA
Input Low Current	I_{INL}	V_{IN} = 0.8V, all others = 2.4V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

Electrical Specifications - Single +2.5V Supply

(V+ = +2.5V ± 10%, GND = 0V, V_{INH} = 1.8V, V_{INL} = 0.6V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ =2.5V, I_{COM} = –8mA V_{NO} or V_{NC} = 1.8V	25		1.6	2	Ohm
			Full		–	2.7	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ =2.5V, I_{COM} = –8mA V_{NO} or V_{NC} = 0.8V, 1.8V	25		0.13	0.16	
			Full		0.2	–	
On-Resistance Flatness	$R_{FLAT(ON)}$		25		0.25	0.3	
			Full		0.45	–	
Dynamic							
Turn-On-Time	t_{ON}	V+ =2.5V, V_{NO} or V_{NC} = 1.8V, Figure 1	25		40	55	ns
			Full		–	70	
Turn-Off-Time	t_{OFF}		25		30	40	
			Full		–	55	
Break-Before-Make	t_{BBM}	Figure 3 PI5A4624 Only)	25	1	33	39	
Make-Break-Before	t_{MBB}	Figure 4 PI5A4625 Only)	25	1	9	13	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		20		pC
Supply							
Positive Supply Current	I+	V+ = 2.75V, V_{IN} =0V or V+ All Channels on or off	Full		0.5	1	µA
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	1.8			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel	Full			0.6	
Input High Current	I_{INH}	V_{IN} = 2.0V, all others = 0.8V	Full	–1		1	µA
Input Low Current	I_{INL}	V_{IN} = 0.8V, all others = 2.0V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

Electrical Specifications - Single +1.8V Supply

(V+ = +1.8V ± 10%, GND = 0V, V_{INH} = 1.5V, V_{INL} = 0.6V)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ. (2)	Max. (1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V+	V
On-Resistance	R_{ON}	V+ =1.8V, I_{COM} = –2mA V_{NO} or V_{NC} = 1.5V	25		2.8	4	Ohm
			Full		–	5	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V+ =1.8V, I_{COM} = –2mA V_{NO} or V_{NC} = 0.6V, 1.5V	25		0.44	0.6	
			Full		0.7		
On-Resistance Flatness	$R_{FLAT(ON)}$		25		0.5	0.6	
			Full		0.9		
Dynamic							
Turn-On-Time	t_{ON}	V+ =1.8V, V_{NO} or V_{NC} = 1.5V, Figure 1	25		65	70	ns
			Full			95	
Turn-Off-Time	t_{OFF}		25		40	55	
			Full			70	
Break-Before-Make	t_{BBM}	Figure 3	25	1	60	72	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		10		pC
Supply							
Positive Supply Current	I+	V+ = 2.0V, V_{IN} =0V or V+ All Channels on or off	Full		0.5	1	µA
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	1.8			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel	Full			0.6	
Input High Current	I_{INH}	V_{IN} = 1.5V, all others = 0.8V	Full	–1		1	µA
Input Low Current	I_{INL}	V_{IN} = 0.8V, all others = 1.5V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

Test Circuits/Timing Diagrams

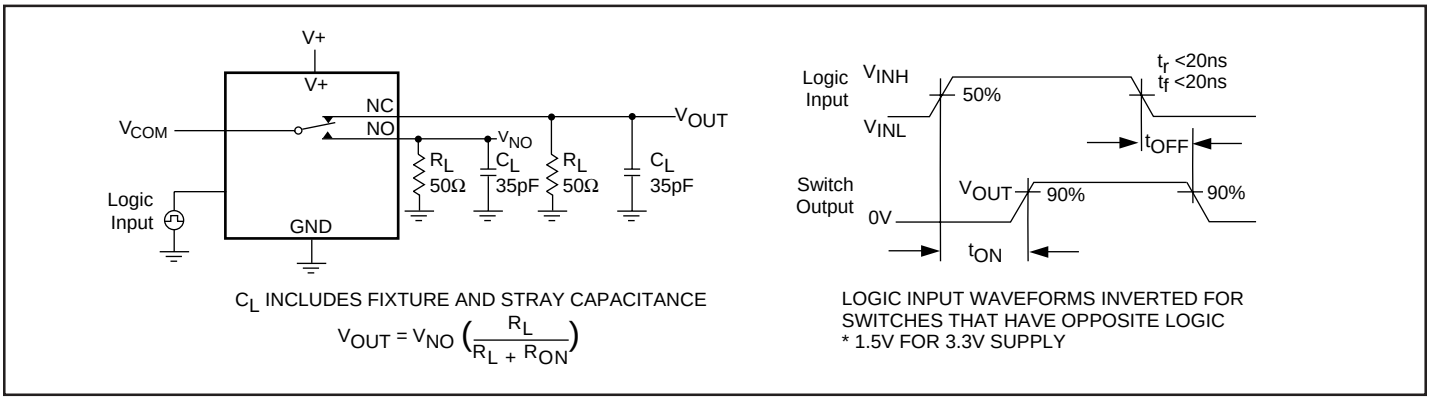


Figure 1. Switching Time

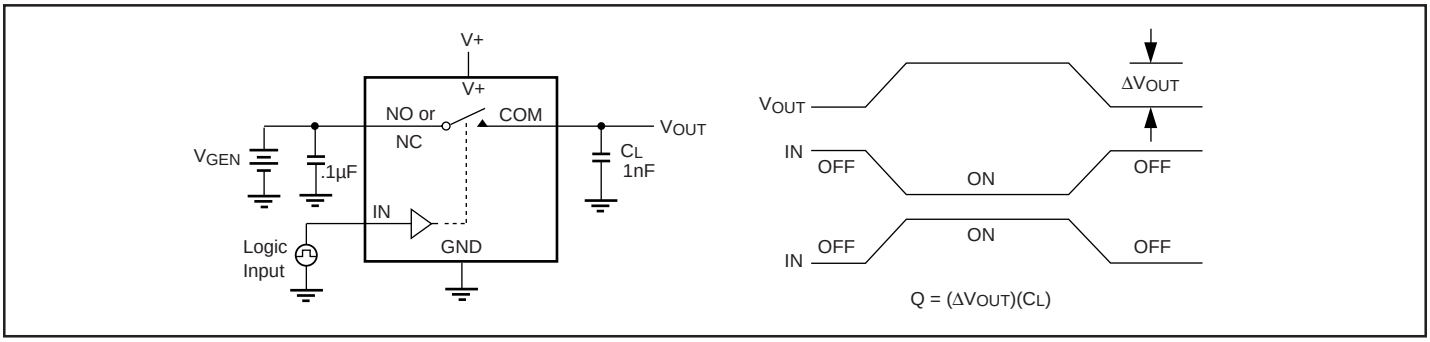


Figure 2. Charge Injection

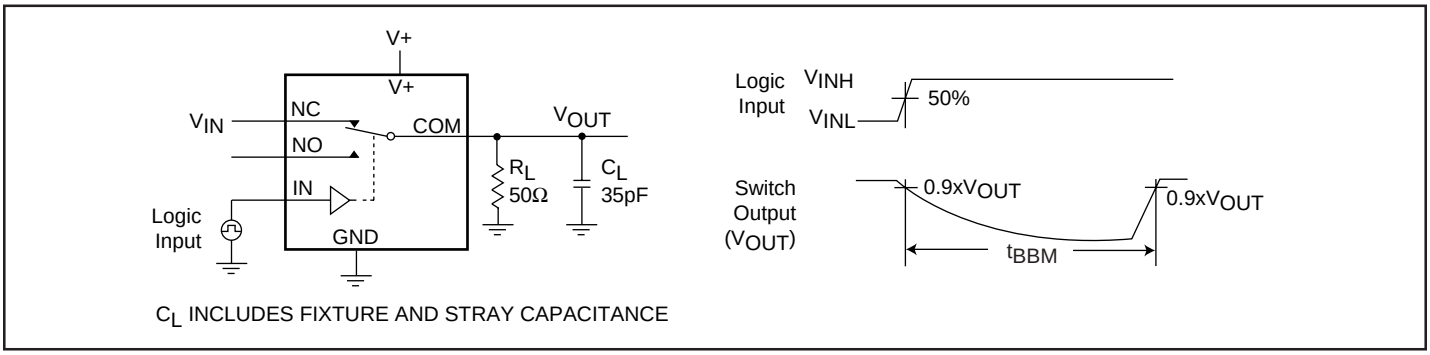


Figure 3. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)

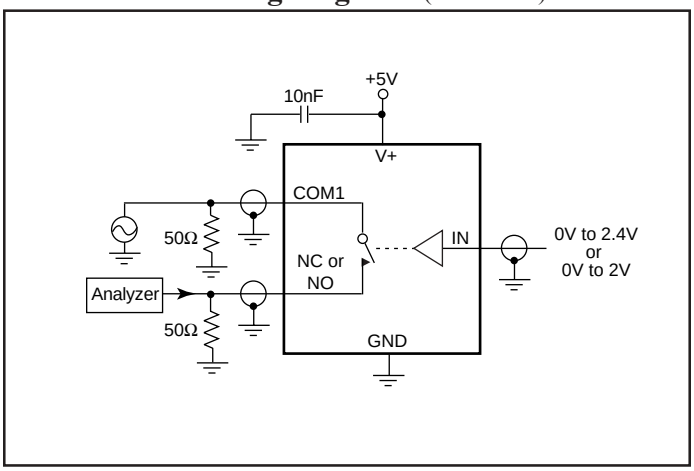


Figure 4. Off Isolation/On-Channel Bandwidth

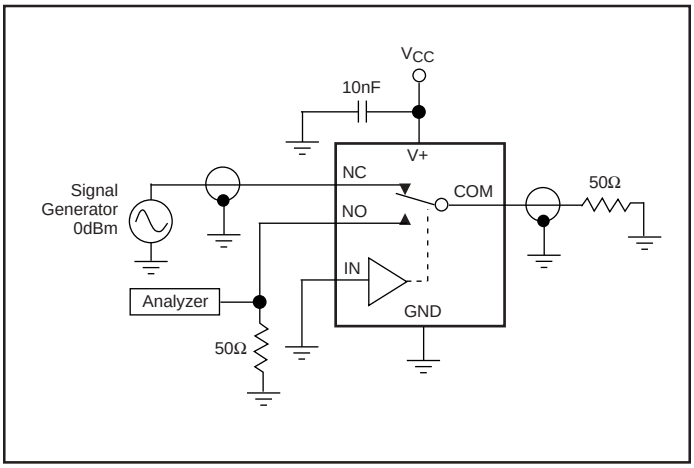


Figure 5. Crosstalk

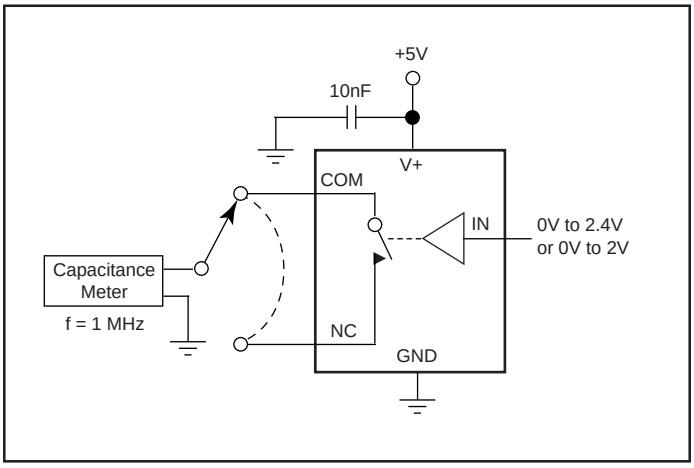


Figure 6. Channel-Off Capacitance

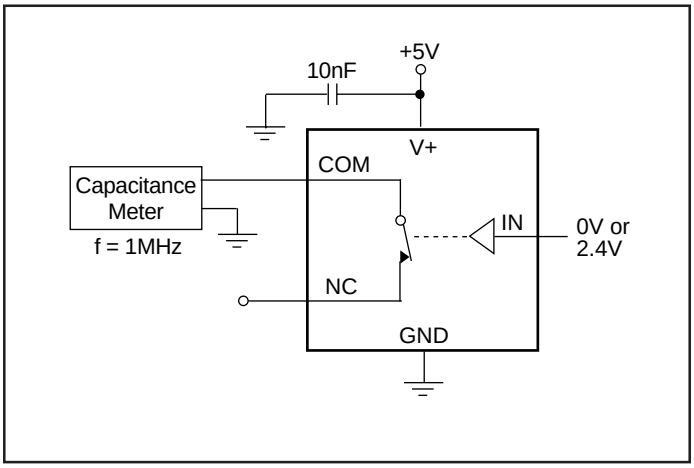


Figure 7. Channel-On Capacitance

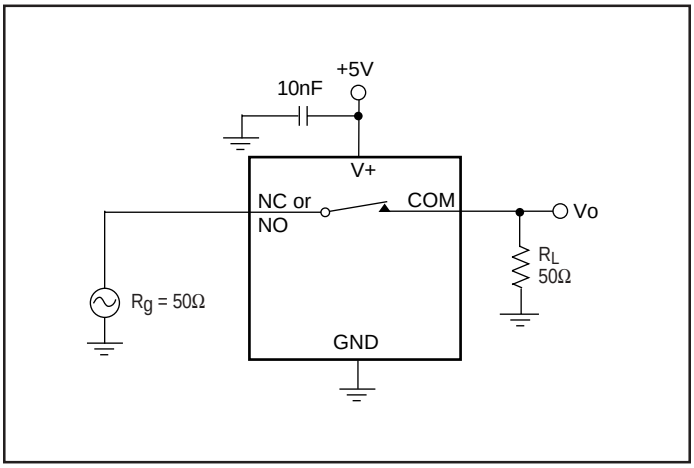
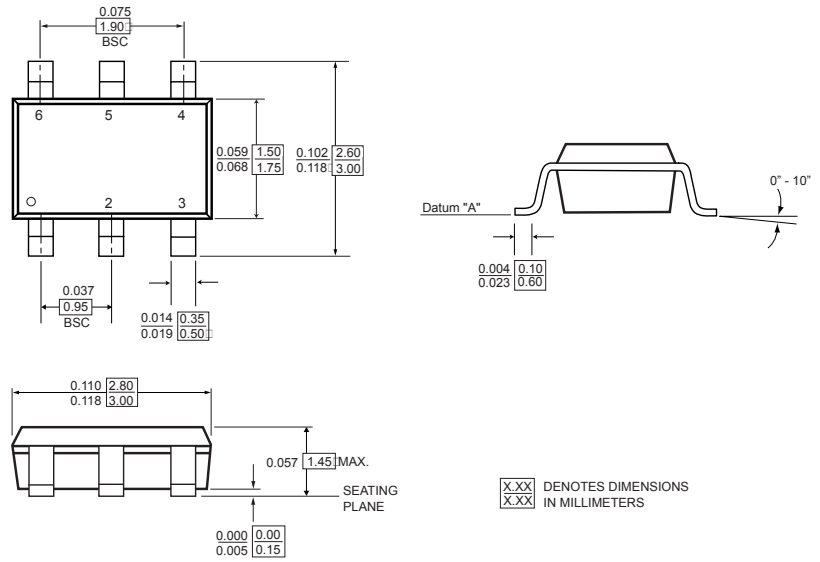
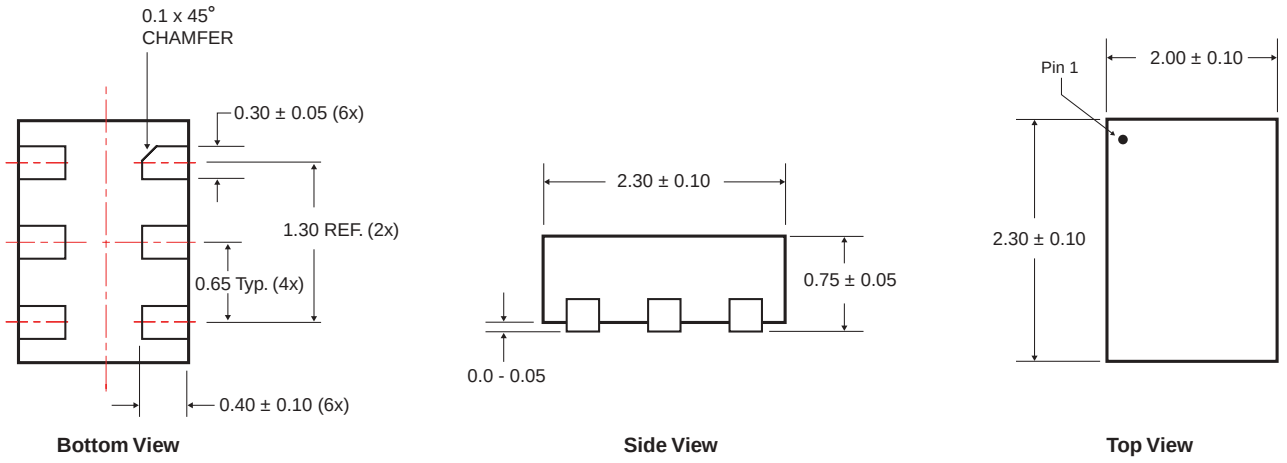


Figure 8. Bandwidth

Packaging Mechanical: 6-Pin SOT-23(T) Package



Packaging Mechanical: 6-Pin TDFN (ZC)



Thermal Characteristics can be found on the world wide web at: http://www.pericom.com/packaging/mechanicals.php
Number of transistors : 753

Ordering Information

Part Number	Package	Package Top Mark
PI5A3159TX	SOT-23	A3B
PI5A3159ZCX	TDFN-6	TBD

Pericom Semiconductor Corporation
2380 Bering Drive • San Jose, CA 95131 • 1-800-435-2336 • Fax (408) 435-1100 • http://www.pericom.com