

3.0V, SOTINY™ 0.4Ω Single-Supply SPDT Analog Switch

Features

- Low On-Resistance: 0.4Ω (+2.7V Supply)
- R_{ON} Matching: 0.1Ω Max. at 25 °C
- R_{ON} Flatness: 0.1Ω Max. (+3.0V Supply) at 25 °C
- Low 2nA Input Leakage at 25 °C
- +1.5V to +3.6V Single-Supply Operation
- Fast Switching Time: 30ns Max.
- Make-Before-Break Switching Guaranteed
- -41dB Off-Isolation at 100KHz
- TTL/CMOS Logic Compatible
- Low Power Consumption: 5μW
- Packages (Pb-free available):
 - 6-pin Small Compact SOT-23
 - 6-pin Ultra Compact Thin Dual in-line Flat No Lead (TDFN)

Applications

- Communication Circuits
- Cellular Phones
- Audio and Video Signal Routing
- Portable Battery-Operated Equipment
- Data Acquisition Systems
- Computer Peripherals
- Telecommunications
- Relay Replacement
- Wireless Terminals and Peripherals
- Hard Drives
- Modems

Truth Table

Logic	NC	NO
0	ON	OFF
1	OFF	ON

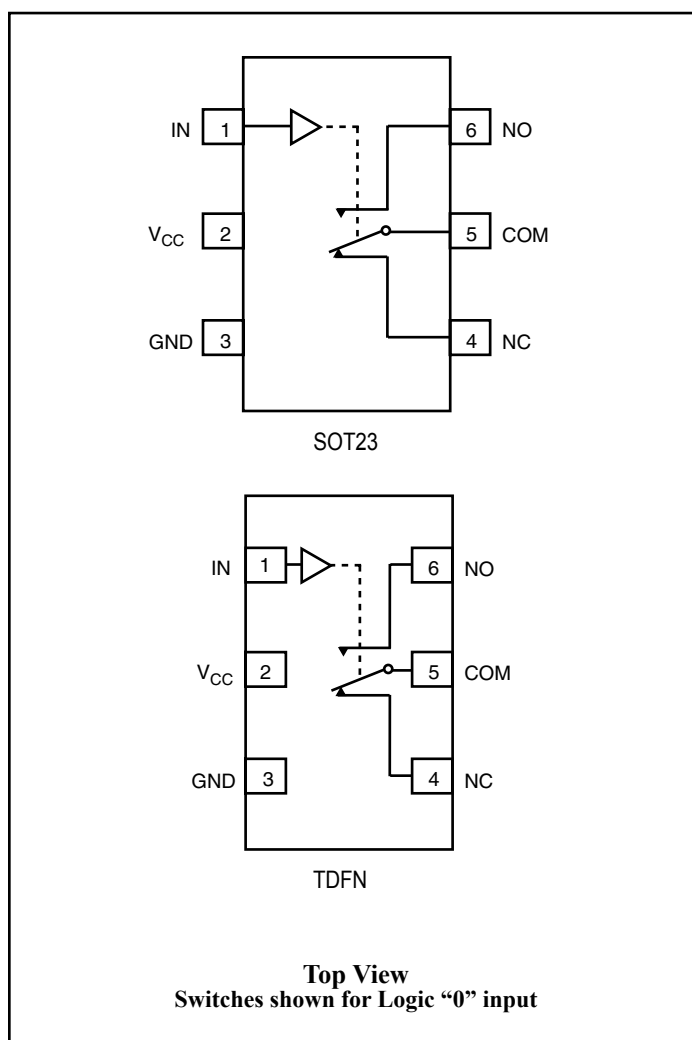
Description

The PI3A4625 is a single-pole, double-throw (SPDT) analog switch. Improved specifications include a low On-Resistance of 0.4Ω, and fast switching times (30ns Max.) with 3.0V supply operation.

Specifications are given for 1.8V, 2.5V and 3.3V power supply operation. Operating voltage range is +1.5V to +3.6V.

To minimize PC board area use, the device is available in the ultra compact TDFN, and the small compact SOT-23 packages.

Functional Diagram, Pin Configuration



Absolute Maximum Ratings

Voltages Referenced to GND

V_{CC} -0.5V to +3.6V

V_{IN} , V_{COM} , V_{NC} , V_{NO} (Note 1) -0.5V to $V_{CC} + 0.3V$
or 30mA, whichever occurs first

Current (any terminal)..... ±200mA

Peak Current, COM, NO, NC

(Pulsed at 1ms, 10% duty cycle)..... ±400mA

Thermal Information

Continuous Power Dissipation

SOT-23 6-pin (derate 7.1mW/°C above +70°C) 0.5W

Storage Temperature -65°C to +150°C

Lead Temperature (soldering, 10s) +300°C

Notes:

1. Signals on NC, NO, COM, or IN exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Single +3.3V Supply

($V_{CC} = +3.3V \pm 10\%$, GND = 0V, $V_{IH} = 1.4V$, $V_{IL} = 0.5V$)

Parameter	Symbol	Conditions	Temp. (°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V_{ANALOG}		Full	0		V_{CC}	V
On-Resistance	R_{ON}	$V_{CC} = 2.7V$, $I_{COM} = 100mA$, V_{NO} or $V_{NC} = +1.5V$	25		0.4	0.5	Ω
			Full			0.55	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR_{ON}		25			0.1	
			Full			0.1	
On-Resistance Flatness ⁽⁵⁾	$R_{FLAT(ON)}$	$V_{CC} = 2.7V$, $I_{COM} = 100mA$, V_{NO} or $V_{NC} = 0.8V, 2.0V$	25			0.1	Ω
			Full			0.1	
NO or NC Off Leakage Current ⁽⁶⁾	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_{CC} = 3.3V$, $V_{COM} = 0V$, V_{NO} or $V_{NC} = +2.0V$	25	-1		1	nA
			Full	-10		10	
COM On Leakage Current ⁽⁶⁾	$I_{COM(ON)}$	$V_{CC} = 3.3V$, $V_{COM} = +2.0V$, V_{NO} or $V_{NC} = +2.0V$	25	-2		2	
			Full	-20		20	

Electrical Specifications - Single +3.3V Supply (continued)
 $(V_{CC} = +3.3V \pm 10\%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)$

Parameter	Symbol	Conditions	Temp. (°C)	Min ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Logic Input							
Input High Voltage	V _{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V _{IL}	Guaranteed Logic LowLevel				0.5	
Input Current with Voltage High	I _{INH}	V _{IN} = 1.4V, all others = 0.5V		−1		1	μA
Input Current with Voltage Low	I _{INL}	V _{IN} = 0.5V, all others = 1.4V		−1		1	
Dynamic							
Turn-On-Time	t _{ON}	V _{CC} = 3.3V, V _{NO} or V _{NC} = 2.0V, Figure 1	25			10	ns
			Full			20	
Turn-Off-Time	t _{OFF}		25			15	
			Full			30	
Make-Before-Break	T _{BBM}		25	1		20	
			Full	1		25	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0Ω, Figure 2	25		40		pC
Off Isolation ⁽⁷⁾	O _{IRR}	R _L = 50Ω, f = 100 KHz, Figure 3			-27		dB
CrossTalk ⁽⁸⁾	X _{TALK}	R _L = 50Ω, f = 100 KHz, Figure 4			-41		
NC or NO Capacitance	C _{NC/NO (OFF)}	f = 1 MHz, Figure 5			75		pF
COM Off Capacitance	C _{COM(OFF)}				75		
COM On Capacitance	C _{COM(ON)}	f = 1 MHz, Figure 6			200		
Supply							
Power-Supply Range	V _{CC}		Full	1.5		3.6	V
Positive Supply Current	I _{CC}	V _{CC} = 3.6V, V _{IN} = 0V or V _{CC}				100	nA

Notes:

- The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
- Guaranteed by design.
- $\Delta R_{ON} = R_{ON \text{ max.}} - R_{ON \text{ min.}}$
- Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.
- Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
- Off Isolation = $20\log_{10} [V_{COM} / (V_{NO} \text{ or } V_{NC})]$. See Figure 4
- Between any two switches. See Figure 5

Electrical Specifications - Single +2.5V Supply

(V_{CC} = +2.5V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Parameter	Symbol	Conditions	Temp. (°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}			0		V _{CC}	V
On-Resistance	R _{ON}	V _{CC} = 2.5V, I _{COM} = −8mA, V _{NO} or V _{NC} = 1.8V	25			0.5	Ω
			Full			0.6	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}	V _{CC} =2.5V, I _{COM} = −8mA, V _{NO} or V _{NC} = 0.8V, 1.8V	25			0.1	
			Full			0.1	
On-Resistance Flatness ⁽⁵⁾	R _{FLAT(ON)}		25			0.1	
			Full			0.1	
Dynamic							
Turn-On-Time	t _{ON}	V _{CC} = 2.5V, V _{NO} or V _{NC} = 1.8V, Figure 1	25			10	ns
			Full			20	
Turn-Off-Time	t _{OFF}		25			20	
			Full			40	
Make- Before-Break	t _{BBM}	Figrue 3	25	1		20	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0V, Figure 2	25		40		pC
Logic Input							
Input High Voltage	V _{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V _{IL}	Guaranteed Logic LowLevel	Full			0.5	
Input High Current	I _{INH}	V _{IN} = 1.4V, all others = 0.5V	Full	−1		1	μA
Input Low Current	I _{INL}	V _{IN} = 0.5V, all others = 1.4V	Full	−1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. ΔR_{ON} = R_{ON} max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

Electrical Specifications - Single +1.8V Supply

(V_{CC} = +1.8V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Parameter	Symbol	Conditions	Temp. (°C)	Min. ⁽¹⁾	Typ. ⁽²⁾	Max. ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V _{ANALOG}			0		V _{CC}	V
On-Resistance	R _{ON}	V _{CC} = 1.8V, I _{COM} = −4mA, V _{NO} or V _{NC} = 1.5V	25			0.6	Ω
			Full			0.6	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR _{ON}	V _{CC} = 1.8V, I _{COM} = −4mA, V _{NO} or V _{NC} = 0.8V, 1.5V	25			0.1	
			Full			0.2	
On-Resistance Flatness ⁽⁵⁾	R _{FLAT(ON)}		25			0.9	
			Full			1.2	
Dynamic							
Turn-On-Time	t _{ON}	V _{CC} = 1.8V, V _{NO} or V _{NC} = 1.5V, Figure 1	25			15	ns
			Full			30	
Turn-Off-Time	t _{OFF}		25			20	
			Full			40	
Make-Before-Break	t _{BBM}	Figure 3	25	1		15	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0V, Figure 2	25		36		pC
Logic Input							
Input High Voltage	V _{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V _{IL}	Guaranteed Logic LowLevel	Full			0.5	
Input High Current	I _{INH}	V _{IN} = 1.4V, all others = 0.5V	Full	−1		1	μA
Input Low Current	I _{INL}	V _{IN} = 0.5V, all others = 1.4V	Full	−1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. ΔR_{ON} = R_{ON} max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-resistance measured.

The diagram on the left shows a switch model. A logic input is connected to a switch controlled by V_{COM} . The switch connects the input to either V_{CC} or GND. The output node is connected to V_{CC} through a resistor R_L (50Ω) and to GND through a parallel combination of a capacitor C_L (35pF) and a resistor R_L (50Ω). The output voltage is V_{OUT} . The text below the diagram states: "C_L INCLUDES FIXTURE AND STRAY CAPACITANCE" and provides the formula:
$$V_{OUT} = V_{NO} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

The diagram on the right shows logic input waveforms. The Logic Input consists of V_{INH} and V_{INL} . The Switch Output is V_{OUT} . The waveforms show a transition from 0V to 90% of V_{OUT} with a rise time t_{ON} and a fall time t_{OFF} . The input signals have a 50% duty cycle and transition times $t_r < 20ns$ and $t_f < 20ns$.

The circuit diagram shows a 555 timer configured as a monostable multivibrator. The timing network consists of a resistor R and a capacitor C connected to pins 1 (GND), 5 (V_{CC}), and 6 (COM). The trigger pin (2) is connected to GND through a 10 kΩ resistor. The output pin (3, NO or NC) is connected to V_{CC} through a 10 kΩ resistor and to the timing capacitor C . The output voltage is V_{OUT} . The timing capacitor C is labeled with a value of 1 nF. The input pin (4, IN) is connected to a logic input through a 10 kΩ resistor. The output pin (5, OUT) is connected to V_{CC} through a 10 kΩ resistor. The output voltage is V_{OUT} . The timing capacitor C is labeled with a value of 1 nF. The input pin (4, IN) is connected to a logic input through a 10 kΩ resistor. The output pin (5, OUT) is connected to V_{CC} through a 10 kΩ resistor. The output voltage is V_{OUT} .

The timing diagram shows the output voltage V_{OUT} and the input signal IN over time. The input signal IN is a square wave that transitions from OFF to ON and back to OFF. The output voltage V_{OUT} is a square wave that transitions from 0 to V_{CC} when IN transitions from OFF to ON, and returns to 0 when IN transitions from ON to OFF. The pulse width of the output is labeled ΔV_{OUT} . The output voltage is V_{OUT} . The input signal IN is a square wave that transitions from OFF to ON and back to OFF. The output voltage V_{OUT} is a square wave that transitions from 0 to V_{CC} when IN transitions from OFF to ON, and returns to 0 when IN transitions from ON to OFF. The pulse width of the output is labeled ΔV_{OUT} .

The formula for the output pulse width is given as:

$$Q = (\Delta V_{OUT})(C_L)$$
[illegible]

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Test Circuits/Timing Diagrams (continued)

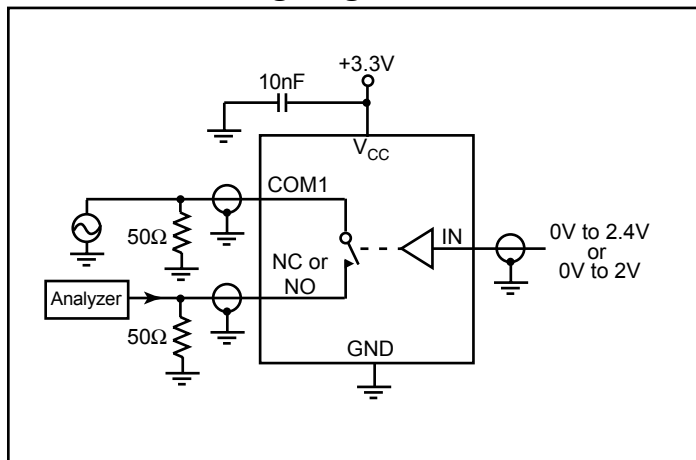


Figure 4. Off Isolation

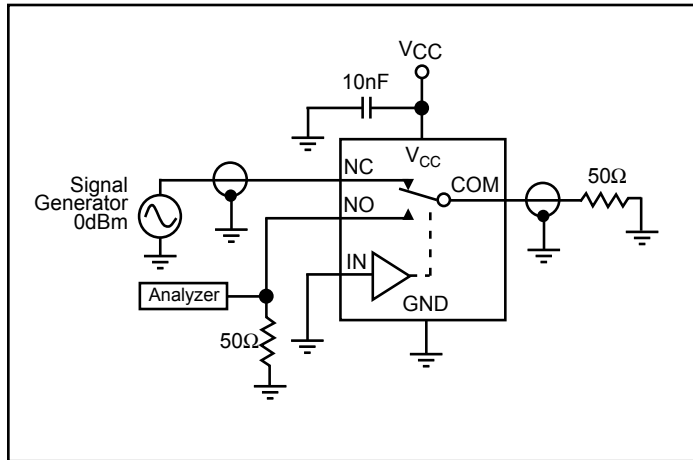


Figure 5. Crosstalk

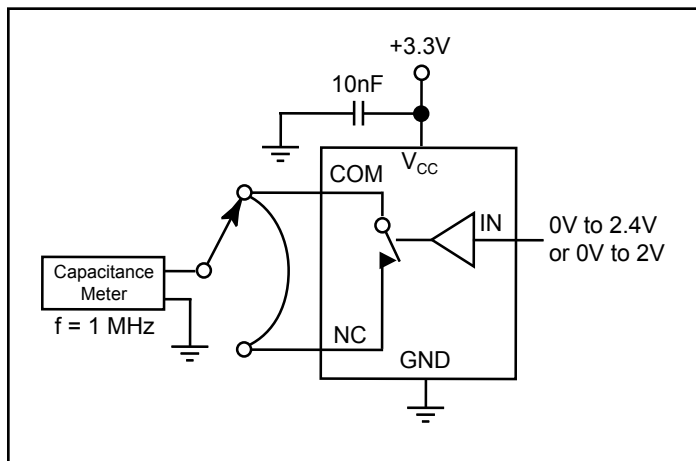


Figure 6. Channel-Off Capacitance

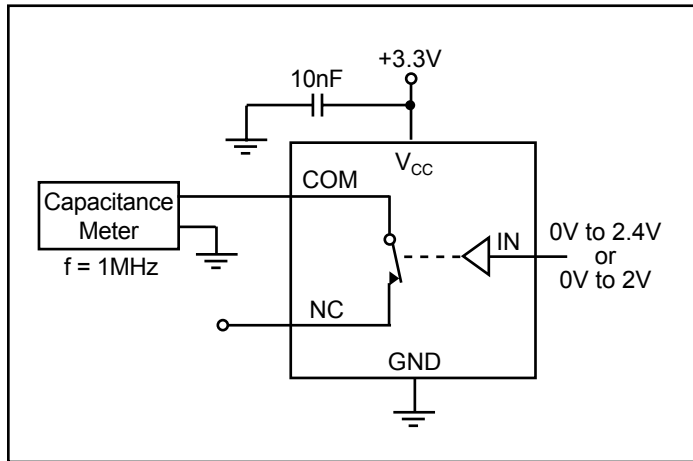
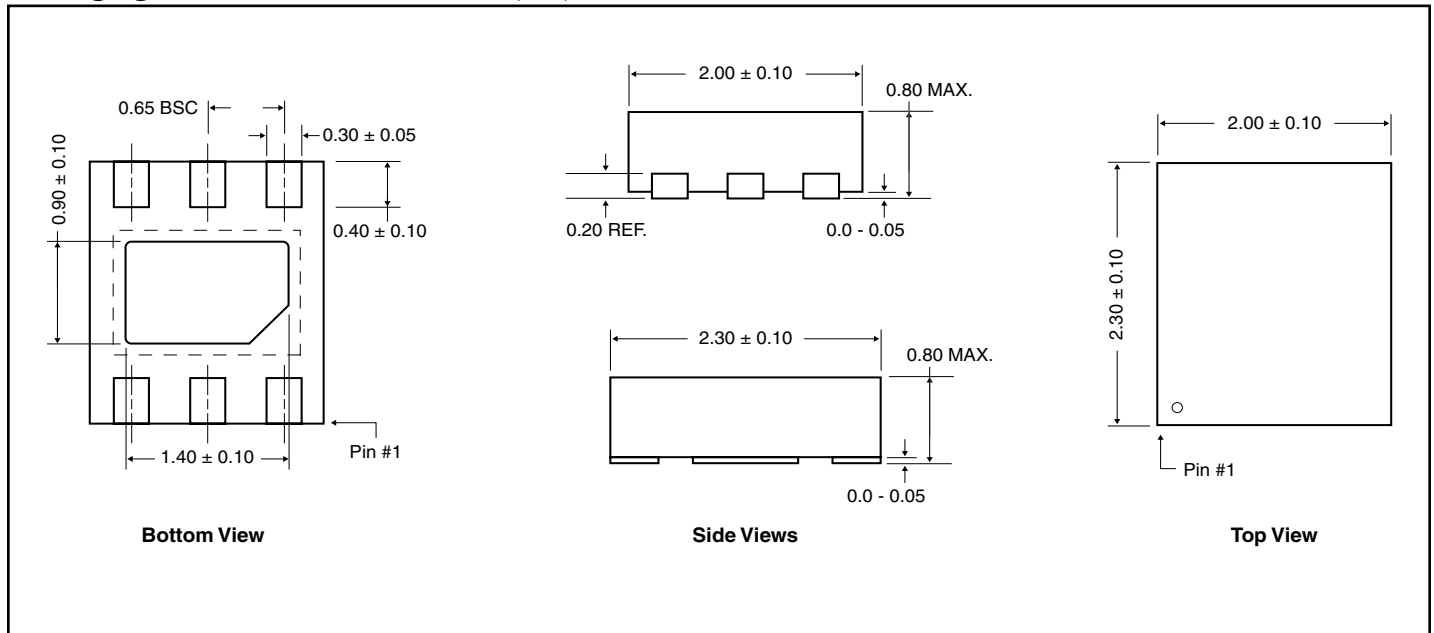
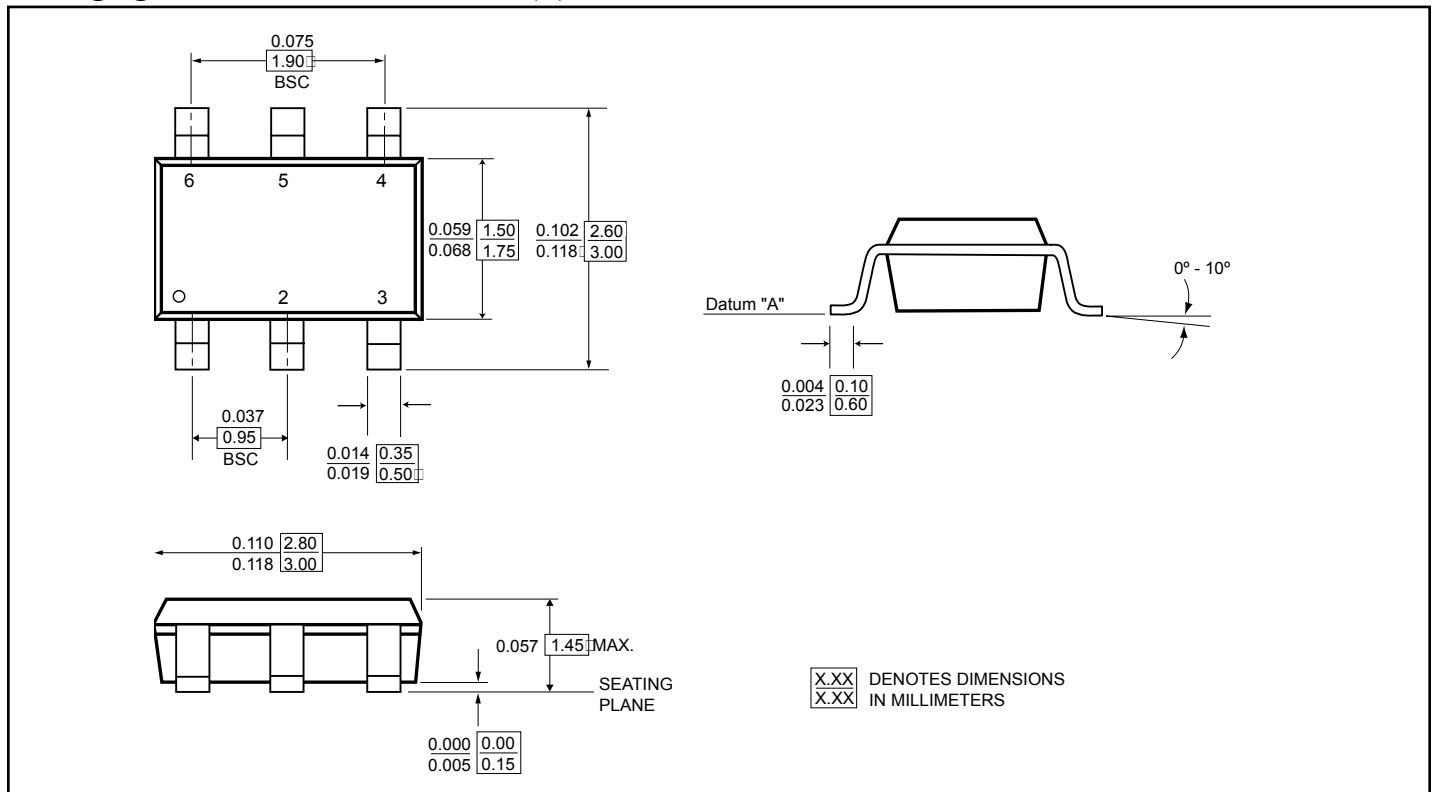


Figure 7. Channel-On Capacitance

Packaging Mechanical: 6-Pin TDFN (ZC)



Packaging Mechanical: 6-Pin SOT-23 (T)



Ordering Information

Order Code	Package Code	Package Type	Package Top Mark
PI3A4625TX	T	6-pin, Small Compact SOT-23	ZE
PI3A4625TEX	T	Pb-free & Green, 6-pin, Small Compact SOT-23	ZE
PI3A4625ZCEX	ZC	Pb-free & Green, 6-pin, Ultra Compact TDFN	ZE

Notes:

1. Thermal characteristics can be found on the company web site at <http://www.pericom.com/packaging/>
2. X = Tape/Reel