3.3V, High-Bandwidth, 40:10-Bit DDR Mux/Demux NanoSwitch™

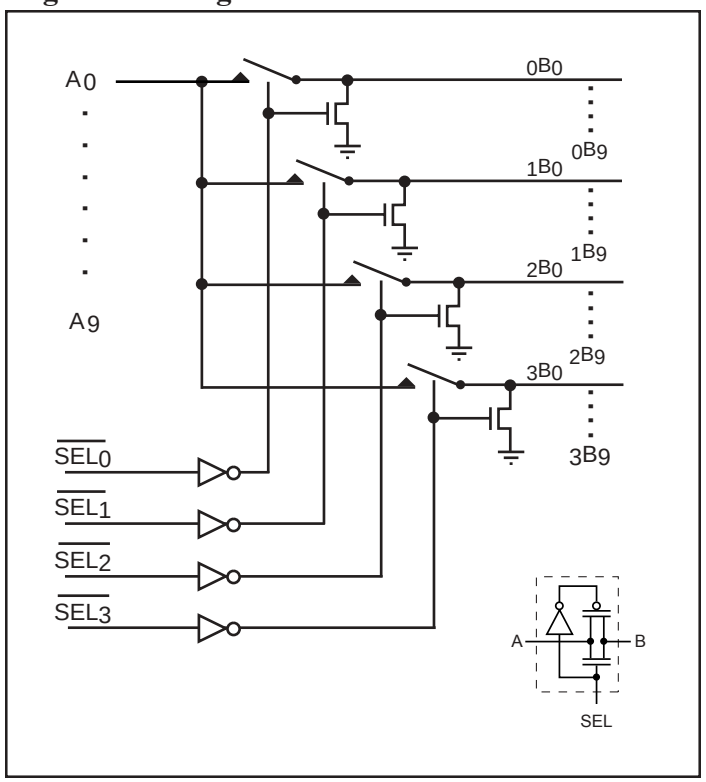
Product Features

- R_{ON} is 20 ohms max.
- Standard Operating Temperature: 0ºC to +70ºC
- Channel ON Capacitance: 15pF max.
- V_{CC} Operating Range: +3.0V to +3.6V
- Fast switching time: 3ns max.
- Package options include:
  - 64-ball Thin Fine Pitch Ball Grid Array (TFBGA)

Applications

- DDR DIMM bank switching

Logic Block Diagram

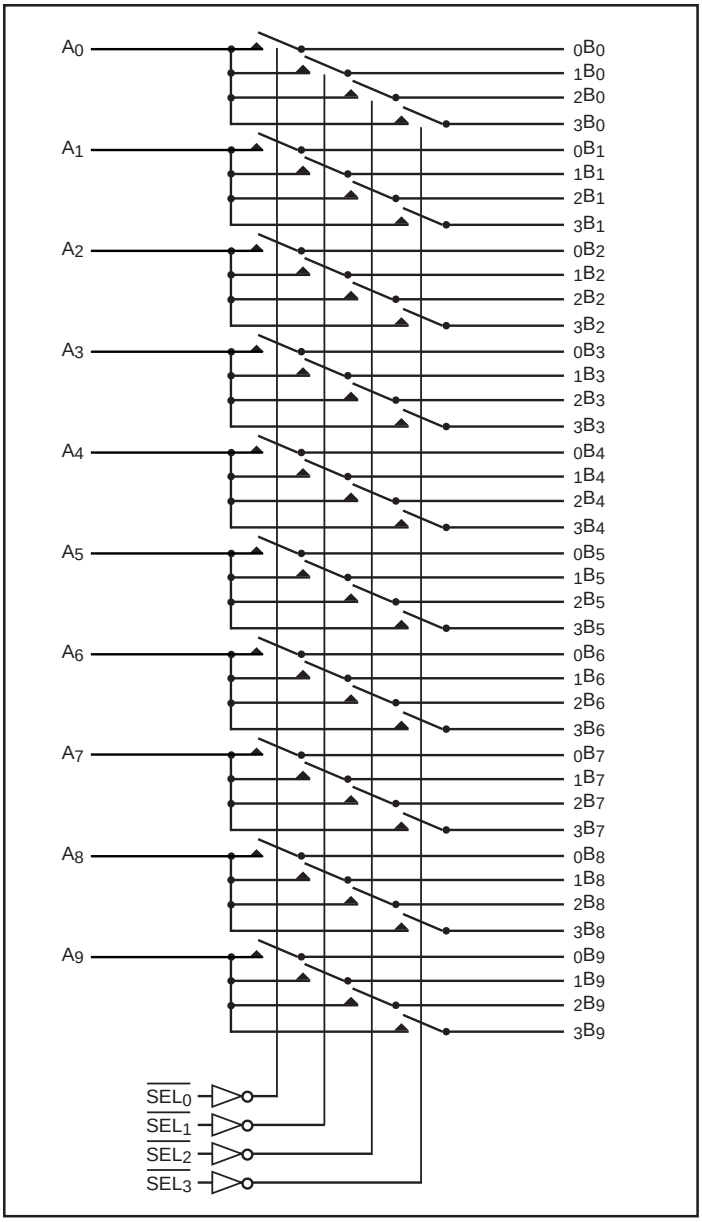


Product Description

Pericom Semiconductor's PI3B series of logic circuits are produced using the Company's advanced submicron CMOS technology, achieving industry-leading performance.

The PI3B4011 is a 3.3V, 10- to 40-bit demultiplexing/multiplexing bus switch. It is intended for multiple data or address muxing. Industry leading advantages include a propagation delay of 225ps, resulting from the 20-ohm channel resistance, and low I/O capacitance. The A-port multiplexes to one of four or all outputs allowing a complete bank of 10 bits to switch. The switch is bidirectional.

Expanded Block Diagram



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65ºC to +150ºC
Supply Voltage Range	–0.5V to +4.6V
DC Input Voltage	–0.5V to +4.6V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Product Pinout by Location on Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11
A	GND	$\overline{SEL_1}$	V_{DD}		$_1B_0$	$_2B_0$	$_3B_0$		$_2B_1$	$_3B_1$	$_0B_2$
B	$\overline{SEL_2}$	VDD	$\overline{SEL_0}$	GND	$_0B_0$	Ao	$_0B_1$	$_1B_1$	A_1	GND	$_1B_2$
C	V_{DD}	$\overline{SEL_3}$								A_2	$_2B_2$
D		GND								$_3B_2$	
E	$_2B_9$	$_3B_9$								$_0B_3$	$_1B_3$
F	$_1B_9$	A_9								A_3	$_2B_3$
G	$_0B_9$	$_3B_8$								GND	$_3B_3$
H		$_2B_8$								$_0B_4$	
J	$_1B_8$	A_8								A_4	$_1B_4$
K	$_0B_8$	GND	A_7	$_0B_7$	$_3B_6$	A_6	GND	$_3B_5$	A_5	$_3B_4$	$_2B_4$
L	$_3B_7$	$_2B_7$	$_1B_7$		$_2B_6$	$_1B_6$	$_0B_6$		$_2B_5$	$_1B_5$	$_0B_5$

Top View

Product Pin Description

Pin Name	Description
A_N	Demux Input Pins
$_NB_0$ - $_NB_9$	Mux Input Pins
$\overline{SEL_N}$	Bank Select Pins (Active LOW)
GND	Ground
V_{DD}	Power

Note: N = 0 through 3 for each set of 10 Bits

Truth Table

Function	$\overline{SEL_0}$	$\overline{SEL_1}$	$\overline{SEL_2}$	$\overline{SEL_3}$
Connect A_N to $_0B_N$	L	H	H	H
Connect A_N to $_1B_N$	H	L	H	H
Connect A_N to $_2B_N$	H	H	L	H
Connect A_N to $_3B_N$	H	H	H	L
$_0B_N$, $_1B_N$, $_2B_N$, $_3B_N$ = Pulldown, A_N = Hi-Z	H	H	H	H

DC Electrical Characteristics over Operating Range (T_A = 0°C to 70°C, V_{CC} = 3.3V ±5%)

Parameter	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH Level	1.6	–	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage	Guaranteed HIGH Level	–0.3	–	0.9	
V_{IK}	Clamp Diode Voltage	V_{CC} = Max., V_{IN} = –18mA	–	–0.7	–1.2	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}	–	–	±10	mA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND	–	–	±10	
R_{ON}	Switch On Resistance[3]	V_{CC} = Min., 0.8V ≤V_{IN} ≤2.5V, I_{IN} = –20mA	–	15	20	Ω
$R_{FLAT(ON)}$	On Resistance Flatness[4]	V_{CC} = Min., V_{IN}@0.8V and 1.7V I_{IN} = –20mA	–	1.0	–	
ΔR_{ON}	On Resistance match from center ports to any other port[4]	V_{CC} = Min., 0.8V ≤V_{IN} ≤2.5V, I_{IN} = –20mA	–	0.9	2	
R_{PD}	Pull-Down Resistance	V_{IN} = 0V to 2.5V	80	100	130	

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters	Description	Test Conditions	Typ.[4]	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	–	pF
$C_{OFF(A)}$	Port A Capacitance, Switch OFF		12.0	–	
$C_{ON(A/B)}$	A/B Capacitance, Switch ON		15.0	–	
$C_{OFF(B)}$	Port B Capacitance, Switch OFF		4.5	–	

Notes:
1. For min. or max. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between A and B pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A & B) pins.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
I_{CC}	Quiscent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	–	–	10	µA

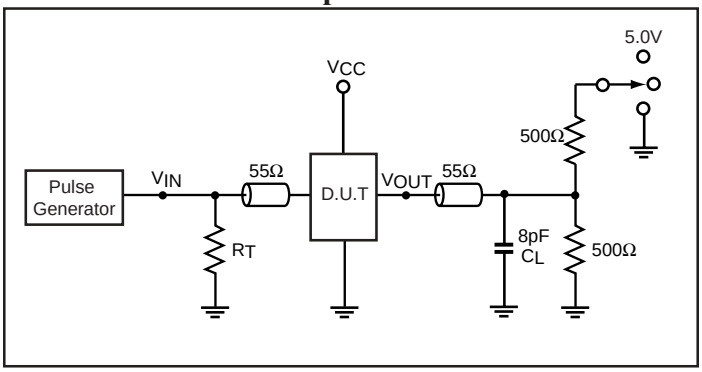
Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input (control inputs only); A and B pins do not contribute to I_{CC}.

Switching Characteristics (over operating range over recommended operating free-air temperature range).

Parameter	Description	Conditions	Com			Units
			Min.	Typ.	Max.	
t_{IY}	Propagation Delay[2,3] A_N to B_N w/Z_O = 50 ohms	–	–	0.225	–	ns
t_{SY}	Bus Select Time - $\overline{SEL_N}$ to A_N, B_N	–	0.5	–	3.0	
t_{PZL}	Bus Enable Time - $\overline{SEL_N}$ to A_N, B_N	–	0.5	–	3.0	
t_{PLZ}	Bus Disable Time - $\overline{SEL_N}$ to A_N, B_N	–	0.5	–	3.0	
$t_{SK(o)}$	Output skew between center ports (A_4 & A_5) to any other port[2]	–	–	0.1	0.2	
$t_{SK(p)}$	Skew between opposite transitions of the same output (It_{PHL} - $t_{PLH}I$)[2]	–	–	0.1	0.2	

Notes:
1. See test circuit and waveforms.
2. This parameter is guaranteed by design.
3. The bus switch contributes no propagational delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.225ns for 50pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Test Circuits for All Outputs[1]

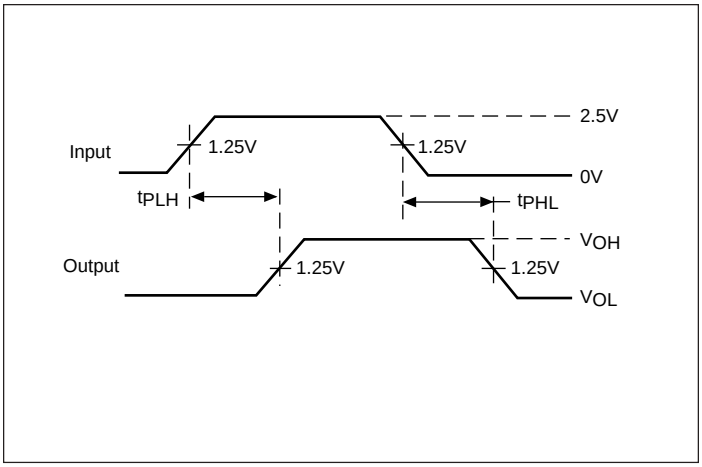


Switch Positions

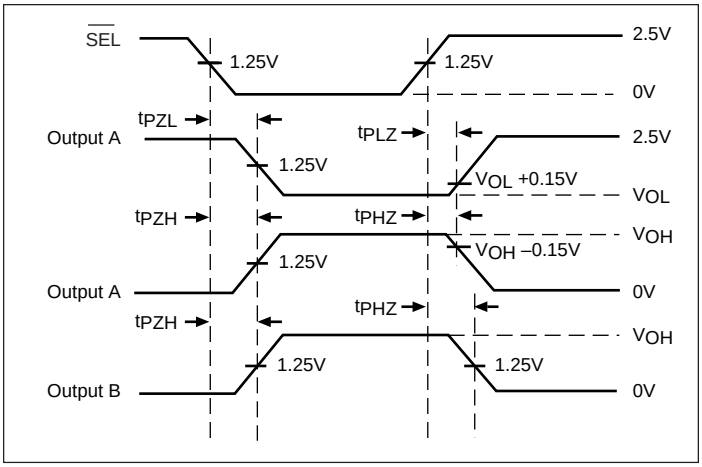
Test	Switch
Disable LOW, Enable LOW (output on A side)	5.0V
Disable HIGH, Enable HIGH (output on A side)	GND
Disable/Enable High (output on B side) & Prop Delay	Open

Notes:
1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, Z_O = 50Ω, t_R ≤ 2.5ns, t_F ≤ 2.5ns.
5. The outputs are measured one at a time with one transition per measurement.

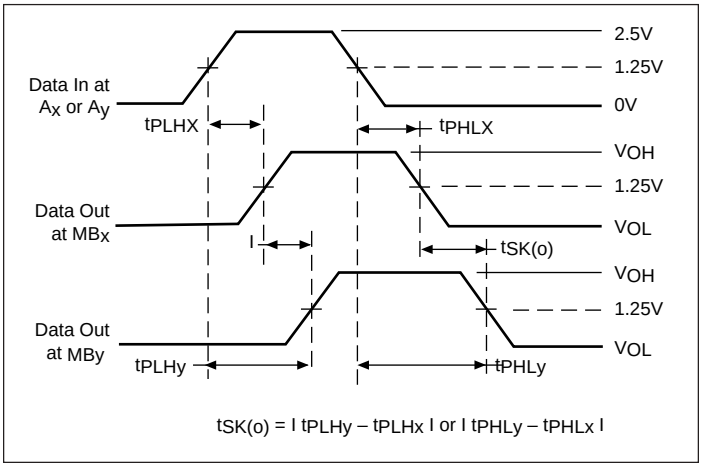
Switching Waveforms



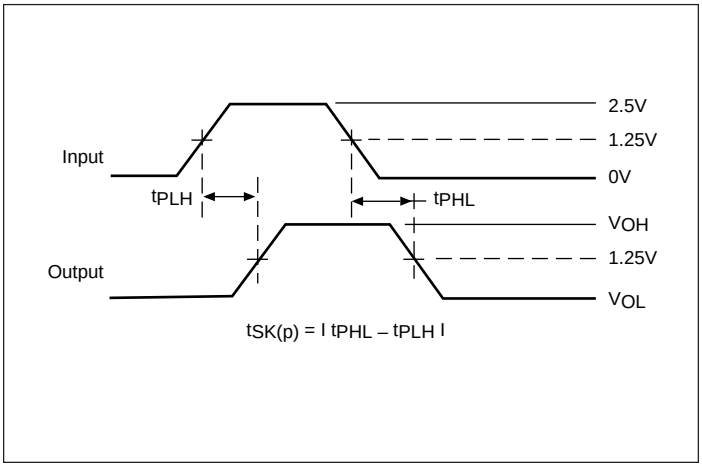
Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

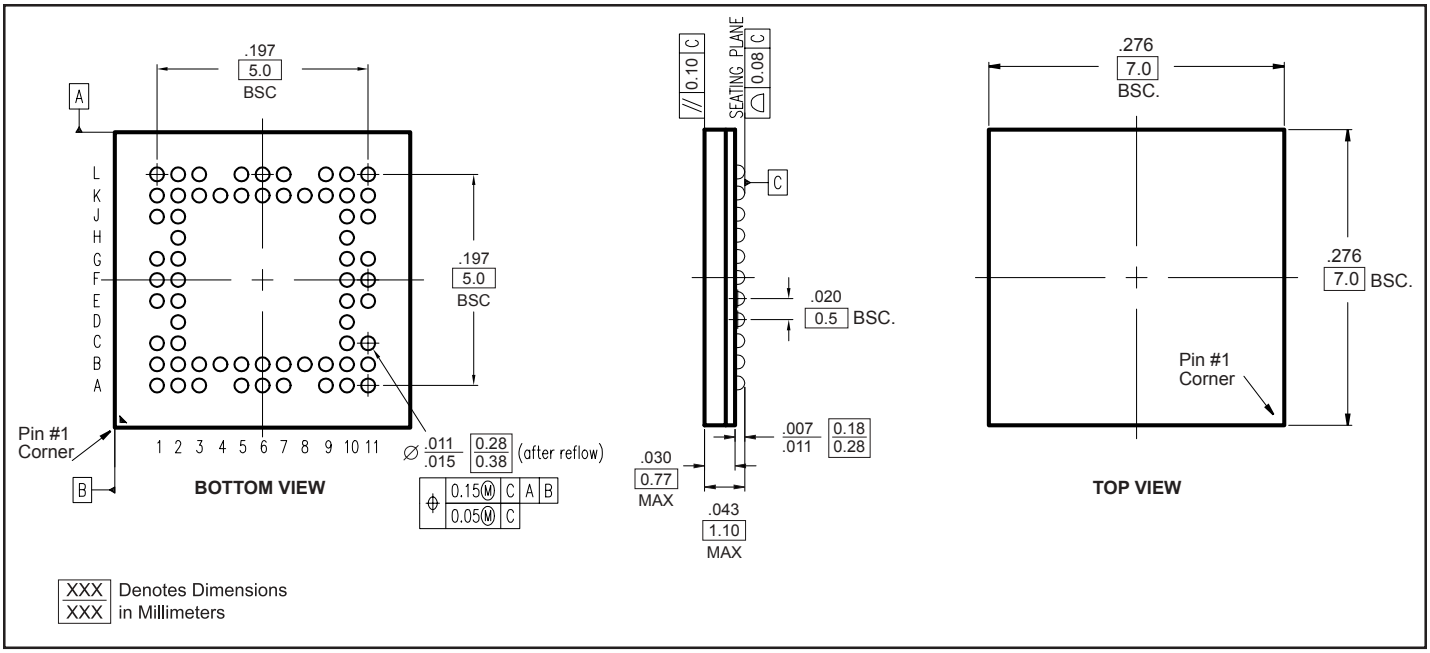


Output Skew - $t_{SK(o)}$



Pulse Skew - $t_{SK(p)}$

64-Pin TFBGA Package Drawing



Ordering Information

Part	Pin - Package
PI3B4011NC	64 - TFBGA

Applications Information

Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a + 3.3V supply, IN may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

Power-Supply Sequencing and Hot-Plug Information

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} and GND before applying signals to input/output or control pins.

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