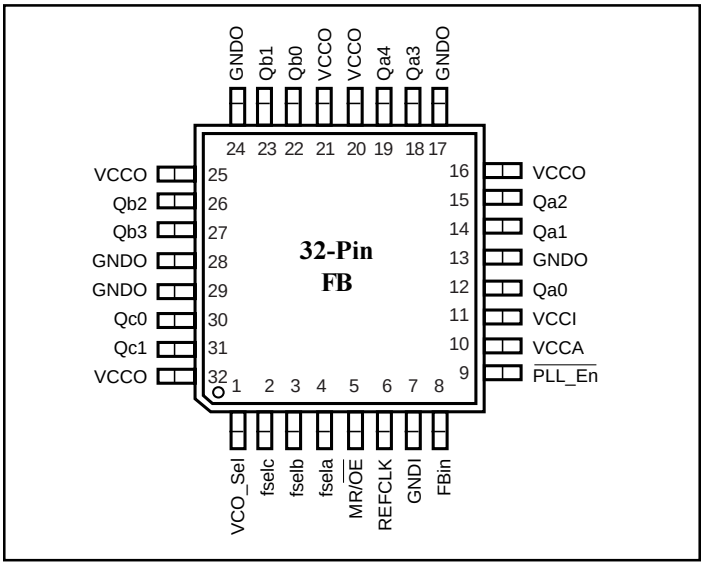
Low Voltage PLL Clock Driver

Features

- ±100ps Cycle-to-Cycle Jitter
- Fully Integrated PLL
- Output Frequency up to 180MHz
- High-Impedance Disabled Outputs
- Compatible with PowerPC, Intel, and High-Performance RISC Microprocessors
- Configurable Output Frequency
- 32-Pin LQFP Package (FB)

Pin Configuration



Description

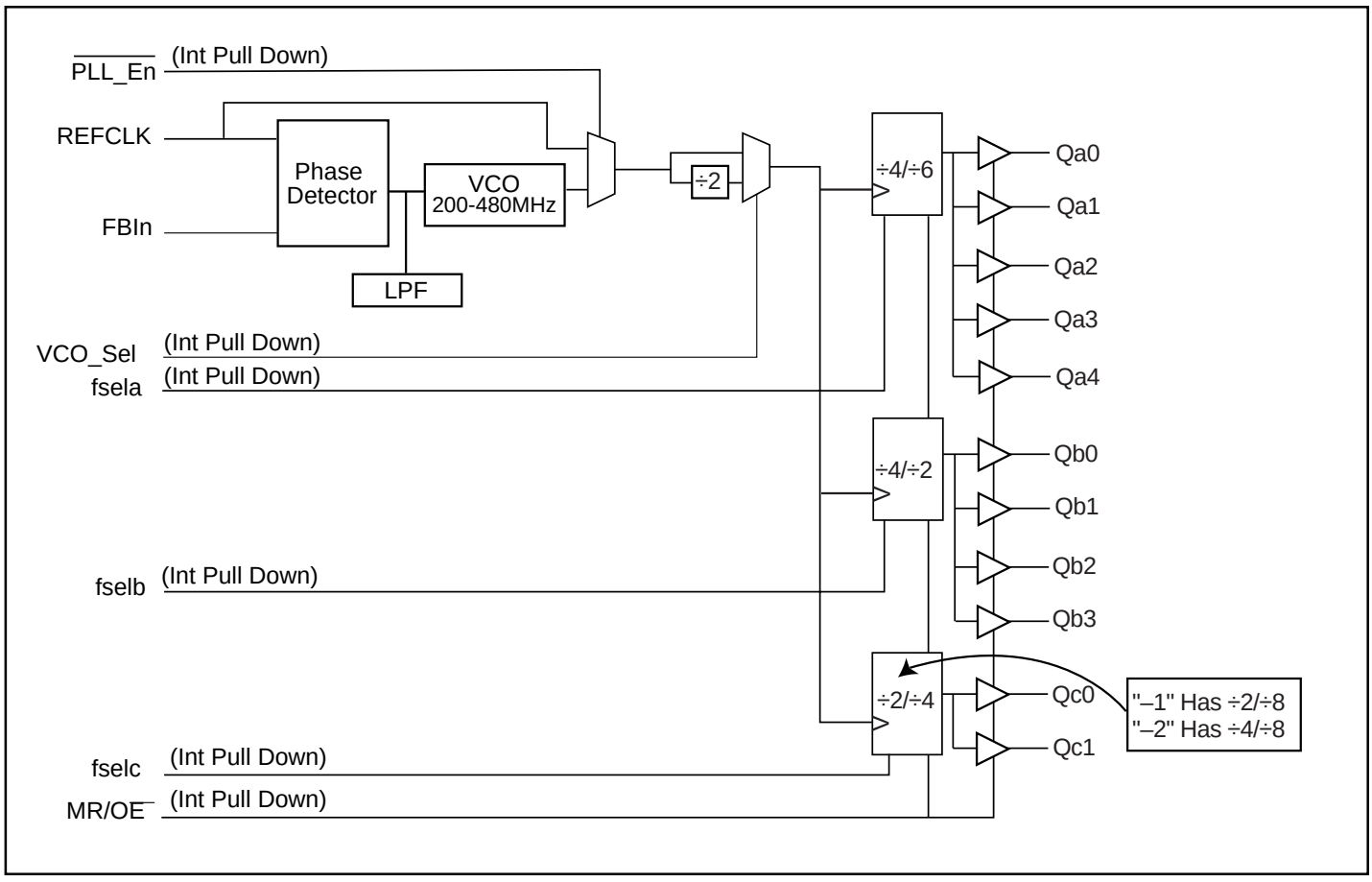
The PI6C2952 is a 3.3V compatible, PLL-based clock driver device targeted for high-performance clock applications. The device features a fully integrated PLL with no external components required. With output frequencies up to 180MHz and eleven low-skew outputs, the PI6C2952 is well suited for high-performance designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance.

The PI6C2952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs, and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1, and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins and other inputs are LVCMOS/LVTTL compatible inputs.

The PI6C2952 uses external feedback to the PLL. This features allows the device to be used as a "zero delay" buffer. Any of the eleven outputs can be used as feedback to the PLL. To optimize PLL stability and jitter performance,the VCO_Sel pin allows for the choice of two VCO ranges. For board level test, the MR/$\overline{OE}$ pin allows a user to force the outputs into high impedance. For system debug, the PI6C2952's PLL can be bypassed. When forced to a logic HIGH, the PL_LEN input routes the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers, it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The PI6C2952's outputs are LVCMOS which are optimally designed to drive terminated transmission lines. For applications using series-terminated transmission lines, each PI6C2952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most clock tree designs.

Block Diagram



Function Tables

fsela	Qan	fselb	Qbn	fselc	Qcn
0	÷4	0	÷4	0	÷2
1	÷6	1	÷2	1	÷4

Control Pin	Logic 'O'	Logic '1'
VCO_Sel	fVCO	fVCO/2
MR/$\overline{OE}$	Output Enable	High Z
$\overline{PLL\_En}$	Enable PLL	Disable PLL

Pin Name	Description
VCCA	PLL Power Supply
VCCO	Output Buffer Power Supply
VCCI	Internal Core Logic Power Supply
GNDI	Internal Ground
GNDO	Output Buffer Ground

Absolute Maximum Ratings*

Symbol	Parameters	Min.	Max.	Units
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	
I_{IN}	Input Current		±20	mA
T_{STOR}	Storage Temperature Range	–40	125	°C

*Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

DC Characteristics (T_A = 0°C to 70° C, V_{CC} = 3.3V± 5%)

Symbol	Conditions	Characteristic	Min.	Typ	Max.	Units
V_{IH}		Input HIGH Voltage	2.0		3.6	V
V_{IL}		Input LOW Voltage			0.8	
V_{OH}	I_{OH} = 20mA (Note1.)	Output HIGH Voltage	2.4			
V_{OL}	I_{OL} = 20mA (Note1.)	Output LOW Voltage			0.5	
I_{IN}	Note 2.	Input Current			±120	µA
C_{IN}		Input Capacitance		2.7	4.0	pF
C_{PD}		Power Dissipation Capacitance		25		
I_{CC}	Total ICC Static Current	Maximum Quiescent Supply Current			160	mA
I_{CCA}		PLL Supply Current		15	20	

Notes:
1. The PI6C2952 outputs can drive series- or parallel-terminated 50 ohms (or 50 ohms to $V_{CC}/2$) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up, pull–down resistors that affect input current.

PLL Input Reference Characteristics (T_A = 0°C to 70°C)

Symbol	Parameters	Min.	Max.	Units	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 3	Note 3	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

3. Maximum and minimum input reference is limited by the V_{CO} lock range and the feedback divider.

AC Characteristics (T_A = 0°C to 70°C, V_{CC} = 3.3V± 5%)

Symbol	Characteristics	Conditions	Min.	Typ.	Max.	Units
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.8 to 2.0V	0.10		1.0	ns
I_{PW}	Output Pulse Width (Note 4.)		$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +750	ps
t_{OS}	Output-to-Output Skew Excluding Qa0 (Note 4.) All Outputs All Outputs	Same Frequencies Same Frequencies Different Frequencies			350 450 550	ps
f_{VCO}	PLL VCO Lock Range Feedback = VCO/4 Feedback = VCO/6 Feedback = VCO/8 Feedback = VCO/12	VCO_Sel = 0 VCO_Sel = 0 VCO_Sel = 1 VCO_Sel = 1	200 200 200 200		480 480 480 480	MHz
f_{max}	Maximum Output Frequency Qc,Qb (÷2) Qa,Qb,Qc (÷4) Qa (÷6)	(Note 4.)	 180 120 80			
t_{pd}	REFCLK to FB_{IN} Delay	Notes 4 and 5.	–200	0	200	ps
t_{PLZ}, t_{PHZ}	Output Disable Time	50ohms to $V_{CC}/2$	2		8	ns
t_{PZL}, t_{PZH}	Output Enable Time	50ohms to $V_{CC}/2$	2		10	
tjitter	Cycle–to–Cycle Jitter (Peak–to–Peak)			±100		ps
t_{lock}	Maximum PLL Lock Time	Note 5.			10	ms
t_{JP}	Long term Period Jitter				TBD	ps

4. 50 ohms to $V_{CC}/2$.
5. t_{pd} is specified for 50 MHz input ref, the window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The t_{pd} does not include jitter.

Applications Information

Driving Transmission Lines

The PI6C2952 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10 ohms, the drivers can drive either parallel- or series-terminated transmission lines.

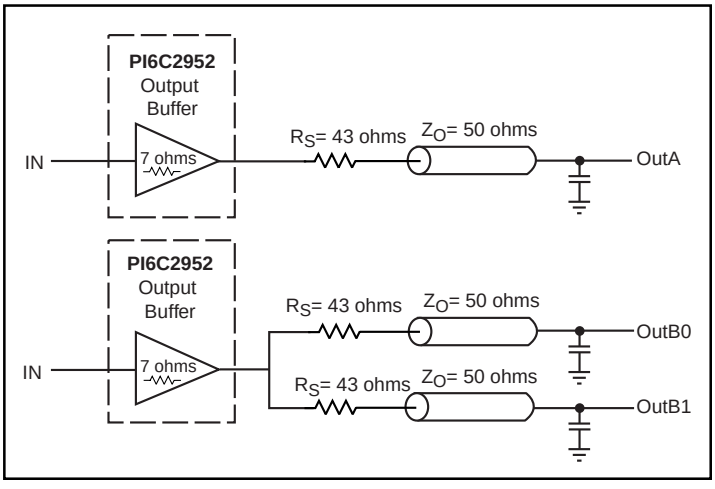


Figure 3. Single versus Dual Transmission Lines

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50ohm resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the PI6C2952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the PI6C2952 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the PI6C2952 output buffers is more than sufficient to drive 50-ohm transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the PI6C2952. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43ohm series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS\,(Zo / Rs + Ro + Zo) = 3.0\,(25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

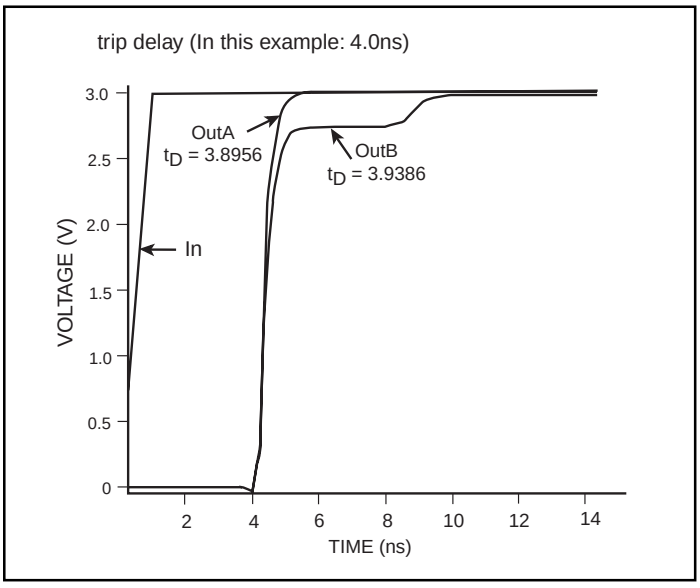


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

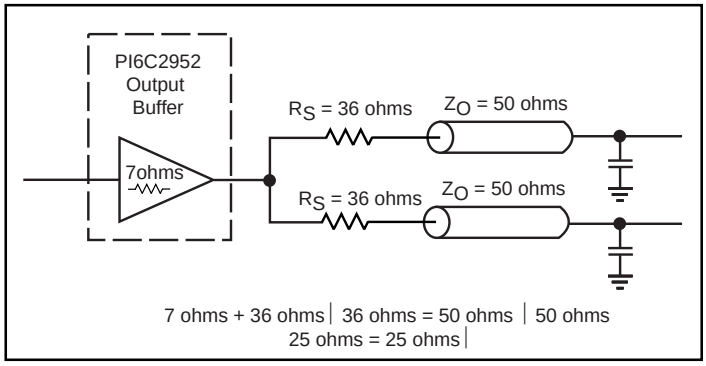


Figure 5. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

Power Supply Filtering

The PI6C2952 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The PI6C2952 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the PI6C2952.

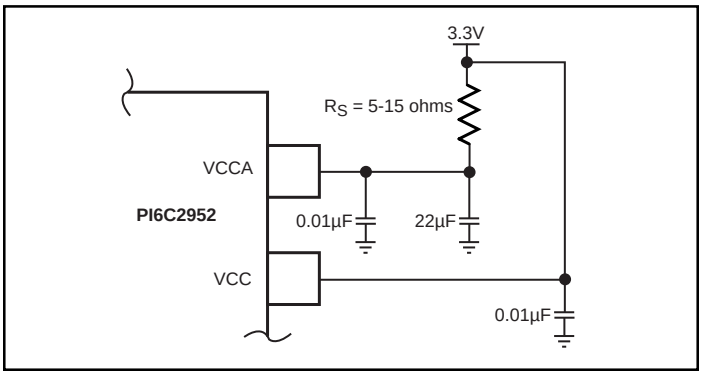
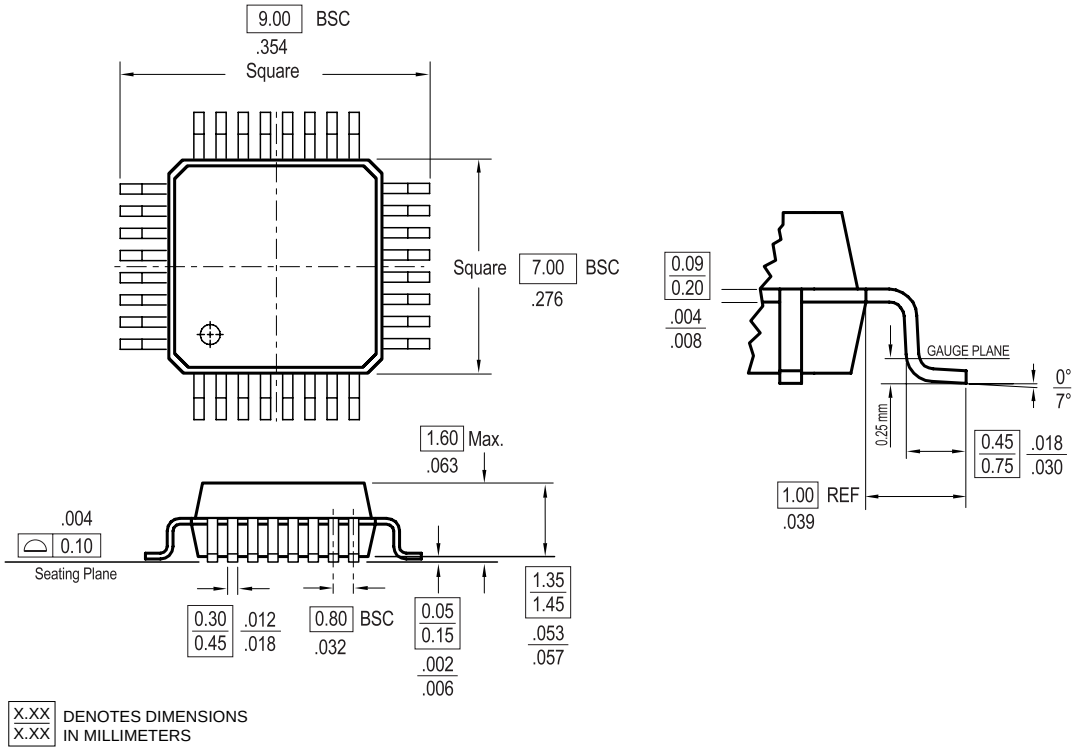


Figure 6. Power Supply Filter

32-Pin LQFP (FB) Package



Ordering Information

Part Number	Package	Operating Temperature
PI6C2952FB	32-LQFP	Commercial
PI6C2952-1FB		
PI6C2952-2FB		