PI6C2516

Phase-Locked Loop Clock Driver with 16 Clock Outputs

Product Features

- High Performance Phase-Locked Loop Clock Distribution for Synchronous DRAM, server and networking applications.
- Zero Input-to-Output delay: Distribute One Clock Input to four banks of four outputs, with separate output enables for each bank.
- Allow Clock Input to have Spread Spectrum modulation for EMI reduction. The clock outputs track the Clock Input modulation.
- Maximum clock frequency of 150 MHz.
- Low jitter: Cycle-to-Cycle jitter ±100ps max
- Operates at 3.3V V_{CC}
- Available Packaging:
  – 48-pin TSSOP (Thin Shrink Small Outline) (A)

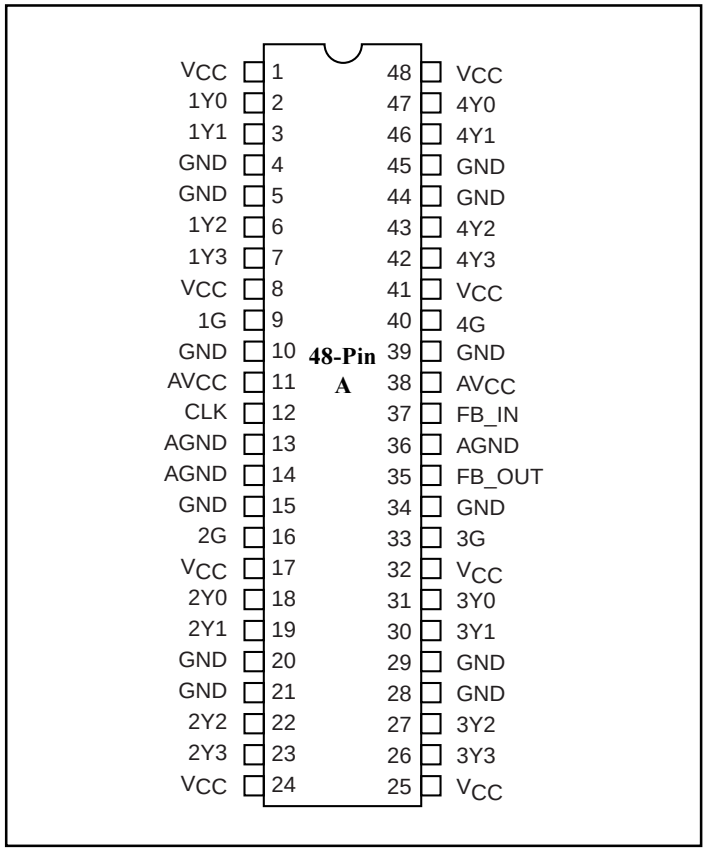
Description

The PI6C2516 family is a low-skew, low jitter, phase-locked loop (PLL) clock driver, distributing high-frequency clock signals for SDRAM, server and networking applications. By connecting the feedback FB_OUT output to the feedback FB_IN input, the propagation delay from the CLK input to any clock output will be nearly zero. This zero-delay feature allows the CLK input clock to be distributed, providing 4 banks of four outputs.

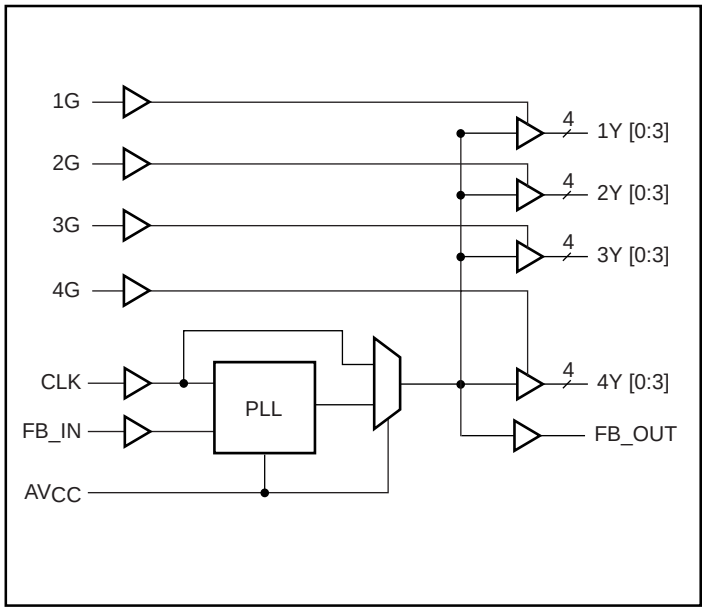
For test purposes, the PLL can be bypassed by strapping the AV_{CC} to ground.

The PI6C2516 family has the same pinout as the TI CDC2516, with the added feature of allowing Spread Spectrum clock input.

Pin Description



Block Diagram



Pin Functions

Pin Name	Pin Number	Type	Description
CLK	12	I	Clock input. CLK allows spread spectrum.
FB_IN	37	I	Feedback input. FB_IN provides the feedback signal to the internal PLL. CLK↑ and FB_IN↑ are synchronized so that there is normally zero phase error between CLK and FB_IN.
1G	9	I	Output bank enable. When 1G is LOW, outputs 1Y[0:3] are disabled to a logic low state. When 1G is HIGH, all outputs 1Y[0:3] are enabled and switched at the same frequency as CLK.
2G	16	I	Output bank enable. When 2G is LOW, outputs 2Y[0:3] are disabled to a logic low state. When 2G is HIGH, all outputs 2Y[0:3] are enabled and switched at the same frequency as CLK.
3G	33	I	Output bank enable. When 3G is LOW, outputs 3Y[0:3] are disabled to a logic low state. When 3G is HIGH, all outputs 3Y[0:3] are enabled and switched at the same frequency as CLK.
4G	40	I	Output bank enable. When 4G is LOW, outputs 4Y[0:3] are disabled to a logic low state. When 4G is HIGH, all outputs 4Y[0:3] are enabled and switched at the same frequency as CLK.
FB_OUT	35	O	Feedback output. FB_OUT is dedicated for external feedback. FB_OUT has an embedded 25Ω series-damping resistor of the same value as the clock outputs.
1Y[0:3]	2,3,6,7	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded 25Ω series-damping resistor of the same value as the clock outputs.
2Y[0:3]	18,19,22,23	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded 25Ω series-damping resistor of the same value as the clock outputs.
3Y[0:3]	26,27,30,31	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded 25Ω series-damping resistor of the same value as the clock outputs.
4Y[0:3]	42,43,46,47	O	Clock outputs. These outputs provide low-skew copies of CLK_IN. Each output has an embedded 25Ω series-damping resistor of the same value as the clock outputs.
AV_{CC}	11,38	Power	Analog power supply. AV_{CC} can be also used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	13,14,36	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	1,8,17,24,25,32,41,48	Power	Power supply
GND	4,5,10,15,20,21,28,29, 34,39,44,45	Ground	Ground

Absolute Maximum Ratings (Over Operating Free-Air Temperature Range, unless otherwise noted)†

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply voltage range	– 0.5	4.6	V
V_I	Input voltage range(1)	– 0.5	6.5	
V_O	Voltage range applied to any output(1,2)	– 0.5	V_{CC} + 0.5	
V_{IK}	Input Clamp Current	–50		mA
I_O_DC	Continuous output current (V_O = 0 or V_{CC})		±50	
I_O_DC	Continuous output through V_{CC} or ground		±100	
Power	Maximum power dissipation at T_A= 55°C in still air(3)		0.85	W
T_{STG}	Storage temperature	– 65	150	°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect reliability.

Notes:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6V maximum.
3. Maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions(4)

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply voltage	3.0	3.6	V
V_{IH}	High level input voltage	2.0		
V_{IL}	Low level input voltage		0.8	
V_I	Input voltage	0.0	V_{CC}	
T_A	Operating free-air temperature	0	70	°C
I_{OH}	High level output current		–12	mA
I_{OL}	Low level output current		12	

Note

4. Unused inputs must be held high or low to prevent them from floating.

Function Table

xG	CLK	xY [0:3]	FB_OUT
L	L	L	L
L	H	L	H
H	L	L	L
H	H	H	H

Note:
x is from 1 to 4

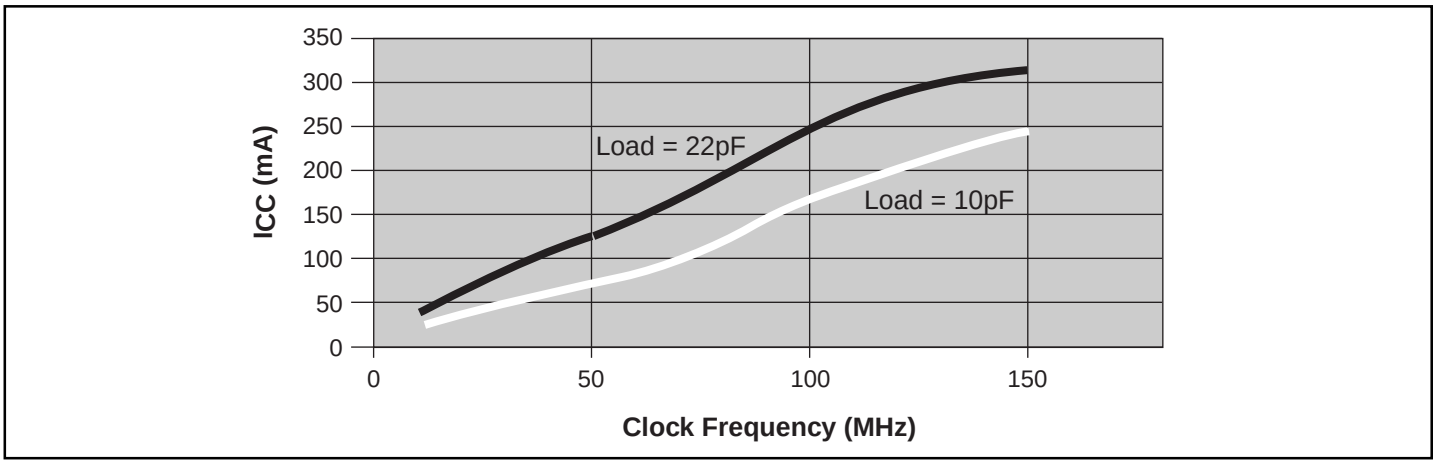
Electrical Characteristics (Over Recommended Operating Free-air Temperature Range)

Symbol	Test Condition	V_{CC}	Min.	Typ.	Max.	Units
V_{IK}, Input clamp voltage	Input current at –18mA	3V		–0.79	–1.2	V
V_{OH}	I_{OH} = –100µA	Min. to Max.	V_{CC} –0.2	2.99		
	I_{OH} = –12mA	3V	2.1	2.66		
	I_{OH} = –6mA		2.4	2.83		
V_{OL}	I_{OL} = 100µA	Min. to Max.		0.01	0.2	
	I_{OL} = 12mA	3V		0.3	0.8	
	I_{OL} = 6mA			0.15	0.55	
I_I, Input current	Clock input voltage = V_{CC} or GND	3.6V			±5	µA
Analog supply current, I_{CC}	Clock input voltage = V_{CC} or GND				12	mA
C_I	Input voltage = V_{CC} or GND	3.3V		4.0	4.0	pF
C_O	Output voltage = V_{CC} or GND			6.0		
ΔI_{CC}	One input @ V_{CC} –0.6V, other inputs @V_{CC} or GND	3.3V to 3.6V		5.0	500	µA

Timing Requirements (Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature)

Symbol	Parameter	Min.	Max.	Units
F_{CLKOP}	Operator clock frequency (1)	25	150	MHz
t_{CLKAPP}	Application clock frequency(2,4)	6	133	
$t_{STABLILIZATION}$	Stabilization time after power up(3)	–	1	ms
D_{CYI}	Input clock duty cycle	40	60	%

Notes:
1. Operating Clock Frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters (used for low-speed system debug).
2. Application Clock Frequency indicates a range over which the PLL must meet all of the timing parameters.
3. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable.
4. Frequency and loading condition should not exceed 0.85 watt power dissipation (package limitation). Please refer to Graph 1.



Graph 1. Dynamic Current vs. Clock Frequency (V_{CC} = 3.6V, T_A = 25°C)

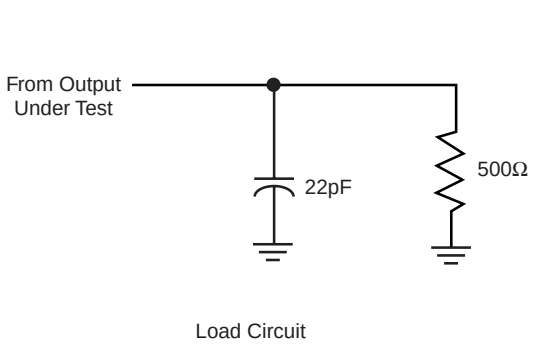
Switching Characteristics

(Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature, C_L = 22pF) (1,3)

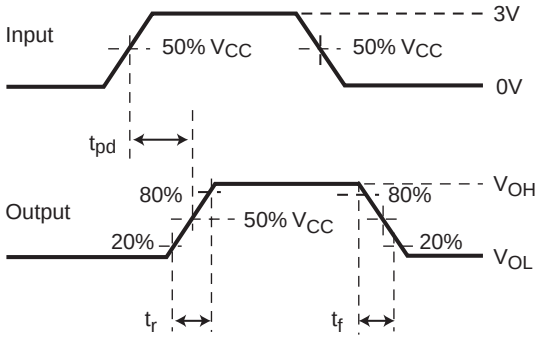
Parameter	From (Input)	To (Output)	V_{CC} = 3.3V ± 0.165V			V_{CC} = 3.3V ± 0.3V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{phase} error	CLKIN↑ = 100MHz	FBIN↑				–150		+170	ps
$t_{sk(O)}$(2)	Any Y or FBOUT	Any Y or FBOUT						200	
$Jitter_{(pk-pk)}$	F(CLKIN > 66MHz)					–100		100	
Duty cycle	F(CLKIN ≤ 66MHz)					45		55	%
	F(CLKIN > 66MHz)					45		55	
t_r	CLKIN = 50 to 150MHz from 20% to 80%			1.3	2.1	0.7		2.1	ns
t_f				1.7	2.5	1.2		2.5	

Notes:
1. These parameters are not production tested.
2. The $t_{sk(O)}$ specification is only valid for equal loading of all outputs.
3. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

Parameter Measurement Information



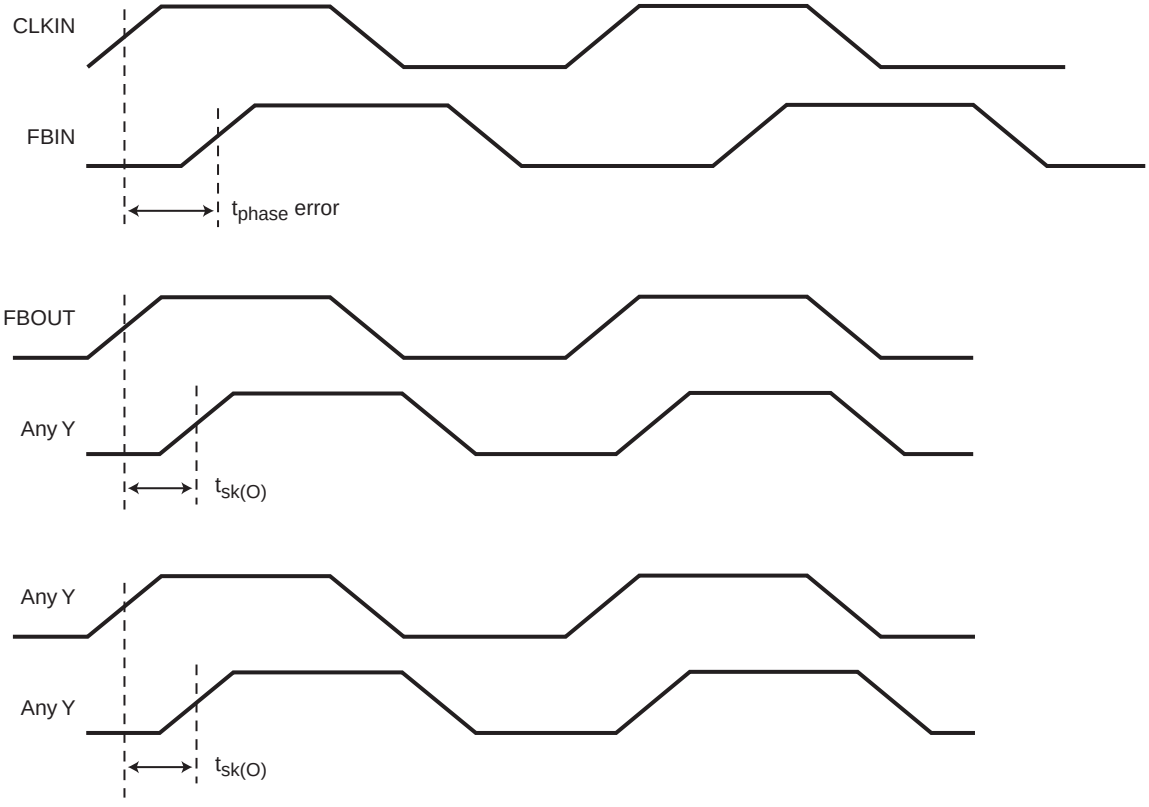
Load Circuit



Voltage Waveforms
Propagation Delay times

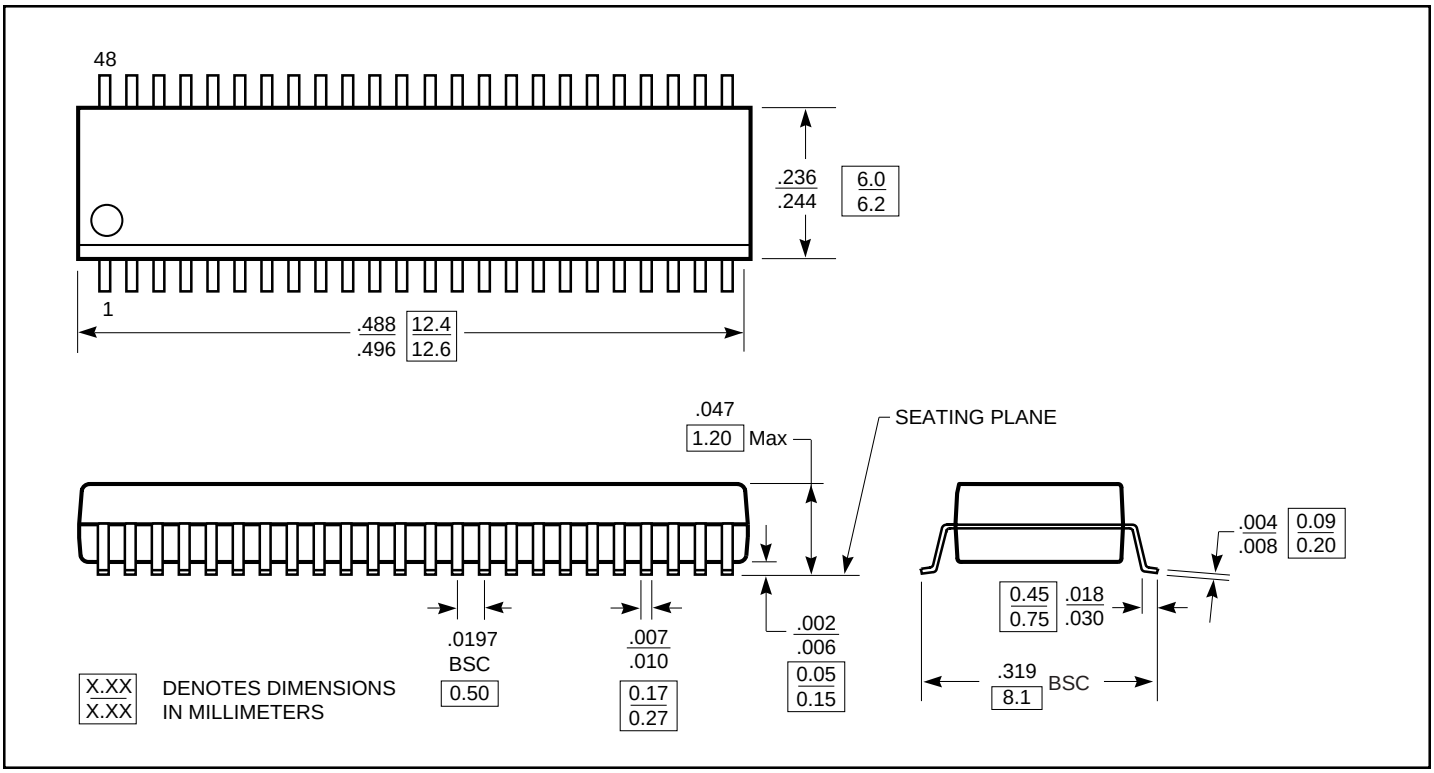
Notes:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:
   CLKIN ≤ 100MHz, Z_O = 50 ohms, t_r ≤ 1.2ns, t_f ≤ 1.2ns.
3. The outputs are measured one at a time with one transition per measurement.



Phase Error and Skew Calculations

48-pin Thin Shrink Small-Outline Package (A)



Ordering Information

Part Number	Ordering P/N	Package
PI6C2516	PI6C2516A	48-pin TSSOP