PI6C9910

Zero-Delay Clock Buffer

Features

- Zero input to output delay
- Eight clock copies from one clock input
- 15 - 80 MHz output operation
- Fifty percent duty cycle
- Low skew (< 250ps typ.)
- V_{CC} = 5.0V +/- 10%, T_A = 0° to 70°
- Low jitter (< 250 ps cycle to cycle), < 60ps RMS
- Low noise unbalanced drive outputs (PI6C9910-5)
- Low noise balanced drive outputs (PI6C9910A)
- Packages available:
  – 24-pin 300 mil wide SOIC (S)
- Compatible with Cypress CY7B9910-5

Test Mode

In normal operation the TEST pin is tied to ground. For testing purposes it can have a removable jumper to ground or a 100Ω pull-down resistor. When the TEST pin is driven HIGH, the VCO output is disconnected, and all eight outputs (Q0-Q7) are directly driven from the REF input.

Description

The PI6C9910 is a low-skew clock driver designed to simplify clock distribution in systems requiring near synchronous clocks. A typical application is in SDRAM modules. Each of the eight outputs (Q0-Q7) can drive individual 50Ω transmission lines with minimal distortion or skew, and full 5V swing.

An on-chip phase-locked loop (PLL) synchronizes the feedback (FB) to the reference (REF) input, achieving "zero-delay" buffered outputs.

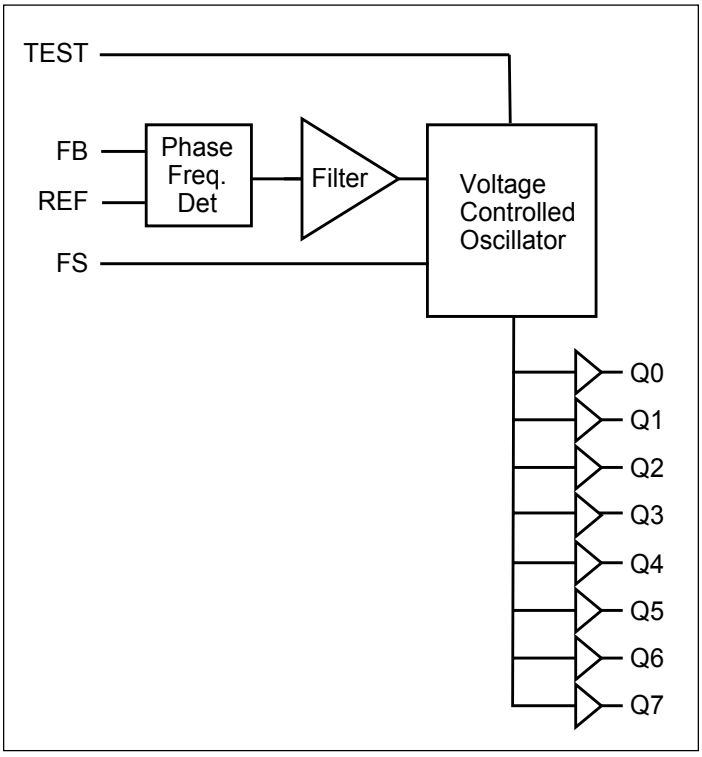
Inserting an external counter between any of the Qx outputs and the FB pin allows for generation of eight synchronous clock copies whose frequency is a multiple of a lower frequency REF input.

The voltage-controlled oscillator (VCO) frequency is determined by the filtered ouput coming from the Phase/Frequency Detector. The frequency select (FS) input sets the VCO operating range.

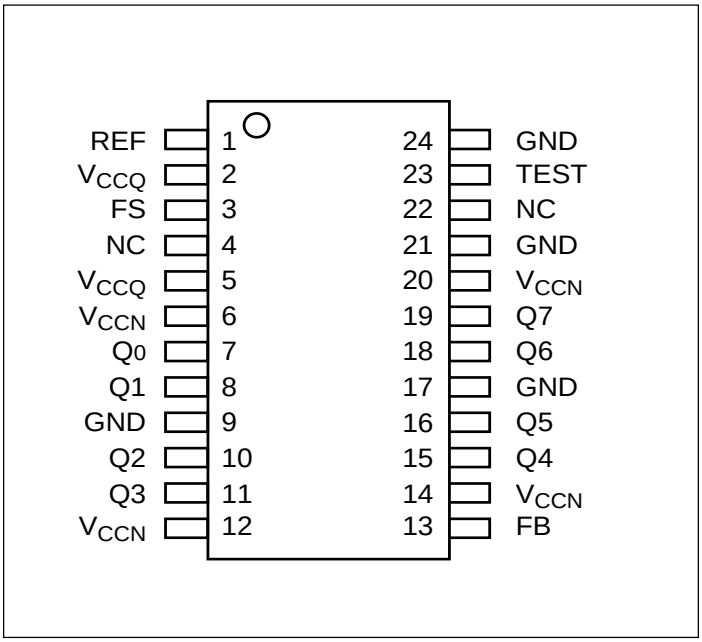
PI6C9910-5 has unbalanced output drivers (TTL), and is fully compatible with the Cypress CY7B9910-5. The PI6C9910A features balanced-drive outputs (CMOS) for improved rise/fall time symmetry.

The FS and TEST inputs have internal pull-up resistors.

Block Diagram



Pinout



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
Output Current into Outputs (LOW)	64mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200mA

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Pin Description

Pin Name	I/O	Functional Description
REF	I	Reference Frequency Input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of eight outputs).
FS	I	Two-level frequency range select. See Table 1. Internal Pull-up.
TEST	I	Two-level select. See Test Mode Section. Internal Pull-up
Q[0-7]	O	Clock Outputs.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Electrical Characteristics Over Operating Range[1]

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage (PI6C9910-5)	V_{CC} = Min., I_{OH} = -16mA	2.4	—	V
V_{OL}	Output LOW Voltage (PI6C9910-5)	V_{CC} = Min., I_{OL} = 46mA	—	0.45	
V_{OH}	Output HIGH Voltage (PI6C9910A)	V_{CC} = Min., I_{OH} = -24mA	2.4	—	
V_{OL}	Output LOW Voltage (PI6C9910A)	V_{CC} = Min., I_{OL} = 24mA	—	0.40	
I_{IH}	Input HIGH Leakage Current (REF, Test, FS, and FB inputs only)	V_{CC} = Max., V_{IN} = Max.	—	10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	–10	—	
	Input LOW Leakage Current (Test and FS inputs only)		-500	—	
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND (25°C only)	—	–250	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Inputs Selects Open	—	85	
I_{CCN}	Output Buffer Current per Output Pair	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0mA Inputs Selects Open, f_{MAX}	—	14	
PD	Power Dissipation per Output Pair	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0mA Inputs Selects Open, f_{MAX}	—	78	mW

Notes:
1. These inputs are normally wired to V_{CC}, GND. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.
2. Tested one output at a time, output shorted for less than one second, less than l0% duty cycle. Room temperature only.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance REF and FB	T_A = 25C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Unbalanced Output Drive AC Test Load and Waveform

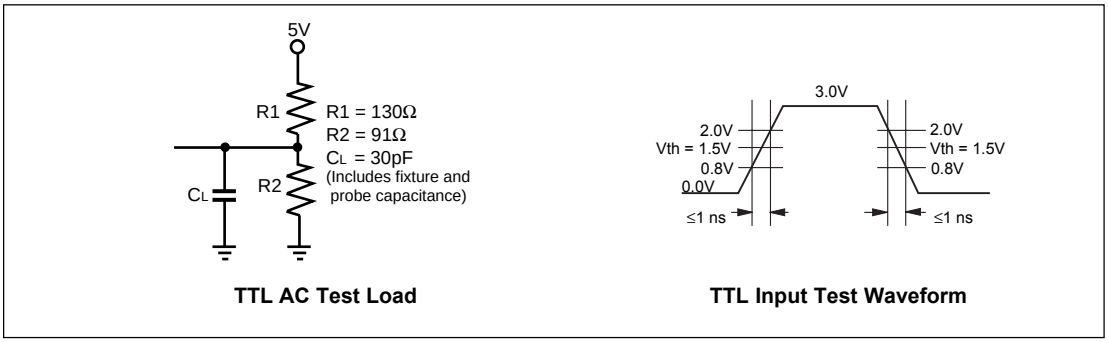
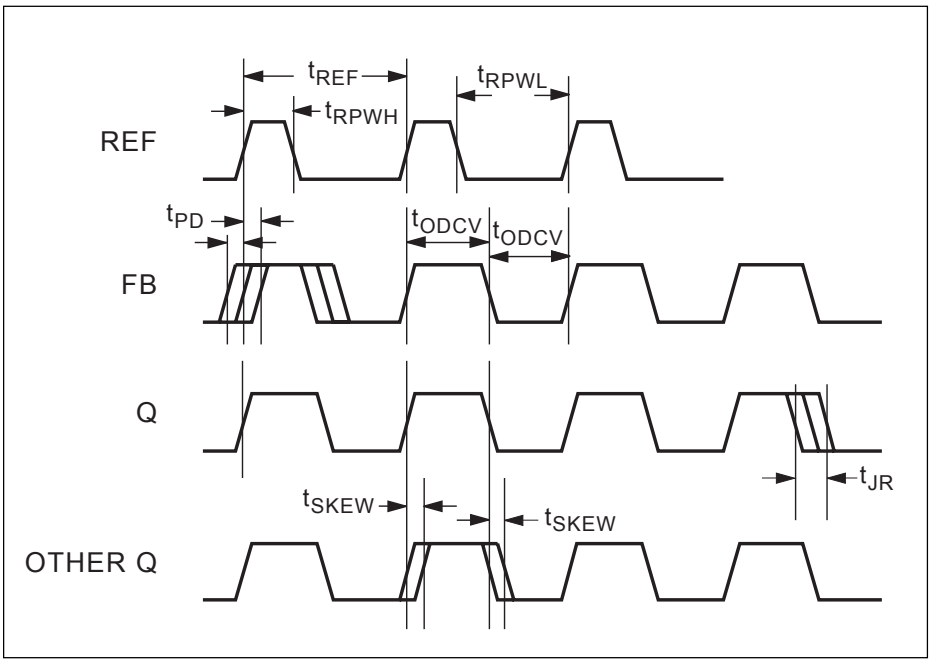


Table 1. Frequency Range Select

FS	f_{NOM} (MHz)	
	Minimum	Maximum
LOW	15	35
HIGH	25	80

AC Timing Diagram



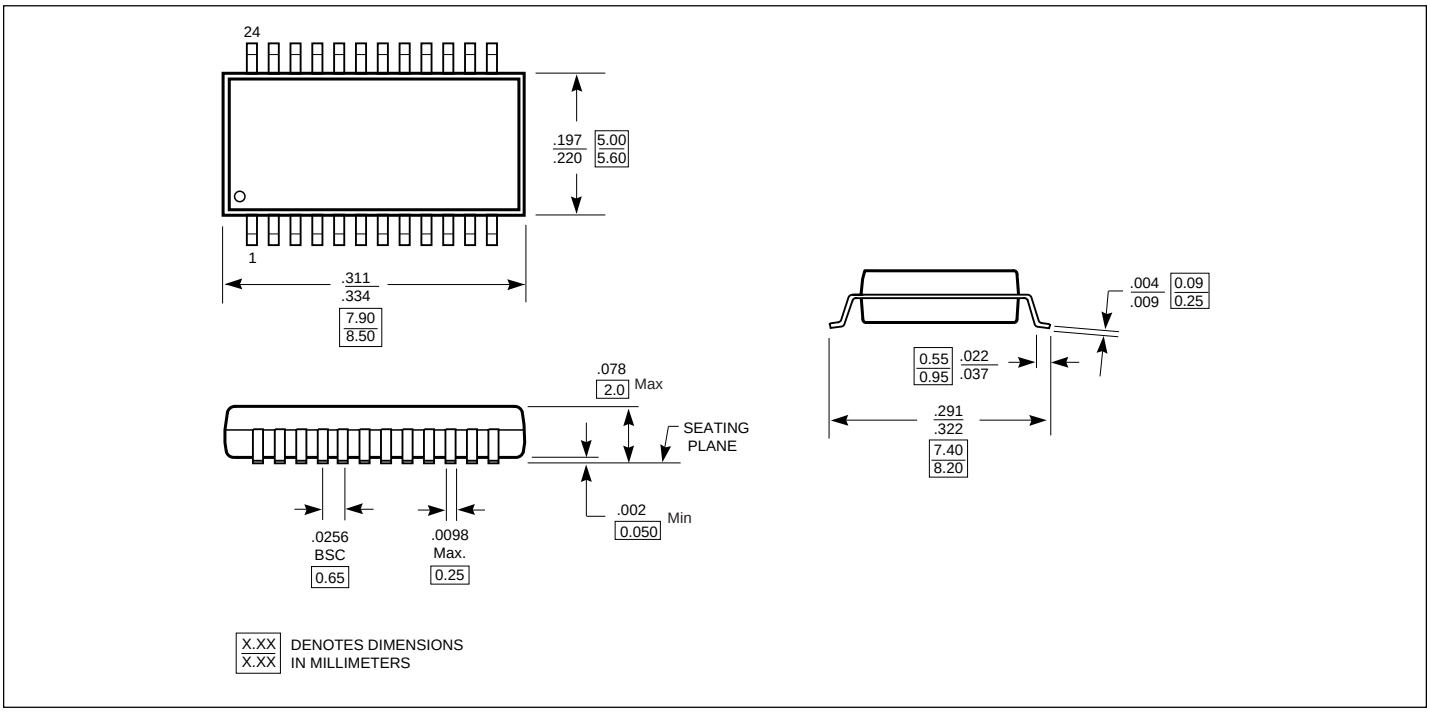
Switching Characteristics Over Operating Range[1]

Symbol	Description		Min.	Typ.	Max.	Units
f_{NOM}	Operation Clock Frequency in MHz	FS = LOW	15	–	35	MHz
		FS = HIGH	25	–	80	
t_{RPWH}	REF Pulsewidth HIGH		5.0	–	–	ns
t_{RPWL}	REF Pulsewidth LOW		5.0	–	–	
t_{SKEW}	Zero Output Skew (All Outputs)[2,3]		–	0.25	0.5	
t_{DEV}	Device-to-Device Skew[4,5]		–	–	1.0	
t_{PD}	Propagation Delay, REF Rise to FB Rise		-0.5	0.0	+0.5	
t_{ODCV}	Output Duty Cycle Variation[6]		-1.0	0.0	+1.0	
t_{ORISE}	Output Rise Time[7,8]		0.15	1.0	1.5	
t_{OFALL}	Output Fall Time[7,8]		0.15	1.0	1.5	
t_{LOCK}	PLL Lock Time[9]		–	–	0.5	ms
t_{JR}	Output Jitter	Cycle-to-Cycle[5]	–	–	250	ps
		RMS[5]	–	–	60	

Notes:

1. Test measurement levels for the PI6C9910-5 are TTL levels (1.5V to 1.5V). Test conditions assume signal transition times of 2ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
2. Skew is defined as the time between the earliest and the latest output transition among all outputs with AC Test Load.
3. t_{SKEW} is defined as the skew between outputs.
4. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.).
5. Tested initially and after any design or process changes that may affect these parameters.
6. t_{ODCV} is the deviation of the output from a 50% duty cycle.
7. Specified with outputs loaded with AC Test Load (30pF).
8. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V.
9. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Package Mechanical: 209-Mil 24-Pin SSOP (S)



Ordering Information

Part Number	Package
PI6C9910AS	300-Mil 24-pin SOIC Package S24
PI6C9910-5S	300-Mil 24-pin SOIC Package S24