PI6C102

Precision Clock Synthesizer for Mobile PCs

Features

- Two copies of CPU clock with V_{DD} of 2.5V ±5%
- 100 MHz or 66.6 MHz operation
- Six copies of PCI clock, (synchronous with CPU clock) 3.3V
- One copy of Ref. Clock @ 14.31818 MHz (3.3V_{TTL})
- Low cost 14.31818 MHz crystal oscillator input
- Power management control
- Isolated core V_{DD}, V_{SS} pins for noise reduction
- 28-pin SSOP package (H)

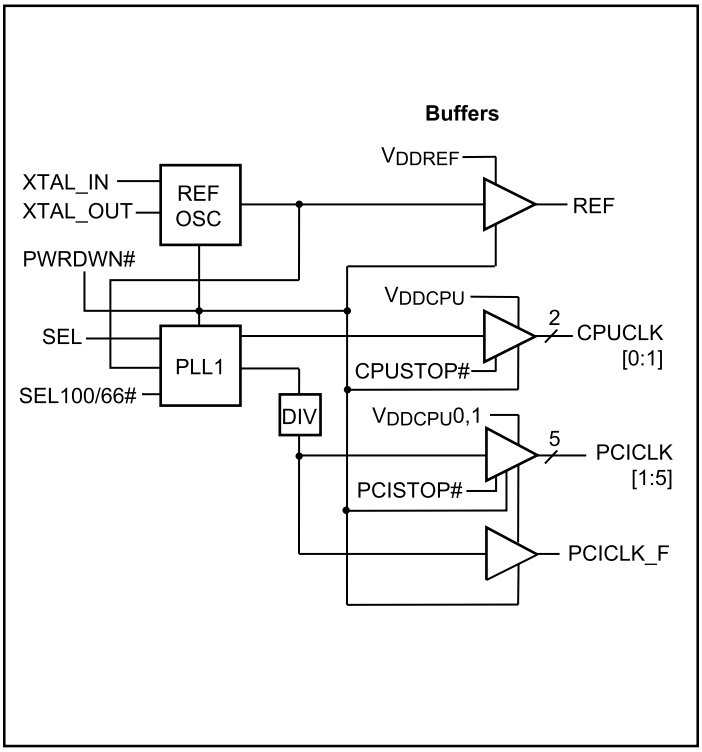
Description

The PI6C102 is a high-speed low-noise clock generator designed to work with the Pericom's PI6C18x clock buffer to meet all clock needs for Mobile Intel Architecture platforms. CPU and chipset clock frequencies of 66.6 MHz and 100 MHz are supported.

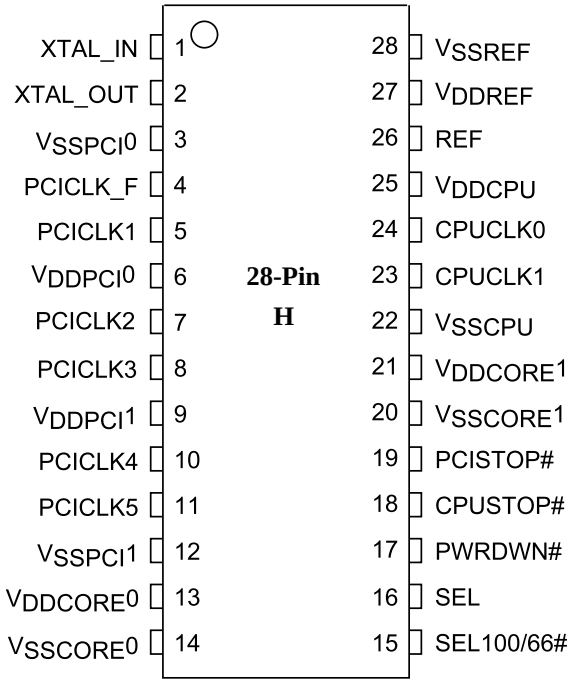
Split supplies of 3.3V and 2.5V are used. The 3.3V power supply powers a portion of the I/O and the core. The 2.5V is used to power the remaining outputs. 2.5V signaling follows JEDEC standard 8-X. Power sequencing of the 3.3V and 2.5V supplies is not required.

An asynchronous PWRDWN# signal may be used to orderly power down (or up) the system.

Block Diagram



Pin Configuration



Pin Description

Pin	Signal Name	Type	Qty.	Description
1	XTAL_IN	I	1	14.318 MHz crystal input
2	XTAL_OUT	O	1	14.318 MHz crystal output
3,12	V_{SSPCI}[0:1]	ground	2	Ground for PCI clock outputs
4	PCICLK_F	O	1	Free running PCI clock output
5,7,8,10,11	PCICLK[1:5]	O	5	PCI clock outputs, TTL comatible 3.3V
6,9	V_{DDPCI} [0:1]	power	2	Power for PCI clock outputs
21	$V_{DDCORE\ 1}$	power	1	Isolated power for core
20	$V_{SSCORE\ 1}$	ground	1	Isolated ground for core
15	SEL100/66#	I	1	Select pin for enabling 100 MHz or 66 MHz H = 100 MHz. L = 66 MHz
16	SEL	I	1	Test or Active Mode Select
17	PWRDWN#	I	1	Powers down device when held LOW
18	CPUSTOP#	I	1	Stops CPU clocks LOW if held LOW
19	PCISTOP#	I	1	Stops PCI clocks LOW if held LOW
22	V_{SSCPU}	ground	1	Ground for CPU outputs
23,24	CPUCLK[0:1]	O	2	CPU and Host clock outputs 2.5V
25	V_{DDCPU}	power	1	Power for CPU outputs
26	REF	O	1	14.318 MHz clock output
27	V_{DDREF}	power	1	Power for REF outputs
28	V_{SSREF}	ground	1	Ground for REF outputs

Select Functions

SEL100/66#	SEL	Function
0	0	Hi-Z
0	1	66 MHz active
1	0	Test Mode
1	1	100 MHz active

Function Description	Outputs		
	CPU [0:1]	PCI[0:5], PCIF	REF
Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2	TCLK/6	TCLK

Notes:
TCLK is a test clock over driven on he XTAL_IN inpu during test mode.

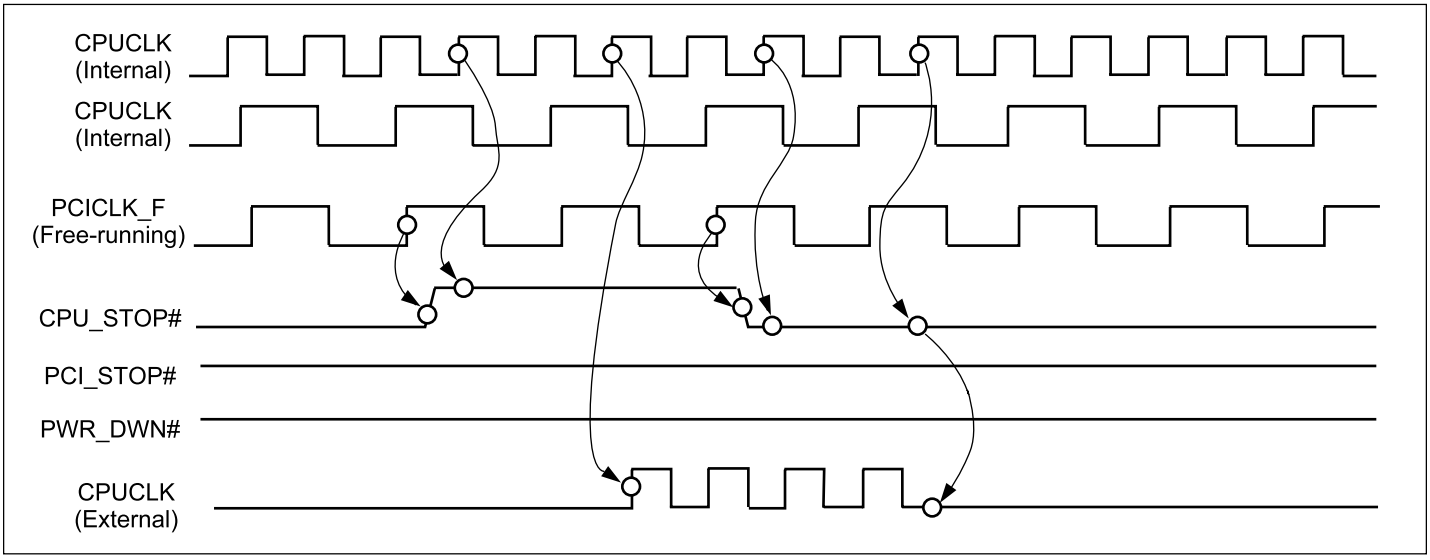
Clock Enable Configuration

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK [0:1]	PCICLK[1:5]	PCICLK_F	Other Clocks	Crystal	VCO's
X	X	0	low	low	low	stopped	off	off
0	0	1	low	low	33 MHz	running	running	running
0	1	1	low	33 MHz	33 MHz	running	running	running
1	0	1	100/66 MHz	low	33 MHz	running	running	running
1	1	1	100/66 MHz	33 MHz	33 MHz	running	running	running

Power Management Timing

Signal	Signal State	Latency
		No. of rising edges of free running PCICLK
CPU_STOP#	0 (disabled)	1
	1 (enabled)	1
PCI_STOP#	0 (disabled)	1
	1 (enabled)	1
PWR_DWN#	1 (normal operation)	3ms
	0 (power down)	2 max.

Notes:
1. Clock on/off latency is defined as the number of rising edges of free running PCICLKs between when the clock disable goes low/high to when the first valid clock comes out of the device.
2. Power-up latency is from when PWR_DWN# goes inactive (HIGH) to when the first valid clocks are driven from the device.

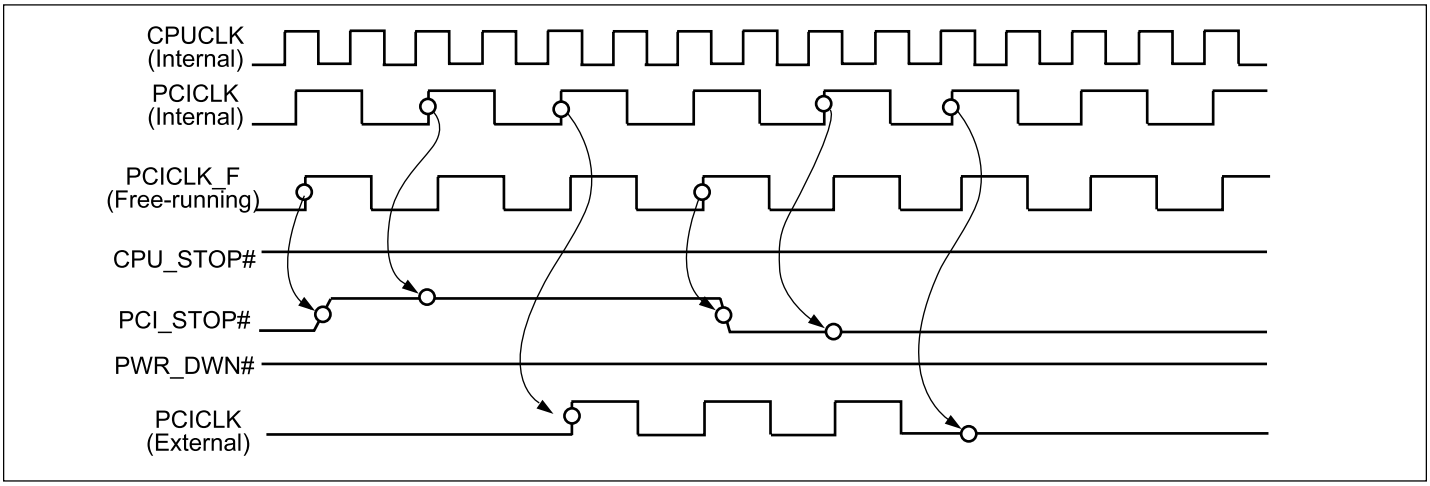


CPU_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only.
3 CPU_STOP# is an input signal that must be made synchronous to the free running PCI_F.
4. ON/OFF latency shown in the diagram is 2 CPU clocks.
5. All other clocks continue to run undisturbed.
6. PWR_DWN# and PCI_STOP# are shown in a HIGH state.
7. Diagrams shown with respect to 66 MHz. Similar operation as CPU = 100 MHz.

CPU_STOP# is an input signal used to turn off the CPU clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock and is internally synchronized to the external PCICLK_F output. All other clocks continue to run while the CPU clocks are disabled. The CPU clocks are always stopped in a LOW state and started guaranteeing that the high pulse width is a full pulse. CPU clock on latency is 2 or 3 CPU clocks and CPU clock off latency is 2 or 3 CPU clocks.

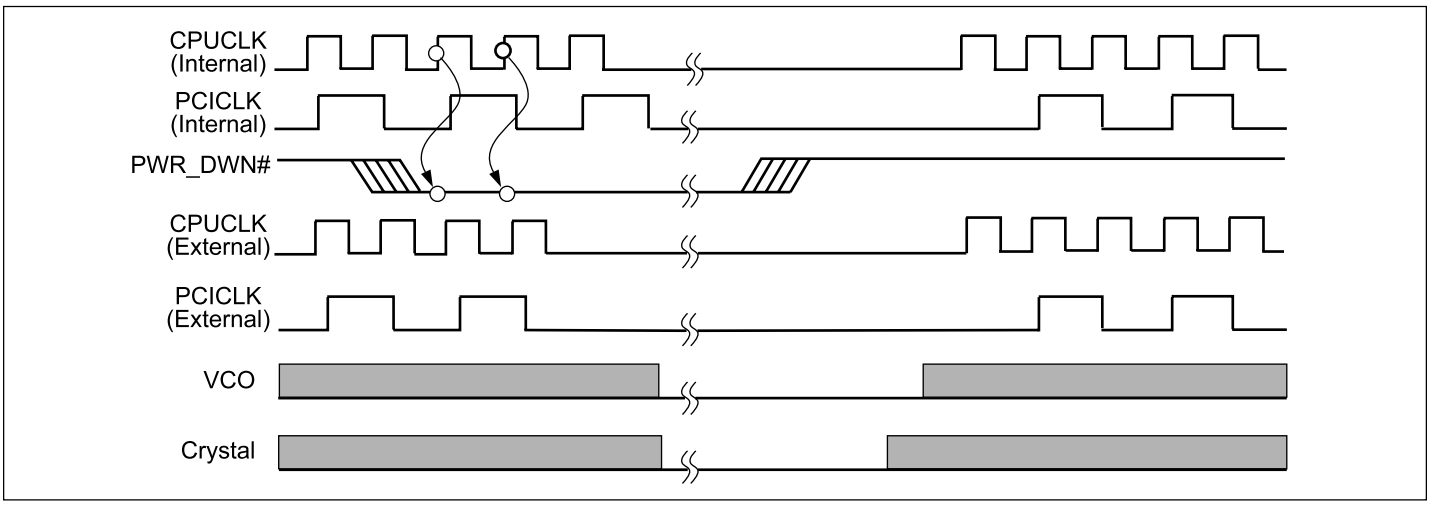
PCI_STOP# is an input signal used to turn off PCI clocks for low power operation. PCI clocks are stopped in the LOW state and started with a guaranteed full high pulse width. There is ONLY one rising edge of external PCICLK after the clock control logic.



PCI_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. PCI_STOP# signal is an input signal which must be made synchronous to PCI_F output.
3 Internal means inside the chip.
4. All other clocks continue to run undisturbed.
5. PWR_DWN# and CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 66 MHz. Similar operation as CPU = 100 MHz.

The PWR_DWN# is used to place the device in a very low power state. PWR_DWN# is an asynchronous active low input. Internal clocks are stopped after the device is put in power-down mode. The power-on latency is less than 3ms. PCI_STOP# and CPU_STOP# are "don't cares" during the power-down operations. The REF clock is stopped in the LOW state as soon as possible.



PWR_DWN# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only.
3. PWR_DWN# is an asynchronous input and metastable conditions could exist. The signal is synchronized inside the part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown wth respect to 66 MHz. Similar operation as CPU = 100 MHz.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
3.3V Supply Voltage to Ground Potential	–0.5V to +4.6V
2.5V Supply Voltage to Ground Potential	–0.5V to +3.6V
DC Input Voltage	–0.5V to +4.6V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (V_{DDQ3} = +3.3V ± 5%, V_{DDQ2} = +2.5V ± 5%, T_A = 0°C to +70°C)

PI6C102 Condition	Max. 2.5V Supply Consumption Max. discrete cap loads, V_{DDQ2} = 2.625V All static inputs = V_{DDQ3} or V_{SS}	Max. 3.3V Supply Consumption Max. discrete cap loads, V_{DDQ3} = 3.465V All static inputs = V_{DDQ3} or V_{SS}
Powerdown Mode (PWRDWN# =0)	100µA	500µA
Active 66 MHz SEL 100/66# = 0	72mA	170mA
Active 100 MHz SEL 100/66# = 1	100mA	170mA

DC Operating Specifications

Symbol	Parameters	Conditions	Min.	Max.	Units
V_{DD} = 3.3V ± 5%					
V_{IH3}	Input high voltage	V_{DD}	2.0	V_{DD} +0.3	V
V_{IL3}	Input low voltage		V_{SS} -0.3	0.8	
I_{IL}	Input leakage current	$0 < V_{IN} < V_{DD}$	-5	+5	µA
V_{DD} = 2.5V ± 5%					
V_{OH2}	Output high voltage	I_{OH} = -1mA	2.0		V
V_{OL2}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{OH3}	Output high voltage	I_{OH} = -1mA	2.4		V
V_{OL3}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{POH}	PCI Bus output high voltage	I_{OH} = -1mA	2.4		V
V_{POL}	PCI Bus output low voltage	I_{OL} = 1mA		0.55	
C_{IN}	Input pin capacitance			5	pF
C_{XTAL}	Xtal pins capacitance	13.5	18.0	22.5	
C_{OUT}	Output pin capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No airflow	0	70	°C

Buffer Specifications

Buffer Name	V_{DD} Range(V)	Impedance (Ω)	Buffer Type
CPU	2.375 -2.625	13.5 - 45	Type 1
REF	3.135 - 3.465	20 - 60	Type 3
PCI	3.135 - 3.465	12 - 55	Type 5

Type 1: CPU Clock Buffers (2.5V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-27			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-27	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	27			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			30	
t_{RH}	2.5V Type 1 output rise edge rate	2.5V ± 5% @ 0.4V-2.0V	1		4	V/ns
t_{FH}	2.5V Type 1 output fall edge rate	2.5V ± 5% @ 2.0V-0.4V	1		4	

Type 3: REF (3.3V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-29			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-23	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	29			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			27	
t_{RH}	3.3V Type 3 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	0.5		2	V/ns
t_{FH}	3.3V Type 3 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	0.5		2	

Type 5: PCI Clock Buffers (3.3V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-33			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			-33	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.95V	30			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			38	
t_{RH}	3.3V Type 5 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	1		4	V/ns
t_{FH}	3.3V Type 5 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	1		4	

AC Timing

Figure 1. Host Clock to PCI CLK Offset	Parameters	66 MHz		100 MHz		Units
		Min.	Max.	Min.	Max.	
t_{HKP} (2.5V)	Host CLK period	15.0	15.5	10.0	10.5	ns
t_{HKH} (2.5V)	Host CLK high time	5.2		3.0		
t_{HKL} (2.5V)	Host CLK low time	5.0		2.8		
t_{HRISE} (2.5V)	Host CLK rise time	0.4	1.6	0.4	1.6	
t_{HFALL} (2.5V)	Host CLK fall time	0.4	1.6	0.4	1.6	
t_{JITTER} (2.5V)	Host CLK Jitter		250		250	ps
Duty Cycle (2.5V)	Measured at 1.25V	45	55	45	55	%
t_{HSKW} (2.5V)	Host Bus CLK Skew		175		175	ps
t_{PZL}, t_{PZH}	Output enable delay	1.0	8.0	1.0	8.0	ns
t_{PLZ}, t_{PHZ}	Output disable delay	1.0	8.0	1.0	8.0	
t_{HSTB}	Host CLK Stabilization from power-up		3		3	ms
t_{PKP}	PCI CLK period	30.0	∝	30.0	∝	ns
t_{PKPS}	PCI CLK period stability		500		500	ps
t_{PKH}	PCI CLK high time	12.0		12.0		ns
t_{PKL}	PCI CLK low time	12.0		12.0		
t_{PSKW}	PCI Bus CLK Skew		500		500	ps
$t_{HPOFFSET}$	Host to PCI Clock Offset	1.5	4.0	1.5	4.0	ns
t_{PSTB}	PCI CLK Stabilization from power-up		3		3	ms

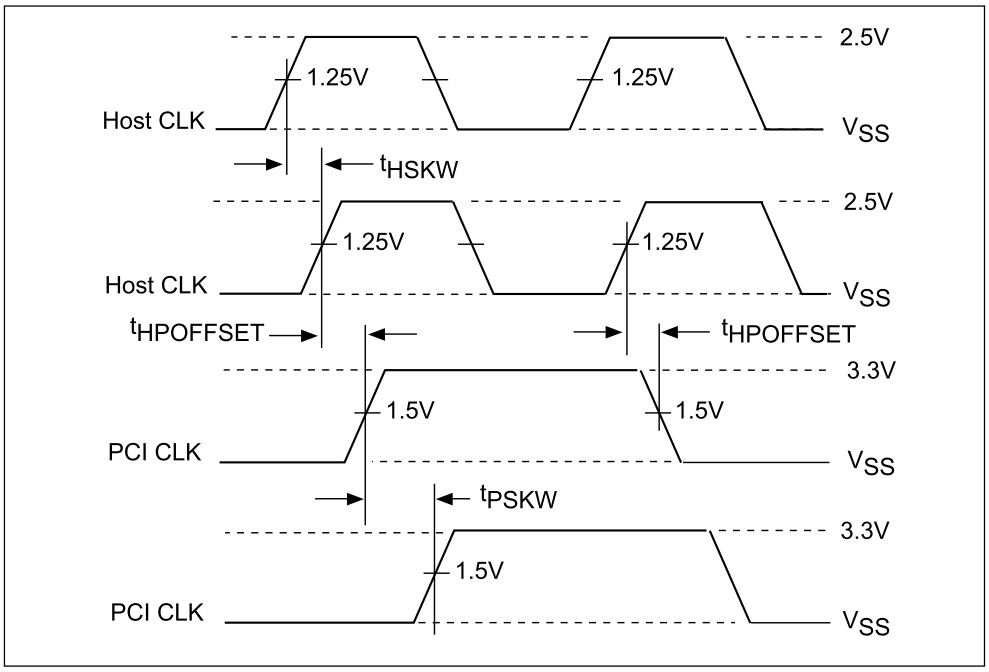


Figure 1. Host Clock and PCI CLK Timing

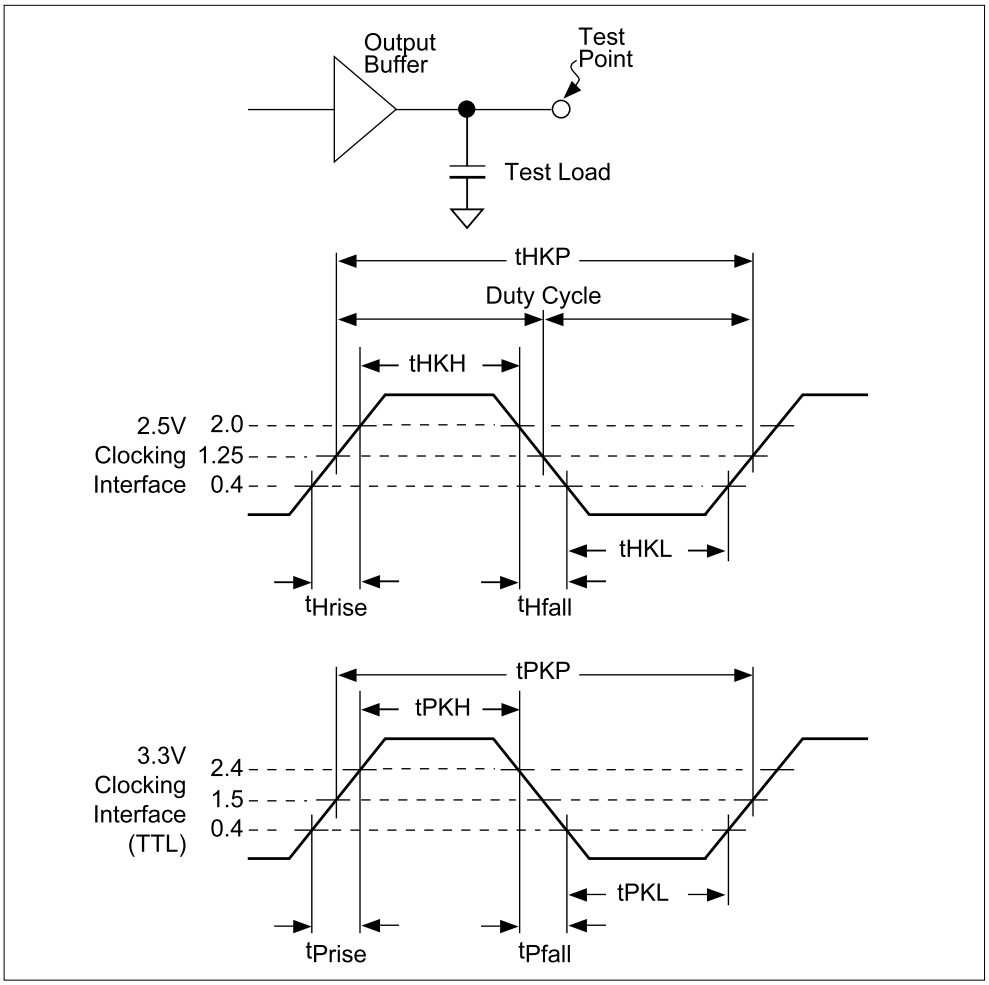
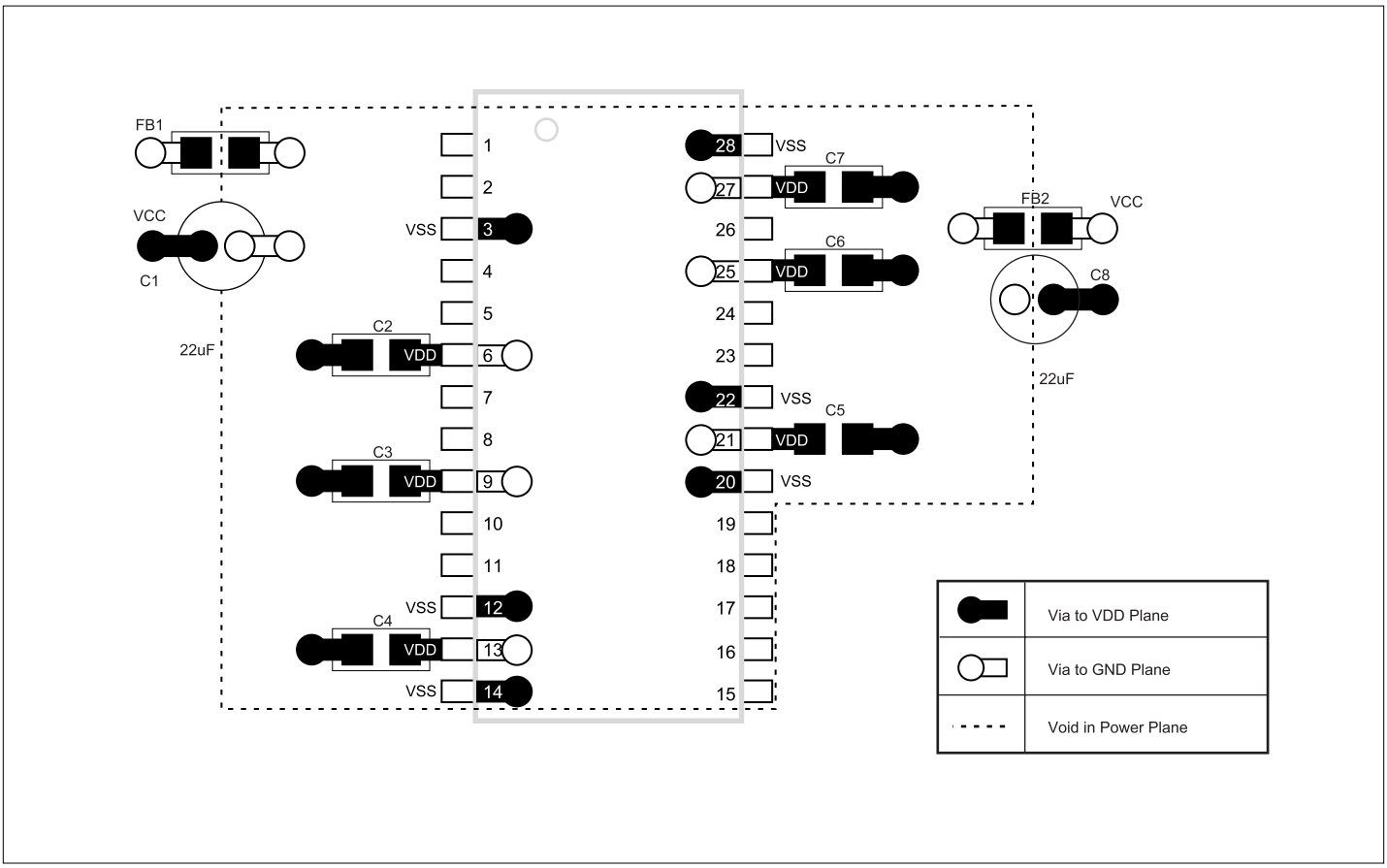


Figure 2. Clock Output Waveforms

PCB Layout Suggestion



Note:

This is only a suggested layout. There may be alternate solutions depending on actual PCB design and layout.

As a general rule, C2-C7 should be placed as close as possible to their respective V_{DD}.

Recommended capacitor values:

C2-C7 ..... 0.1µF, ceramic

C1, C8 ..... 22µF

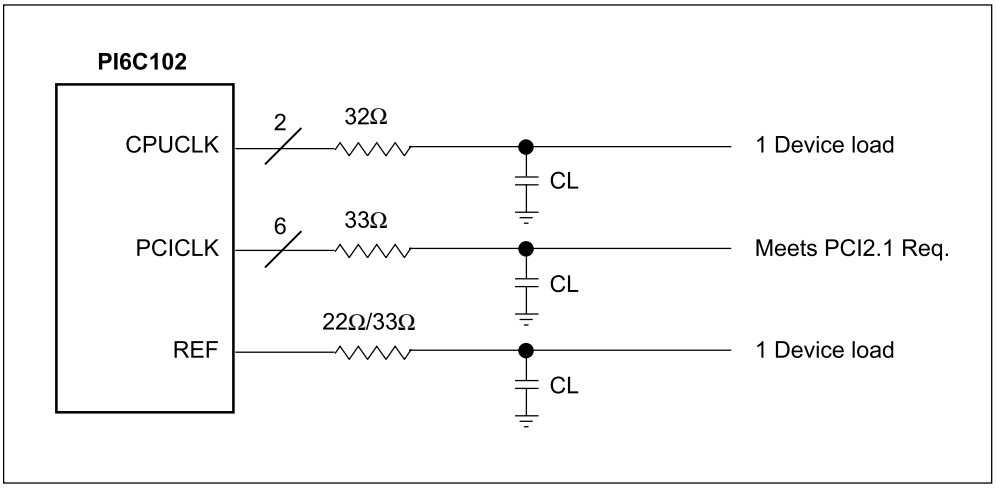
Minimum and Maximum Expected Capacitive Loads

Clock	Min. Load	Max. Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads
PCI Clocks (PCLK)	30	30		Meets PCI 2.1 requirements
REF	10	20		1 device load

Notes:
1. Maximum rise/fall times are guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are guaranteed at minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.



Ordering Information

P/N	Description
PI6C102H	28-pin SSOP Package