PI6C180

Precision 1-18 Clock Buffer

Product Features

- High-speed, to 100 MHz
- Low-noise non-inverting 1-18 buffer
- Supports up to four SDRAM DIMMs
- Low skew (< 250ps) between any two output clocks
- I^2C Serial Configuration interface
- Multiple V_{DD}, V_{SS} pins for noise reduction
- 3.3V power supply voltage
- Separate Hi-Z pin for testing
- 48-pin SSOP package (V)

Description

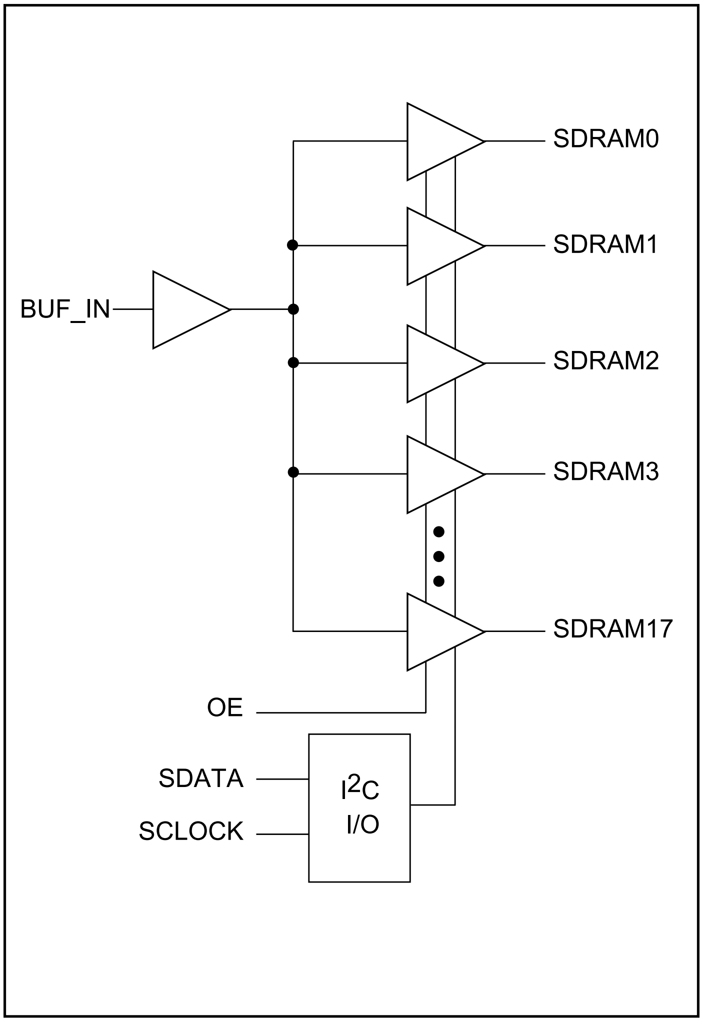
The PI6C180, a high-speed low-noise 1-18 non-inverting buffer designed for SDRAM clock buffer applications operates up to 100 MHz.

At power up all SDRAM output are enabled and active. The I^2C Serial control may be used to individually activate/deactivate any of the 18 output drivers.

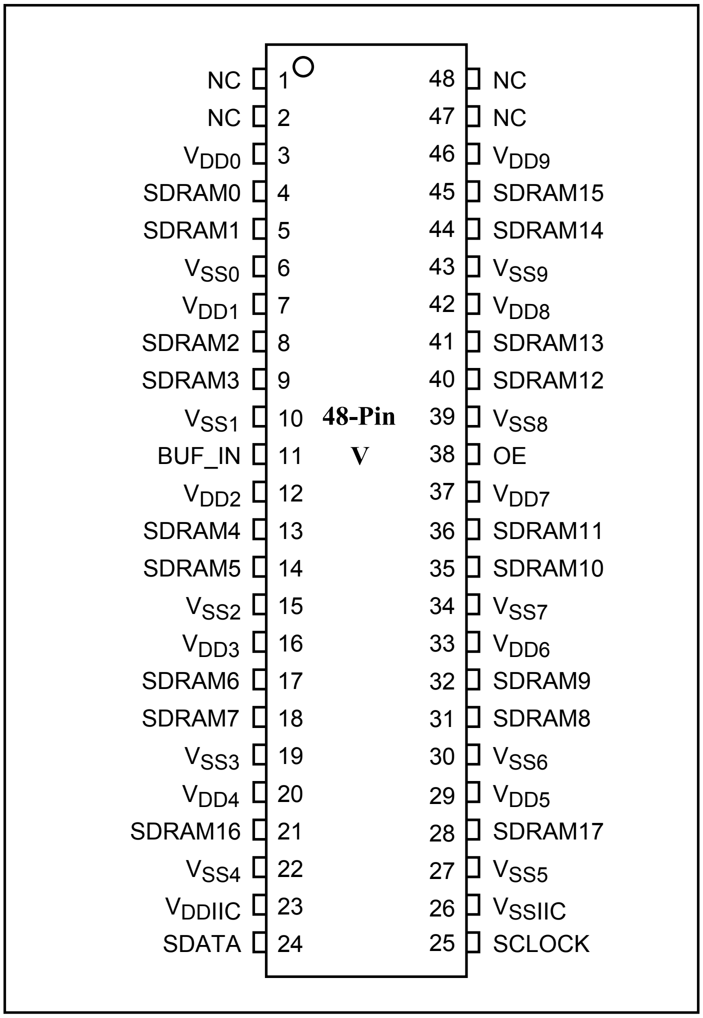
The output enable (OE) pin may be pulled low to put all outputs in a Hi-Z state.

Note:
Purchase of I^2C components from Pericom conveys a license to use them in an I^2C system as defined by Philips.

Logic Block Diagram



Product Pin Configuration



Product Pin Description

Pin	Symbol	Type	Qty	Description
4,5,8,9	SDRAM[0-3]	O	4	SDRAM Byte 0 clock output
13,14,17,18	SDRAM[4-7]	O	4	SDRAM Byte 1 clock output
31,32,35,36	SDRAM[8-11]	O	4	SDRAM Byte 2 clock output
40,41,44,45	SDRAM[12-15]	O	4	SDRAM Byte 3 clock output
21,28	SDRAM[16-17]	O	4	SDRAM clock outputs usable for feedback
11	BUF_IN	I	1	Input for 1-18 buffer
38	OE	I	1	Hi-Z all outputs when held LOW. Has a >100kohm internal pull-up resistor
24	SDATA	I/O	1	Data pin for I^2C circuitry. Has a >100kohm internal pull-up resistor
25	SCLOCK	I/O	1	Clock pin I^2C circuitry. Has a >100kohm internal pull-up resistor
3,7,12,16,20, 29,33,37, 42,46	$V_{DD[0-9]}$	Power	10	3.3V power supply for SDRAM buffers
6,10,15,19,22,27,30,34, 39,43	$V_{SS[0-9]}$	Ground	10	Ground for SDRAM buffers
23	V_{DDIIC}	Power	1	3.3V power supply for I^2C circuitry
26	V_{SSIIC}	Ground	1	Ground for I^2C circuitry
1,2,47,48	NC	Reserved	4	Reserved for future modification. No connects

OE Functionality

OE	SDRAM[0-17]	Note
0	Hi-Z	1
1	BUF_IN	2

Notes:

1. Used for test purposes only
2. Buffers are non-inverting

PI6C180 I^2C Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0

PI6C180 Serial Configuration Map

Byte0: SDRAM Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin Number	Description
Bit 7	18	SDRAM7 (Active/Inactive)
Bit 6	17	SDRAM6 (Active/Inactive)
Bit 5	14	SDRAM5 (Active/Inactive)
Bit 4	13	SDRAM4 (Active/Inactive)
Bit 3	9	SDRAM3 (Active/Inactive)
Bit 2	8	SDRAM2 (Active/Inactive)
Bit 1	5	SDRAM1 (Active/Inactive)
Bit 0	4	SDRAM0 (Active/Inactive)

Note:
Inactive means outputs are held LOW and are disabled from switching.

2-Wire I^2C Control

The I^2C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C180 is a slave receiver device. It can not be read back. Sub addressing is not supported. All preceding bytes must be sent in order to change one of the control bytes.

Every bite put on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiving device.

During normal data transfers SDATA changes only when SCLOCK is LOW. Exceptions: A HIGH to LOW transition on SDATA while SCLOCK is HIGH indicates a “start” condition. A LOW to HIGH transition on SDATAwhile SCLOCK is HIGH is a “stop” condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW= write to addressed device). If the device’s own address is detected, PI6C180 generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (D2), two more bytes must be sent:

1. “Command Code” byte, and
2. “Byte Count” byte.

Although the data bits on these two bytes are “don’t care,” they must be sent and acknowledged.

Byte1: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	Description
Bit 7	45	SDRAM15 (Active/Inactive)
Bit 6	44	SDRAM14 (Active/Inactive)
Bit 5	41	SDRAM13 (Active/Inactive)
Bit 4	40	SDRAM12 (Active/Inactive)
Bit 3	36	SDRAM11 (Active/Inactive)
Bit 2	35	SDRAM10 (Active/Inactive)
Bit 1	32	SDRAM9 (Active/Inactive)
Bit 0	31	SDRAM8 (Active/Inactive)

Byte2: Optional Register for Possible Future Requirements (1 = enable, 0 = disable)

Bit	Pin #	Description
Bit 7	28	SDRAM17 (Active/Inactive)
Bit 6	21	SDRAM16 (Active/Inactive)
Bit 5		(Reserved)
Bit 4		(Reserved)
Bit 3		(Reserved)
Bit 2		(Reserved)
Bit 1		(Reserved)
Bit 0		(Reserved)

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
3.3V Supply Voltage to Ground Potential	–0.5V to +4.6V
DC Input Voltage	–0.5V to +4.6V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Supply Current (V_{DD} = +3.465V, C_{LOAD} = Max.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{DD}	Supply Current	BUF_IN = 0 MHz			3	mA
I_{DD}	Supply Current	BUF_IN = 66.66 MHz			230	
I_{DD}	Supply Current	BUF_IN = 100.0 MHz			360	

DC Operating Specifications (V_{DD} = +3.3V ±5%, T_A = 0°C - 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Units
Input Voltage					
V_{IH}	Input high voltage	V_{DD}	2.0	V_{DD} +0.3	V
V_{IL}	Input low voltage		V_{SS} -0.3	0.8	
I_{IL}	Input leakage current	$0 < V_{IN} < V_{DD}$	-5	+5	mA
V_{DD}[0-9] = 3.3V ±5%					
V_{OH}	Output high voltage	I_{OH} = -1mA	2.4		V
V_{OL}	Output low voltage	I_{OL} = 1mA		0.4	
C_{OUT}	Output pin capacitance			6	pF
C_{IN}	Input pin capacitance			5	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No Airflow	0	70	°C

SDRAM Clock Buffer Operating Specification

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 2.0V	–54			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			–46	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.0V	54			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			53	
t_{RH}SDRAM	Output rise edge rate SDRAM only	3.3V ±5% @04V-2.4V	1.5		4	V/ns
t_{TH}SDRAM	Output fall edge rate SDRAM only	3.3V ±5% @2.4V-0.4V	1.5		4	

AC Timing

Symbol	Parameter	66 MHz		100 MHz		Units
		Min.	Max.	Min.	Max.	
t_{SDKP}	SDRAM CLK period	15.0	15.5	10.0	10.5	ns
t_{SDKH}	SDRAM CLK high time	5.6		3.3		
t_{SDKL}	SDRAM CLK low time	5.3		3.1		
t_{SDRISE}	SDRAM CLK rise time	1.5	4.0	1.5	4.0	V/ns
t_{SDFALL}	SDRAM CLK fall time	1.5	4.0	1.5	4.0	
t_{PLH}	SDRAM Buffer LH prop delay	1.0	5.0	1.0	5.0	ns
t_{PHL}	SDRAM Buffer HL prop delay	1.0	5.0	1.0	5.0	
t_{PZL},t_{PZH}	SDRAM Buffer Enable delay	1.0	8.0	1.0	8.0	
t_{PLZ},t_{PHZ}	SDRAM Buffer Disable delay	1.0	8.0	1.0	8.0	
Duty Cycle	Measured at 1.5V	45	55	45	55	%
t_{SDSKW}	SDRAM Output to Output Skew		250		250	ps

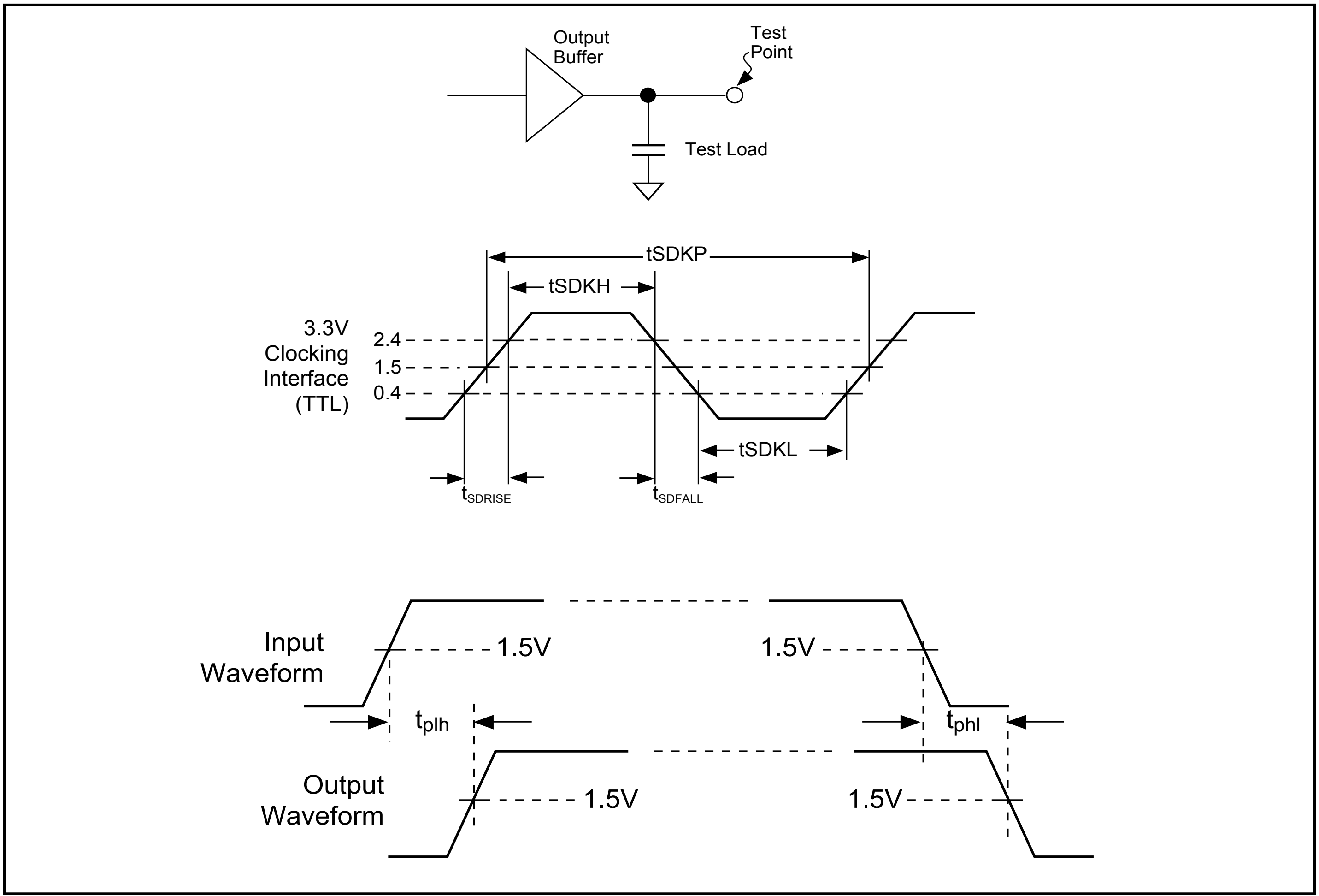


Figure 1. Clock Waveforms

Minimum & Maximum Expected Capacitive Loads

Clock	Min. Load	Max. Load	Units	Notes
SDRAM	20	30	pF	SDRAM DIMM Specification

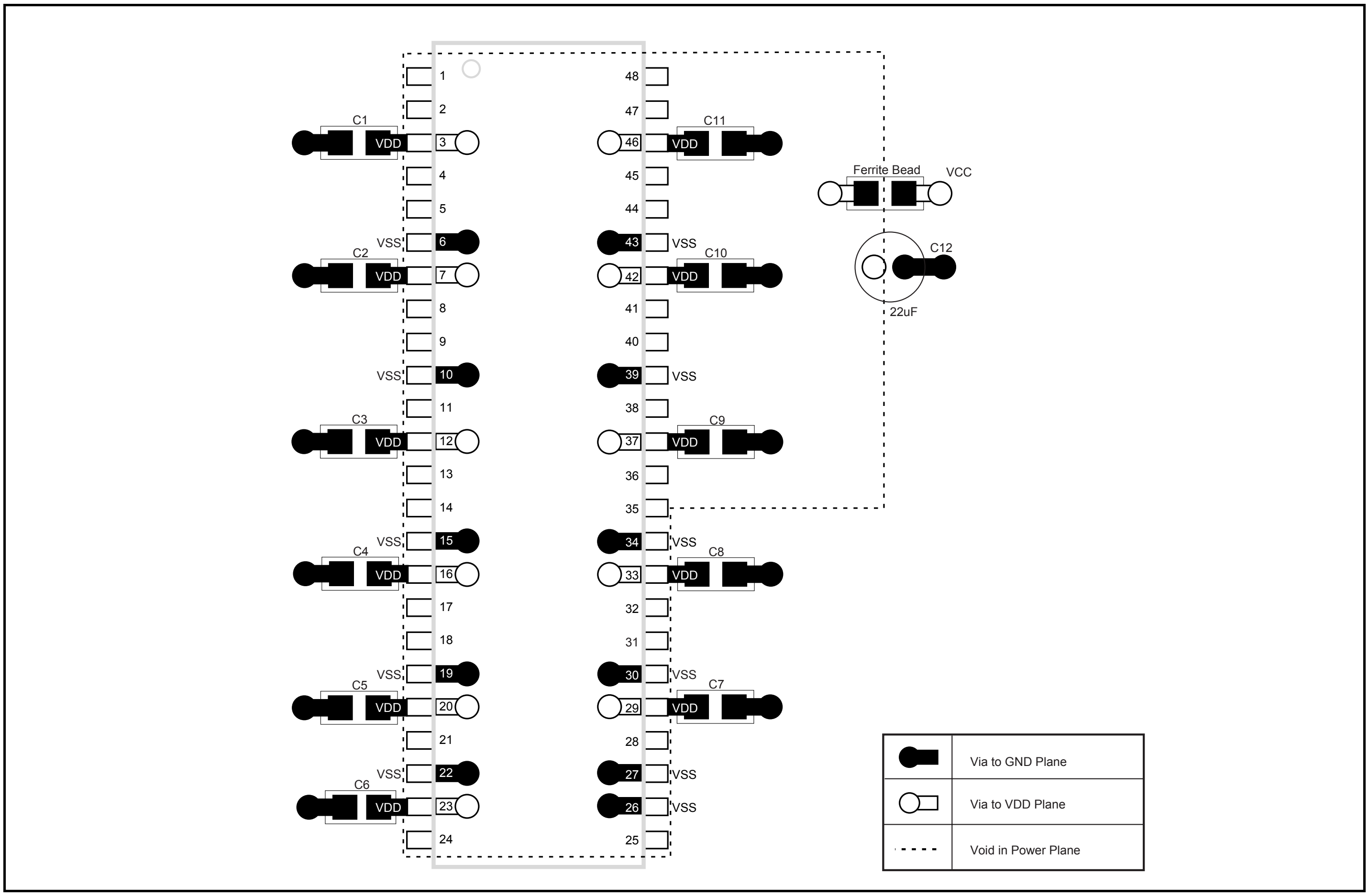
Notes:

1. Maximum rise/fall times are guaranteed at maximum specified load.
2. Minimum rise/fall times are guaranteed at minimum specified load.
3. Rise/fall times are specified with pure capacitive load as shown.
   Testing is done with an additional 500-ohm resistor in parallel.

Design Guidelines to Reduce EMI

1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.

PCB Layout Suggestion



Note:

This is only a suggested layout. There may be alternate solutions depending on actual PCB design and layout.

As a general rule, C1-C11 should be placed as close as possible to their respective V_{DD}.

Recommended capacitor values:
C1-C11 .... 0.1µF, ceramic
C12 .... 22µF

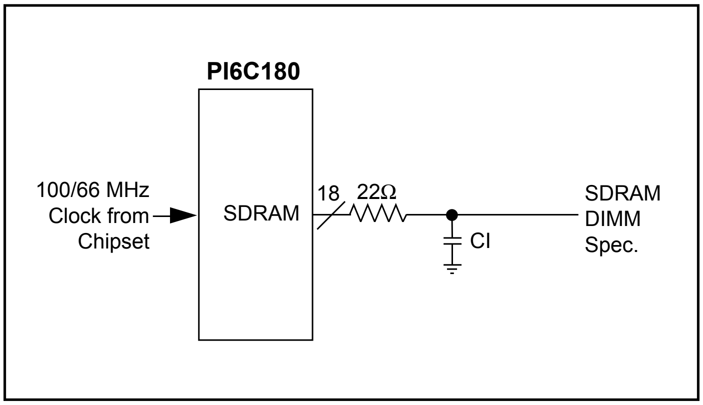


Figure 2. Design Guidelines

48-Pin SSOP (V) Package

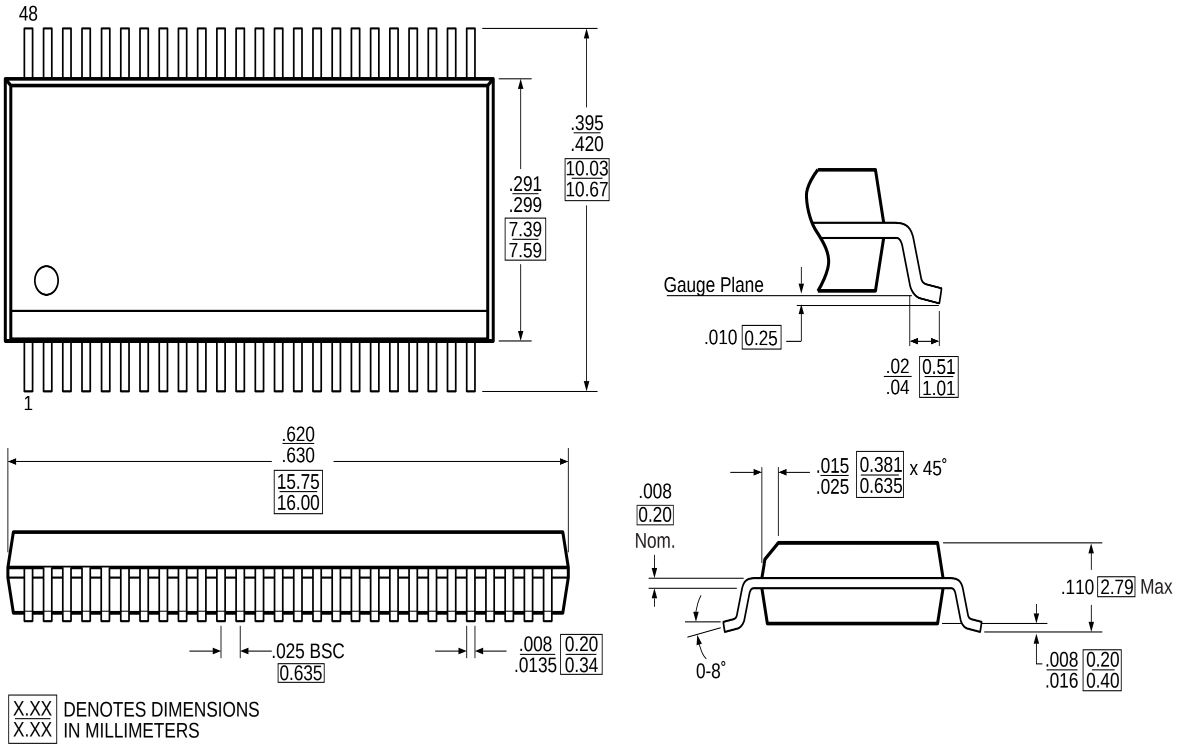


Table of Dimensions

Body		E (Width)	D (Length)	A (Height)	e (Pin-to-Pin pitch)
48 pins	Min.	0.291	0.620	0.095	0.025
(300 mil)	Max.	0.299	0.630	0.110	—

Ordering Information

P/N	Description
PI6C180V	48-pin SSOP Package