PS4530/PS4531/PS4532

Precision 8-Ch, 2-Ch, Latched Analog Multiplexers/Switches

Features

- Low On-Resistance (60 Ohm typ.) Minimizes Distortion and Error Voltages
- Single-Supply Operation (+2.0V to 12.0V)
- Dual-Supply Operation (± 2.0V to ± 6.0V)
- Improved Second Sources for MAX4530/MAX4531/MAX4532
- 75 Ohm On-Resistance with ±5V supplies
- 150 Ohm On-Resistance with ±5V supply
- TTL/CMOS Logic Compatible
- Fast Switching Speed, t_{ON} and t_{OFF} = 150ns & 120ns at ±4.5V
- Break-Before-Make action eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Range
- Low Power Consumption, <1µW
- Narrow SOIC, and SSOP Packages Minimize Board Area

Description

PS4530/PS4531/PS4532 are low voltage CMOS analog ICs configured as an 8-channel multiplexer (mux) (PS4530), two 4-channel muxes (PS4531), and three single-pole/double-throw switches (PS4532). These devices are pin compatible with the industry standard 74H4351/74HC4352/74HC4353. All devices have two complementary switch-enable inputs and address latching.

The PS4530/PS4531/PS4532 operate from a single supply of +2V to +12V, or from dual supplies of ±2V to ±6V. On-resistance (150Ohm max.) is matched between switches to 8Ohm max. Each switch can handle rail-to-rail analog signals. Off-leakage current is only 1nA at T_A = +25°C and 50nA at T_A = +85°C.

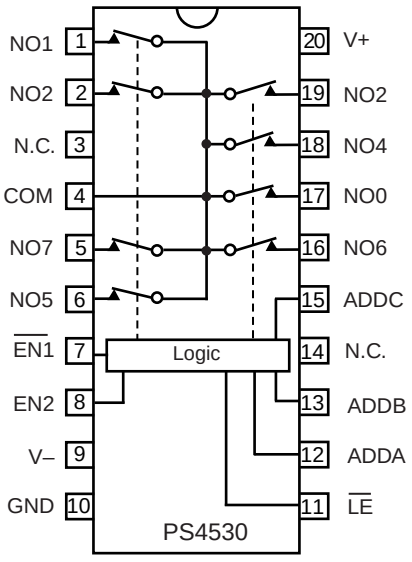
All digital inputs have 0.8V and 2.4V logic thresholds, ensuring both TTL-logic and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

- Data Acquisition Systems
- Audio Switching and Routing
- Test Equipment
- PBX, PABX
- Telecommunication Systems
- Battery-Powered Systems

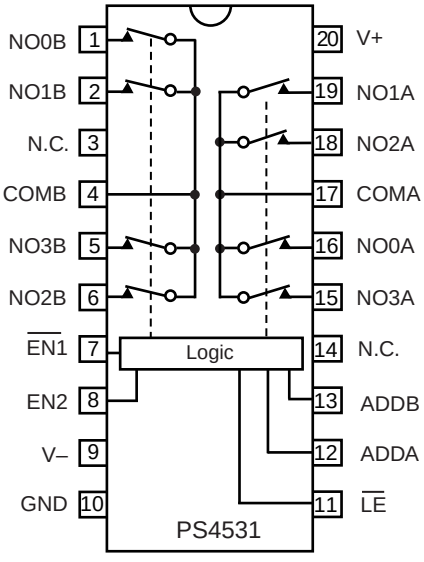
Functional Block Diagrams and Pin Configurations

Top View
PS4530



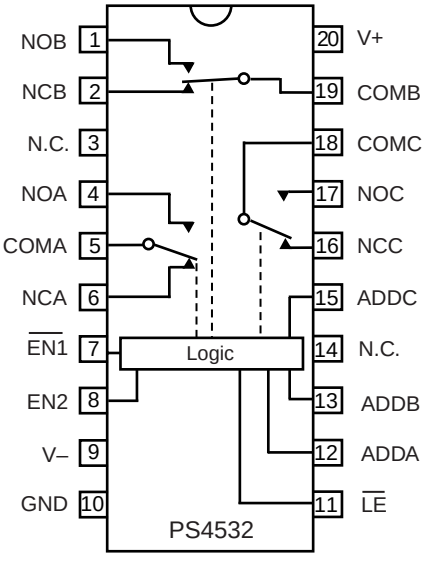
NARROW DIP/WIDE SO

Top View
PS4531



NARROW DIP/WIDE SO

Top View
PS4532



NARROW DIP/WIDE SO

Truth Table

LE	EN2	EN1	ADDRESS BITS			ON SWITCHES		
			ADDC*	ADDB	ADDA	PS4530	PS431	PS4532
0	1	0	X	X	X	Last address	Last address	Last address
X	0	X	X	X	X	All switches open	All switches open	All switches open
X	X	1	X	X	X	All switches open	All switches open	All switches open
1	1	0	0	0	0	COM-NO0	COMA-NO0A, COMB-NO0B	COMA-NCA, COMB-NCB, COMC-NCC
1	1	0	0	0	1	COM-NO1	COMA-NO1A, COMB-NO1B	COMA-NOA, COMB-NCB, COMC-NCC
1	1	0	0	1	0	COM-NO2	COMA-NO2A, COMB-NO2B	COMA-NCA, COMB-NOB, COMC-NCC
1	1	0	0	1	1	COM-NO3	COMA-NO3A, COMB-NO3B	COMA-NOA, COMB-NOB, COMC-NCC
1	1	0	1	0	0	COM-NO4	COMA-NO0A, COMB-NO0B	COMA-NCA, COMB-NCB, COMC-NOC
1	1	0	1	0	1	COM-NO5	COMA-NO1A, COMB-NO1B	COMA-NOA, COMB-NCB, COMC-NOC
1	1	0	1	1	0	COM-NO6	COMA-NO2A, COMB-NO2B	COMA-NCA, COMB-NOB, COMC-NOC
1	1	0	1	1	1	COM-NO7	COMA-NO3A, COMB-NO3B	COMA-NOA, COMB-NOB, COMC-NOC

X = Don't Care *ADDC not present of PS4531.

Note:

NO_ and COM_ pins are identical and interchangeable. Either may be considered an input or an output; signals pass equally well in either direction. LE is independent of EN1 and EN2.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltages Referenced to V–	
V+	–0.3V to +13V
Voltage into Any Terminal(1)	
or ±20mA (whichever occurs first)	–0.3V to (V++0.3V)
Continuous Current into Any Terminal	±20mA
Peak Current, NO, NC, or COM_	
(pulsed at 1ms, 10% duty cycle	±40mA
ESD per Method 3015.7	>2000V
Continuous Power Dissipation (T_A = +70°C)	
SO (derate 10.00mW/°C above +70°C)	800mW
SSOP (derate 8.00mW/°C above +70°C)	640mW
Operating Temperature Ranges	
PS453_C_P	0°C to +70°C
PS453_E_P	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperture (soldering, 10s	+30°C

Note:
Voltages exceeding V+ or V– on any signal terminal are clampled by internal diodes.
Limit forward-diode current to maximum currant rating.

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Specifications - Dual Supplies

(V+ = +5V ±10%, V– = –5V ±10%, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{LE} = 2.4V$, $V_{ADD\_L} = V_{EN\_L} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Symbol	Conditions			Min(2)	Typ(2)	Max(2)	Units
Switch								
Analog Signal Range	V_{COM}, V_{NO}, $V_{NC\_}$	Note(3)			V–		V+	V
Channel On Resistance	R_{ON}	I_{NO} = 2mA, V_{COM} = ±3.5V, V+ = 4.5V, V– = –4.5V		T_A = +25°C		20	35	Ohm
				$T_A = T_{MIN}$ to T_{MAX}			45	
On-Resistance Matching Between Channals(4)	ΔR_{ON}	I_{NO} = 2mA, V_{COM} = ±3.5V, V+ = 4.5V, V– = –4.5V		T_A = +25°C		6	8	
				$T_A = T_{MIN}$ to T_{MAX}		8	10	
On -Resistance Flatnesss(5)	$R_{FLAT(ON)}$	I_{NO} = 2mA, V_{COM} = –3V,0V, +3V; V+ = 5V; V– = –5V		T_A = +25°C			6	
				$T_A = T_{MIN}$ to T_{MAX}			8	
NO-Off Leakage Current(6)	$I_{NO(OFF)}$	V_{NO} = ±4.5V, V_{COM} = ±4.5V, V+ = 5.5V, V– = –5.5V		T_A = +25°C	–80	0.01	80	nA
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
COM-Off Leakage Current(6)	$I_{COM(OFF)}$	V_{COM} = ±4.5V, V_{NO} ±4.5V, V+ = 5.5V, V– = –5.5V	PS4530	T_A = +25°C	–80	0.01	80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
		V_{COM} = ±4.5V, V_{NO} ±4.5V, V+ = 5.5V, V– = –5.5V	PS4531, PS4532	T_A = +25°C	–80	0.01	80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
COM-On Leakage Current(6)	$I_{COM(ON)}$	V_{COM} = ±4.5V, V+ = 5.5V, V– = –5.5V	PS4530	T_A = +25°C	–80	0.01	80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
			PS4531, PS4532	T_A = +25°C	–80	0.01	80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	

Electrical Specifications - Dual Supplies (continued)

(V+ = +5V ±10%, V– = –5V ±10%, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{LE}$ = 2.4V, $V_{ADD\_L} = V_{EN\_L}$ = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Symbol	Conditions		Min(2)	Typ(2)	Max(2)	Units
Digital Logic Input							
Logic High Threshold	V_{ADD_H}, V_{EN_H}, V_{LE}		$T_A = T_{MIN}$ to T_{MAX}			2.4	V
Logic Low Threshold	V_{ADD_H}, V_{EN_H}, V_{LE}		$T_A = T_{MIN}$ to T_{MAX}	0.8			
Input Current with Input Voltage High	I_{ADD_H}, I_{EN_H}, I_{LE}	V_{ADD_H} = 2.4V, V_{ADD_L} = 0.8V		–0.1	0.01	0.1	µA
Input Current with Input Voltage Low	I_{ADD_L}, I_{EN_L}, I_{LE}	V_{ADD_H} = 2.4V, V_{ADD_L} = 0.8V					
Supply							
Power Supply Range	V+, V–			±2.0		±6	V
Positive Supply Current	I+	$V_{EN} = V_{ADD\_} = V_{LE}$ = 0V/V+, V+ = 5.5V, V– = –5.5V	T_A = +25°C	–1	0.001	1	
			$T_A = T_{MIN}$ to T_{MAX}	–10		10	
Negative Supply Current	I–	$V_{EN} = V_{ADD\_} = V_{LE}$ = 0V/V+, V+ = 5.5V, V– = –5.5V	T_A = +25°C	–1	0.001	1	
			$T_A = T_{MIN}$ to T_{MAX}	–10		10	
I_{GND} Supply Current	I_{GND}	$V_{EN} = V_{ADD\_} = V_{LE}$ = 0V/V+, V+ = 5.5V, V– = –5.5V	T_A = +25°C	–1	0.01	1	
			$T_A = T_{MIN}$ to T_{MAX}	–10		10	
Dynamic							
Transition Time	t_{TRANS}	Figure 1	T_A = +25°C		60	150	ns
			$T_A = T_{MIN}$ to T_{MAX}			250	
Break-Before-Make Interval	t_{BBM}	Figure 3	T_A = +25°C	4	10		
Enable Turn-On Time	$t_{ON(EN)}$	Figure 2	T_A = +25°C		10	150	
			$T_A = T_{MIN}$ to T_{MAX}			250	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 2	T_A = +25°C		40	100	
			$T_A = T_{MIN}$ to T_{MAX}			150	
Setup Time, Channel Select to Latch Enable	t_S	Figure 4	T_A = +25°C	50			
			$T_A = T_{MIN}$ to T_{MAX}	60			
Hold Time,Latch Enable to Channel Select	t_H	Figure 6	T_A = +25°C	0			
			$T_A = T_{MIN}$ to T_{MAX}	0			
Pulse Width Latch Enable	t_{MPW}	Figure 5	T_A = +25°C	60			
			$T_A = T_{MIN}$ to T_{MAX}	70			
Charge Injection(3)	Q		T_A = +25°C		1.5	5	pC
Off Isolation(7)	V_{ISO}	V_{EN2} = 0V, R_L = 1kOhm f = 1 MHz			–65		dB
Crosstalk Between Channels	V_{CT}	V_{EN1} = 0V, R_{EN2} = 2.4V, f = 1 MHz, V_{GEN} = 1Vp-p, R_L = 1kOhm			–92		

Electrical Specifications - Dual Supplies (continued)

(V+ = +5V ±10%, V– = –5V ±10%, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{LE}$ = 2.4V, $V_{ADD\_L} = V_{EN\_L}$ = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Symbol	Conditions			Min(2)	Typ(2)	Max(2)	Units
Distortion, THD						0.025		
Logic Input Capacitance	C_{IN}	f = 1 MHz				3		
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1 MHz, $V_{EN} = V_{COM}$ = 0V				3		
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1 MHz, $V_{EN2} = V_{COM}$ = 0V	PS4530	T_A = +25°C		15		pF
			PS4531			9		
			PS4532			6		
COM-On Capacitance	$C_{COM(ON)}$	f = 1 MHz, $V_{EN1} = V_{COM}$ = 0V, V_{EN2} = 2.4V	PS4530			26		
			PS4531			20		
			PS4532			17		

Electrical Characteristics - Single 5V Supply

(V+ = +5V ±10%, V– = –0V, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{LE}$ = 2.4V, $V_{ADD\_L} = V_{EN\_L}$ = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Symbol	Conditions			Min(2)	Typ(2)	Max(2)	Units
Switch								
Analog Signal Range	V_{COM} , V_{NO}	Note(3)			0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		T_A = +25°C		25	65	Ohm
				$T_A = T_{MIN}$ to T_{MAX}			75	
On-Resistance Matching Between Channels (3,4)	ΔR_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		T_A = +25°C		1	8	
				$T_A = T_{MIN}$ to T_{MAX}			12	
On-Resistance Flatness	R_{FLAT}	I_{NO} = 1mA, V_{COM} = 3V,2/V,1V, V+ = 4.5V		T_A = +25°C		4		
NO-Off Leakage Current (8)	$I_{NO(OFF)}$	V_{NO} = 4.5V, V_{COM} = 4.5V, 1V, V+ = 4.5V		T_A = +25°C	–80		80	nA
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
COM-Off Leakage Current (8)	$I_{COM(OFF)}$	V_{COM} = 4.5V, 1V; V_{NO} = 1V, 4.5V; V+ = 5.5V	PS4530	T_A = +25°C	–80		80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
			PS453, PS4532	T_A = +25°C	–80		80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
COM-On Leakage Current (8)	$I_{COM(ON)}$		PS4530	T_A = +25°C	–80		80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	
			PS4531, PS4532	T_A = +25°C	–80		80	
				$T_A = T_{MIN}$ to T_{MAX}	–100		100	

Electrical Characteristics - Single 5V Supply

(V+ = +5V ±10%, V– = –0V, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{LE} = 2.4V$, $V_{ADD\_L} = V_{EN\_L} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Symbol	Conditions		Min(2)	Typ(2)	Max(2)	Units
Digital Logic Input							
Logic-High Threshold	V_{ADD_H}, V_{EN_H}, V_{LE}		$T_A = T_{MIN}$ to T_{MAX}			2.4	V
Logic-Low Threshold	V_{ADD_L}, V_{EN_L}, V_{LE}			0.8			
Input Current with Input Voltage High	I_{ADD_H}, I_{EN_H}, I_{LE}	$V_H = 2.4V$, $V_L = 0.8V$		–0.1		0.1	µA
Input Current with Input Voltage Low	I_{ADD_L}, I_{EN_L}, I_{LE}						
Supply							
Positive-Supply Range				2.0		12	V
Positive-Supply Current	I+	$V_{EN\_} = V_{ADD} = V_{LE} = 0V$, V+; V+ = 5.5V; V– = 0V	T_A = +25°C	–1.0		1.0	µA
			$T_A = T_{MIN}$ to T_{MAX}	–10		10	
Negative-Supply Current	I–		T_A = +25°C	–1.0		1.0	
			$T_A = T_{MIN}$ to T_{MAX}	–10		10	
I_{GND} Supply Current	I_{GND}		T_A = +25°C	–1.0		1.0	
			$T_A = T_{MIN}$ to T_{MAX}	–10		10	
Dynamic							
Transition Time	t_{TRANS}	Figure 1, V_{NO} =3V	T_A = +25°C		90	200	ns
			$T_A = T_{MIN}$ to T_{MAX}			250	
Break-Before-Make Interval	t_{BBM}	Figure 3 (3)	T_A = +25°C	10	20		
Enable Turn-On Time(3)	$t_{ON(EN)}$	Figure 2	T_A = +25°C		100	200	
			$T_A = T_{MIN}$ to T_{MAX}			250	
Enable Turn-Off Time(3)	$t_{OFF(EN)}$	Figure 3	T_A = +25°C		40	100	
			$T_A = T_{MIN}$ to T_{MAX}			125	
Set-Up Time, Channel Select to Latch Enable	t_S	Figure 7	T_A = +25°C	50			
			$T_A = T_{MIN}$ to T_{MAX}	60			
Hold Time, Latch Enable to Channel Select	t_H		T_A = +25°C	0			
			$T_A = T_{MIN}$ to T_{MAX}	0			
Pulse Width, Latch Enable	t_{MPW}		T_A = +25°C	60			
			$T_A = T_{MIN}$ to T_{MAX}	70			
Charge Injection(3)	Q	Figure 7, $C_L = 1nF$, $V_{NO} = 0V$	T_A = +25°C		1.5	5	pC

Electrical Characteristics - Single 3V Supply

(V+ = +2.7V to 3.6V, V– = –0V, GND = 0V, $V_{ADD\_H} = V_{EN\_H} = V_{LE} = 2.4V$, $V_{ADD\_L} = V_{EN\_L} = 0.5V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Symbol	Conditions		Min(2)	Typ(2)	Max(2)	Units
Switch							
Analog Signal Rnage	V_{ANALOG}	Note 3		0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 1.5V V+ = 2.7V	T_A = +25°C		75	185	Ohm
			$T_A = T_{MIN}$ to T_{MAX}			250	
Dynamic							
Transistion Time(3)	t_{TRANS}	Figure 1, V_{IN} = 2.4V V_{NO1} = 1.5V, V_{NO8} = 0V	T_A = +25°C		150	350	ns
Enable Turn-On Time(3)	$t_{ON(EN)}$	Figure 3, V_{INH} = 2.4V V_{INL} = 0V, V_{NO1} = 1.5V			150	350	
Enable Turn-Off Time(3)	$t_{OFF(EN)}$	Figure 3, V_{INH} = 2.4V V_{INL} = 0V, V_{NO1} = 1.5V			60	150	
Set-Up Time, Channel Select to Latch Enable	t_S	Note 3		100			
Hold Time, Latch Enable to Channel Select	t_H			0			
Pulse Width, Latch Enable	t_{MPW}			120			

Notes:

2. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ (max) - R_{ON} (min)
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog ranges, i.e., VNO = 3V to 0V and 0V to –3V.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at T_A = +25ºC.
7. Worst-case isolation is on channel 4 because of its proximity to the COM pin.
   Off isolation = 20log V_{COM}/V_{NO}, V_{COM} = output, V_{NO} = input to off switch
8. Leakage testing at single supply is guaranteed by testing with dual supplies.

Applications Information

Power-Supply Considerations

Overview

The PS4530/PS4531/PS4532 construction is typical of most CMOS analog Switches. They have three supply pins: V+, V, and GND. V+ and V- drive the the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any signal exceeds V+ or V-. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V+ or V–.

Virtually all of the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pine are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages to the V+ and V– pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. For this reason, both sides of a given switch can show leakage currents of either the same or opposite polarity.

The signal paths and GND are not connected.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic level translators convert the logic levels into switched V+ and V- signals to drive the analog signals' gates. This drive signal is the only connection between the logic supplies and signals and the analog supplies. V+ and V- have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V+ = +5V. As V+ rises, the threshold increases slightly, so when V+ reaches +12V, the threshold is about 3.1V – above the TTL guaranteed, high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The PS4530/PS4531/PS4532 operate with bipolar supplies between ±2.0V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the +13V absolute maximum rating.

Single Supply

The PS4530/PS4531/PS4532 operate from a single supply between +2V and 12V when V- is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually work with a single supply at, near, or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

High-Frequency Performance

In 50Ohm systerns, signal response is reasonably flat up to 50MHz (see Typical Operating Characteristics). Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on, but in turning it off. The off-state switch acts lilke a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about –65dB in 50Ohm systems, becoming worse (approximately 21dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Test Circuits/Timing Diagrams

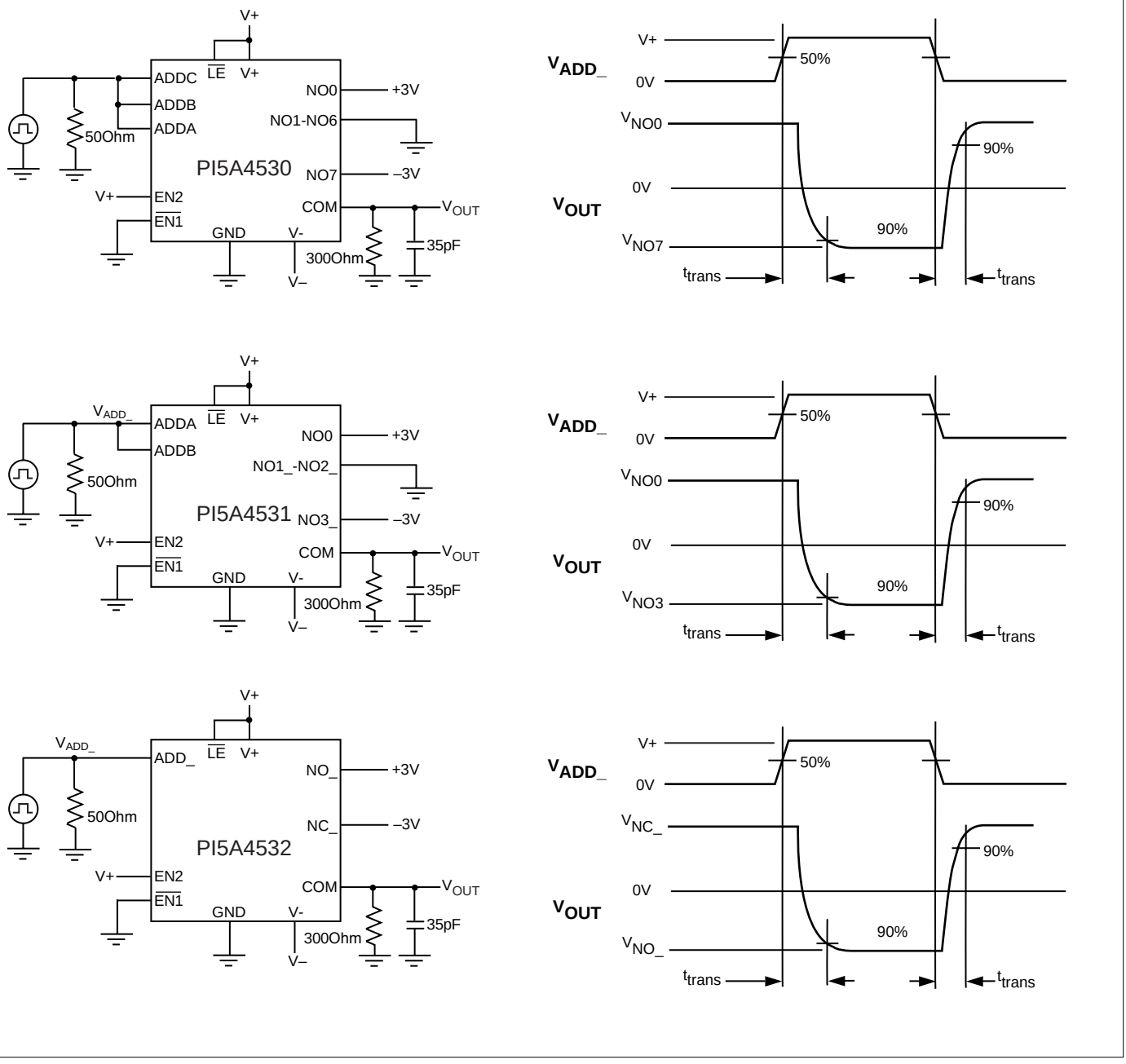
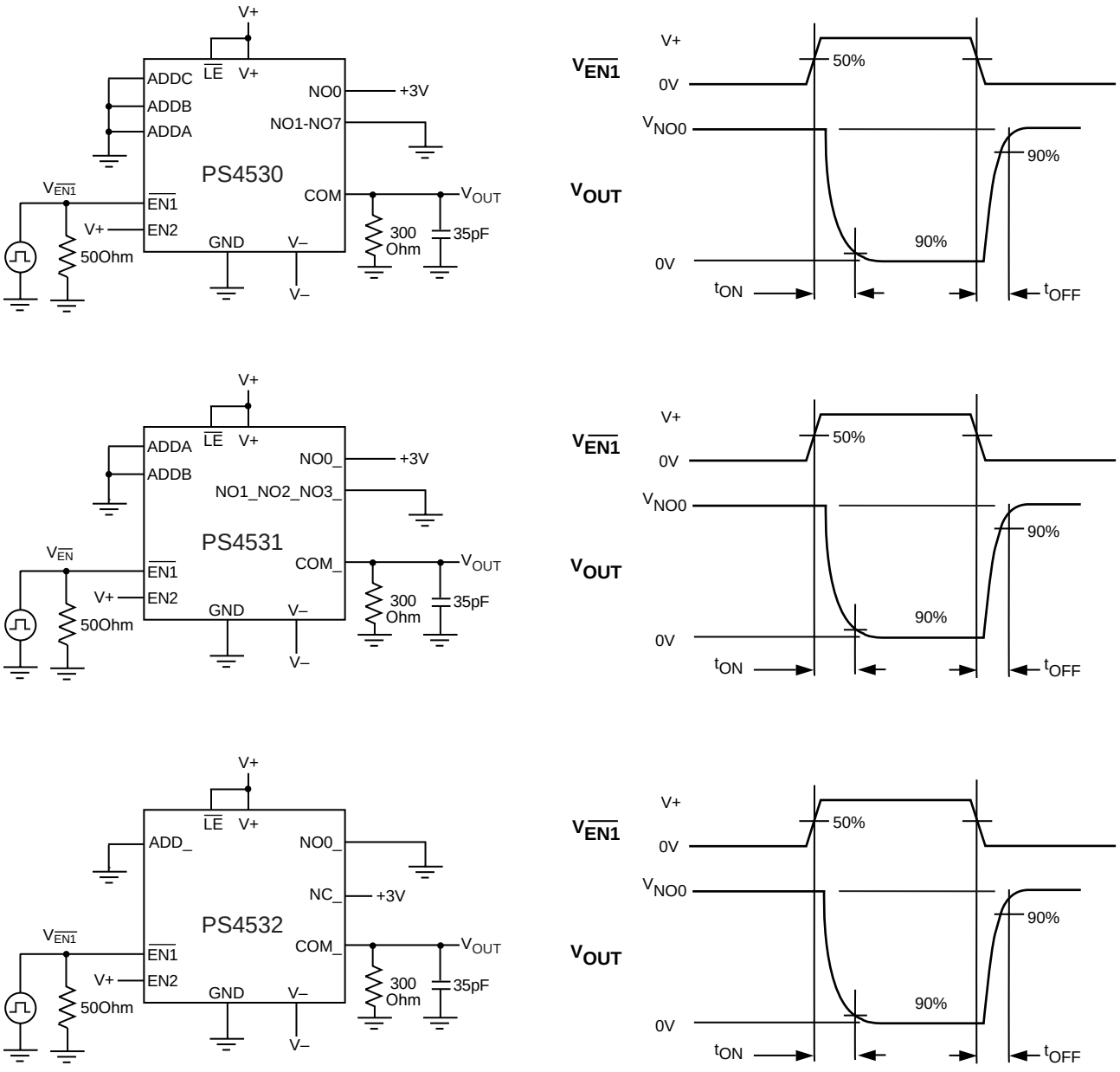


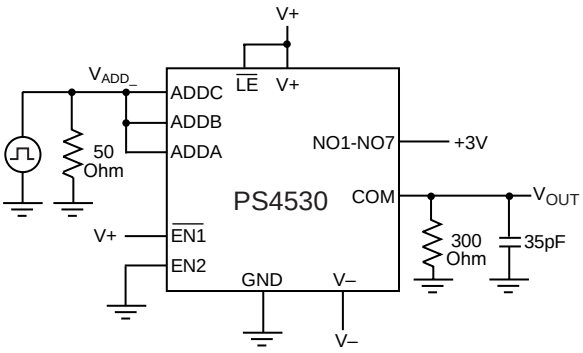
Figure 1. Address Transition Time

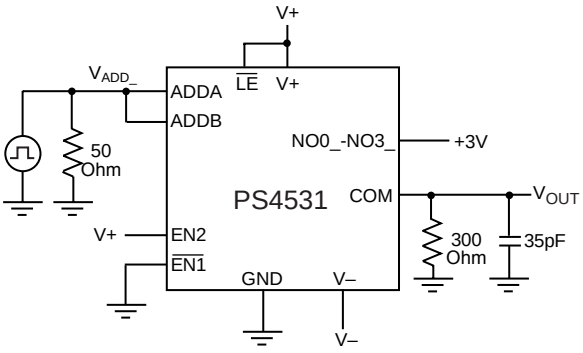
Test Circuits/Timing Diagrams(continued)

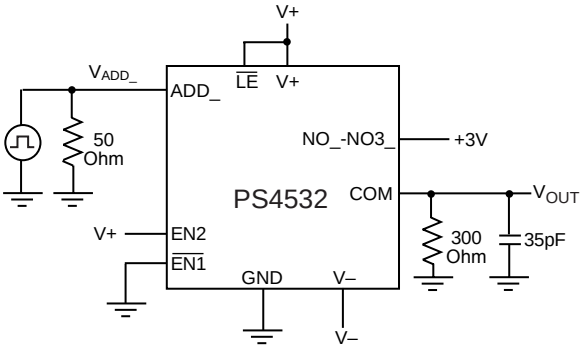


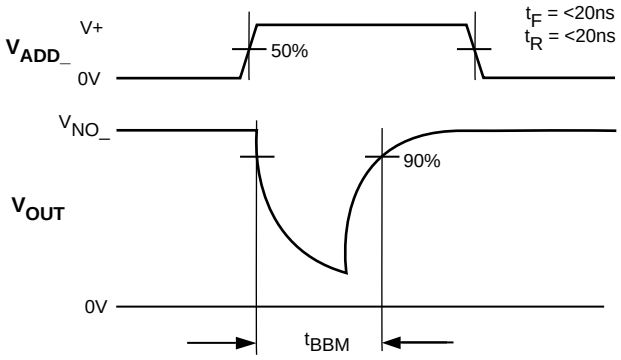
V– = 0V for Single-Supply Operation.
Repeat Test for Each Section
Repeat Test for EN2, with Pulse Inverted and EN1 Connected to GND.

Figure 2. Enable Switching Time



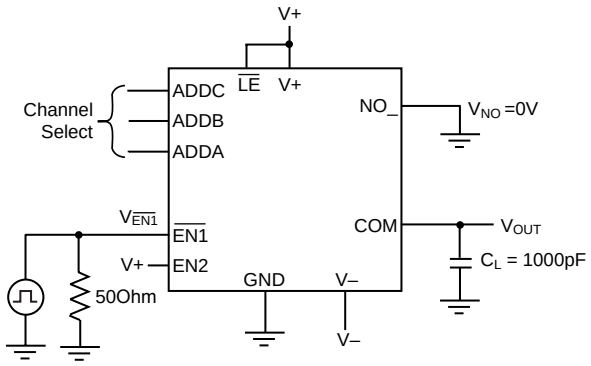




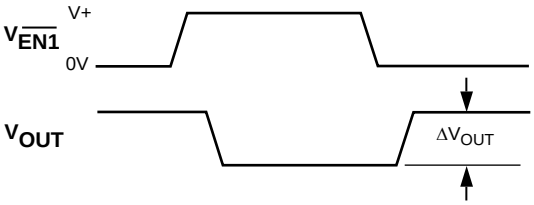


V– = 0V for Single-Supply Operation.
Repeat Test for Each Section

Figure 3. Break-Before-Make Interval

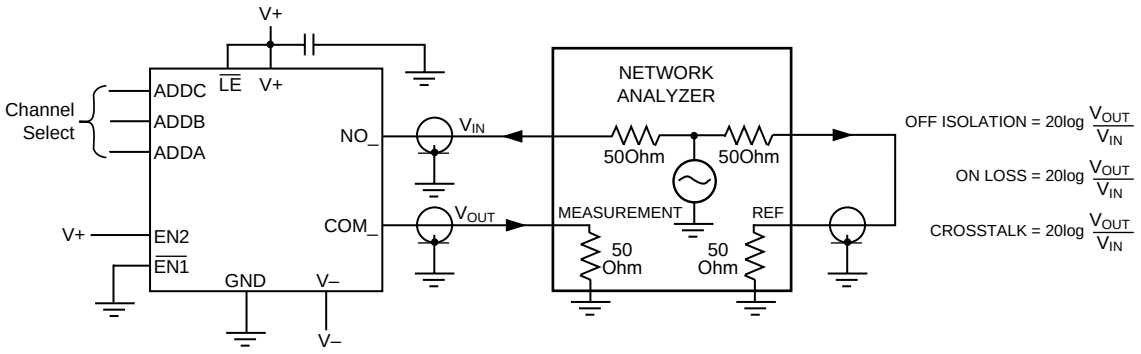


V– = 0V for single-supply operation.
Repeat test for each section.



ΔV_{OUT} is the measured voltage resulting from charge-transfer error Q when the channel turns off.
$Q = \Delta V_{OUT} \times C_L$

Figure 4. Charge Injection



Measurements are standardized against short at socket terminals.
Off isolation is measured between COM_ and OFF NO_ terminal on each switch.
On loss is measured between COM_ and ON terminal on each switch.
Crosstalk (PS4531/PS4532) is measured from one channel (A,B,C) to all other channels.
Signal direction through switch is reversed; worst values are recorded.

Figure 5. Off Isolation, On Loss, and Crosstalk

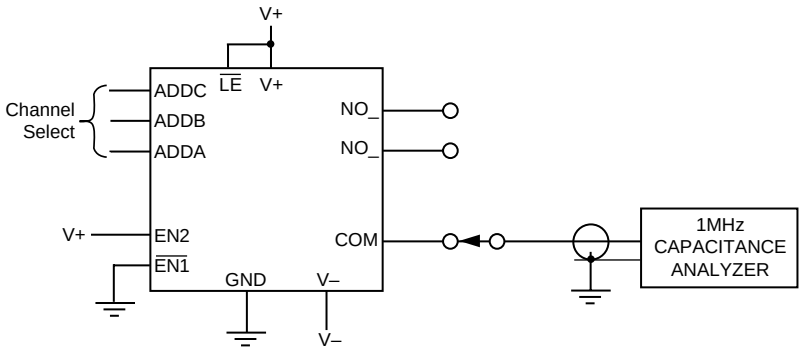
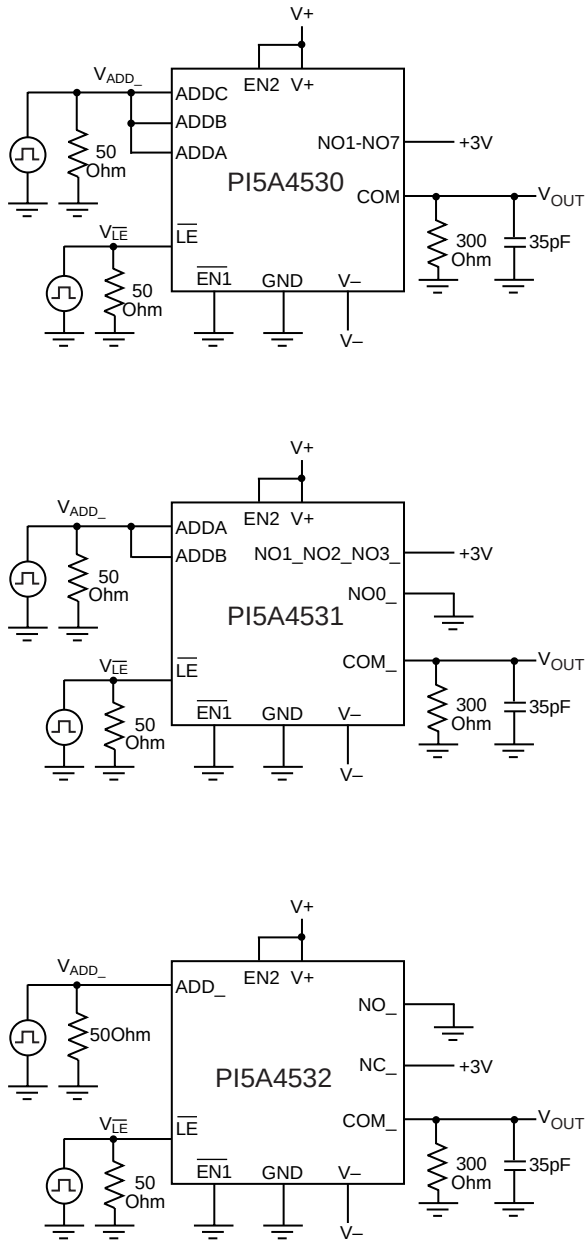
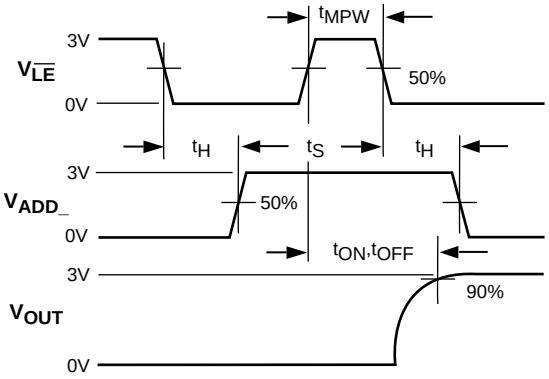


Figure 6. NO/COM Capacitance

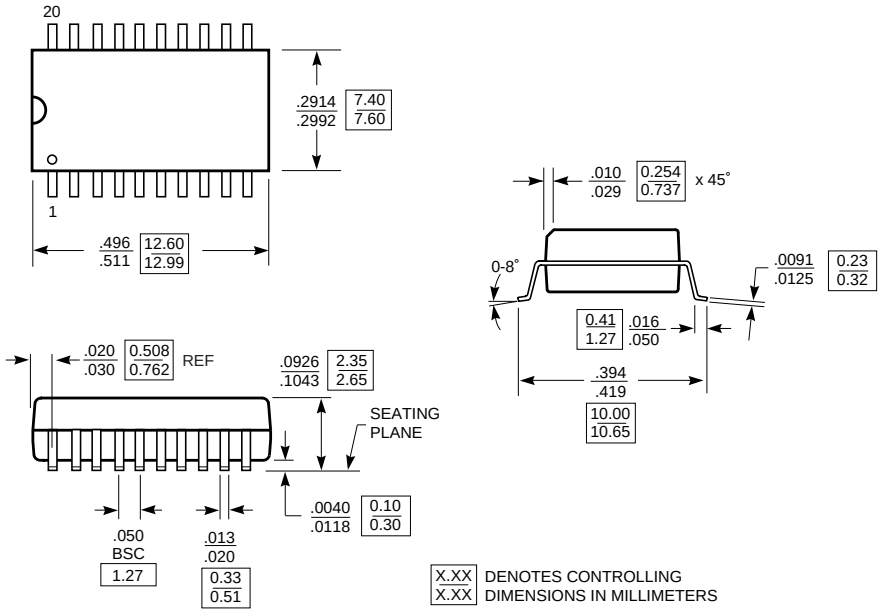




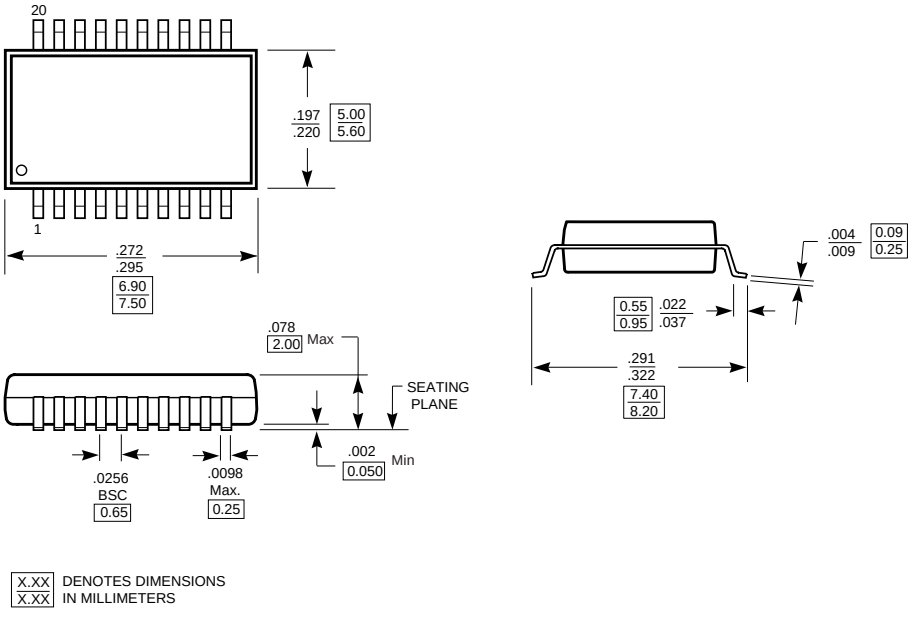
V– = 0V for Single-Supply Operation.
Repeat Test for Each Section

Figure 7. Setup and Hold Times, Minimum $\overline{LE}$ Width

Packaging Mechanical: 20-pin SOIC (S)



Packaging Mechanical: 20-pin SSOP (H)



Ordering Information

Ordering Code	Packaging Code	Package Type
PS4530CWP	S	20-pin SOIC
PS4530CAP	H	20-pin SSOP
PS4530EWP	S	20-pin SOIC
PS4530EAP	H	20-pin SSOP
PS4531CWP	S	20-pin SOIC
PS4531CAP	H	20-pin SSOP
PS4531EWP	S	20-pin SOIC
PS4531EAP	H	20-pin SSOP
PS4532EWP	S	20-pin SOIC

Notes:
1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/mechanicals.php