- **Hot Plug Protection**
- **1.6 to 2.5 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **High-Performance 64-Pin VQFP Thermally Enhanced Package (PowerPAD™)**
- **2.5 V Power Supply for Low Power Operation**
- **Programmable Voltage Output Swing on Serial Output**
- **Interfaces to Backplane, Copper Cables, or Optical Converters**
- **Rated for Industrial Temperature Range**
- **On-Chip 8-Bit/10-Bit (8B/10B) Encoding/Decoding, Comma Alignment, and Link Synchronization**
- **On-Chip PLL Provides Clock Synthesis From Low-Speed Reference**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **Typical Power: 325 mW**
- **Loss of Signal (LOS) Detection**
- **Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link**

## description

The PCI6060 is a serial PCI transceiver, intended for use in the PCI6050 symmetric serialized PCI-PCI bridge. The PCI6050 bridge provides a high-performance solution for connecting two PCI buses via an ultrahigh-speed bidirectional cable medium. The PCI6060 supports an effective serial interface speed of 1.6 Gbps to 2.5 Gbps providing up to 2.0 Gbps of data bandwidth. The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over controlled impedance media of approximately 50 Ω. The transmission media can be printed-circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel, which can be a coaxial copper cable, a controlled impedance backplane, or an optical link. It is then reconstructed into its original parallel format. It offers significant power and cost savings over current solutions, as well as scalability for higher data rate in the future.

The PCI6060 performs data conversion parallel-to-serial and serial-to-parallel. The clock extraction functions as a physical layer interface device. The serial transceiver interface operates at a maximum speed of 2.5 Gbps. The transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (GTX_CLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8B/10B) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (GTX_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the extracted reference clock (RX_CLK). It then decodes the 20 bit wide data using 8-bit/10-bit decoding format resulting in 16 bits of parallel data at the receive data terminals (RXD0-15). The outcome is an effective data payload of 1.28 Gbps to 2.0 Gbps (16 bits data x the GTX_CLK frequency).

The PCI6060 is housed in a high performance, thermally enhanced, 64-pin PQFP PowerPAD™ package. Use of the PowerPAD™ package does not require any special considerations except to note that the PowerPAD™, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. It is recommended that the PCI6060 PowerPAD™ be soldered to the thermal land on the board. All ac performance specifications in this data sheet are measured with the PowerPAD™ soldered to the test board.

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

## description (continued)

The PCI6060 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer, allowing the protocol device a functional self-check of the physical interface.

The PCI6060 is designed to be hot plug capable. An on-chip power-on reset circuit holds the RX_CLK low and goes to high impedance to the parallel side output signal terminals during power up as well as goes to DOUTTXP and DOUTTXN.

The PCI6060 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage amplitude to keep the clock recovery circuit in lock.

To prevent a data bit error from causing a valid data packet from being interpreted as a comma and thus causing the erroneous word alignment by the comma detection circuit, the comma word alignment circuit is turned off after the link is properly established in PCI6060.

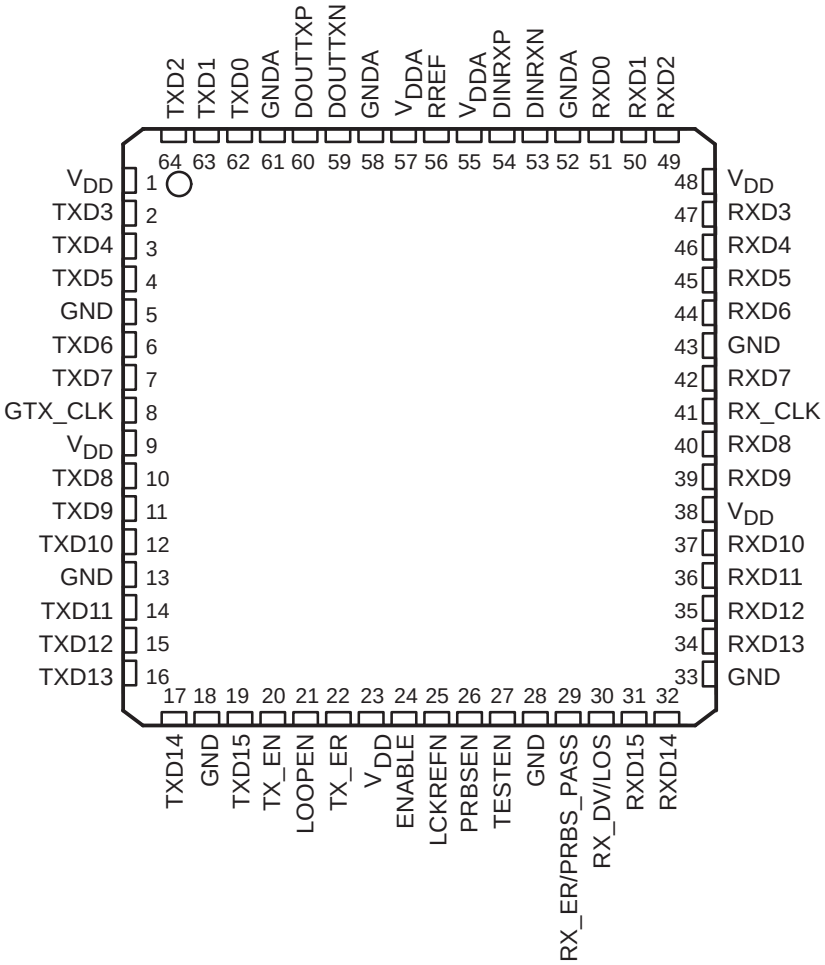
The PCI6060 allows users to implement redundant ports by connecting receive data bus terminals from two PCI6060 devices together. Asserting the LCKREFN to go to a low state will cause the receive data bus terminals, RXD[0:15], RX_CLK and RX_ER, RX_DV/LOS to go to a high impedance state. This places the device in a transmit only mode since the receiver is not tracking the data.

The PCI6060 uses a 2.5-V supply. The I/O section is 3 V compatible. With the 2.5-V supply the chipset is very power-efficient, consuming less than 325 mW typically. The PCI6060 is characterized for operation from –40°C to 85°C.

**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE |
|---|---|
| | **PowerPAD™ QUAD FLATPACK (PQFP)** |
| –40°C to 85°C | PCI6060IRCP |

**RCP PACKAGE**
**(TOP VIEW)**




PRODUCT PREVIEW

PRODUCT PREVIEW

## block diagram

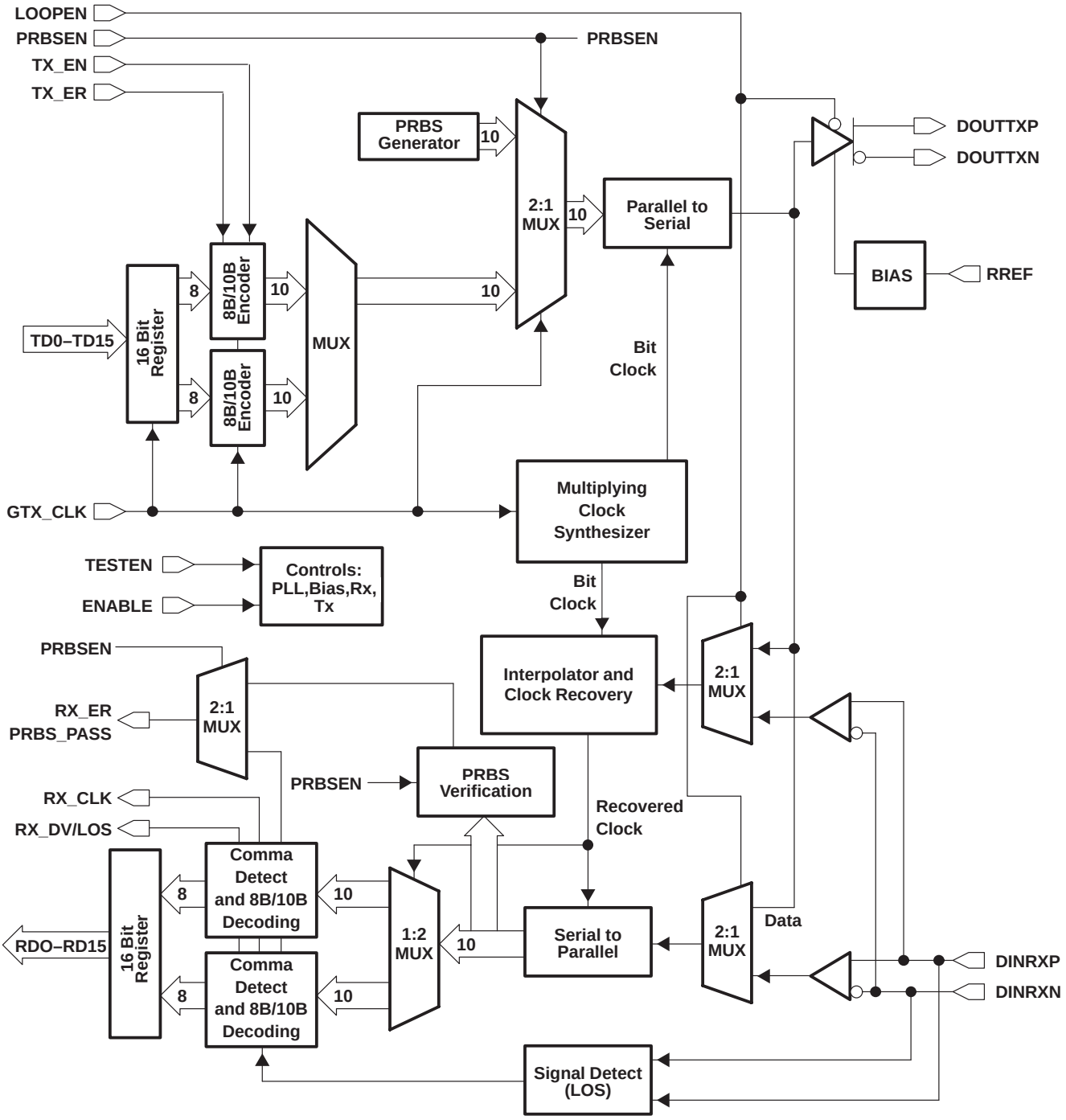



**Figure 1. PCI6060 Block Diagram**

## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| DINRXN<br>DINRXP | 53<br>54 | I | Serial receive inputs. DINRXP and DINRXN together are the differential serial input interface from a copper or an optical I/F module. |
| DOUTTXN<br>DOUTTXP | 59<br>60 | O | Serial transmit outputs (Hi-Z on power up). DOUTTXP and DOUTTXN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the GTX_CLK value. DOUTTXP and DOUTTXN are put in a high impedance state when LOOPEN is high and are active when LOOPEN is low. During power-on reset these terminals are high impedance. |
| ENABLE | 24 | I | Device enable (w/pullup). When this terminal is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When asserted high while the device is in power-down mode, the transceiver will go into power-on reset before beginning normal operation. |
| GND | 5, 13, 18, 28, 33, 43 | | Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers. |
| GNDA | 52, 58, 61 | | Analog ground. GNDA provides a ground reference for the high-speed analog circuits, RX and TX. |
| GTX_CLK | 8 | I | Reference clock. GTX_CLK is a continuous external input clock that synchronizes the transmitter interface signals TX_EN, TX_ER and TXD. The frequency range of GTX_CLK is 80 MHz to 125 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data (TXD) for serialization. |
| LCKREFN | 25 | I | Lock to reference (w/pullup). When LCKREFN is low, the receiver clock is frequency locked to GTX_CLK. This places the device in a transmit only mode since the receiver is not tracking the data. When LCKREFN is asserted low, the receive data bus terminals, RXD[0:15], RX_CLK and RX_ER, RX_DV/LOS are in a high-impedance state.<br>When LCKREFN is deasserted high, the receiver is locked to the received data stream and must receive valid codes from the synchronization state machine before the transmitter is enabled. |
| LOOPEN | 21 | I | Loop enable (w/pulldown). When LOOPEN is active high, the internal loop-back path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTXP and DOUTTXN outputs are held in a high-impedance state during the loop-back test. LOOPEN is held low during standard operational state with external serial outputs and inputs active. |
| PRBSEN | 26 | I | PRBS test enable (w/pulldown). When asserted high results of pseudorandom bit stream (PRBS) tests can be monitored on the RX_ER/PRBS_PASS terminal. A high on PRBS_PASS indicates that valid PRBS is being received. |
| RREF | 56 | I | Reference resistor. The RREF terminal is used to connect to an external reference resistor. The other side of the resistor is connected to analog $V_{DD}$. The resistor is used to provide an accurate current reference to the transmitter and receiver I/O circuitry. |
| RXD0<br>RXD1<br>RXD2<br>RXD3<br>RXD4<br>RXD5<br>RXD6<br>RXD7<br>RXD8<br>RXD9<br>RXD10<br>RXD11<br>RXD12<br>RXD13<br>RXD14<br>RXD15 | 51<br>50<br>49<br>47<br>46<br>45<br>44<br>42<br>40<br>39<br>37<br>36<br>35<br>34<br>32<br>31 | O | Receive data bus (Hi-Z on power up). These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to RX_CLK. The data is valid on the rising edge of RX_CLK as shown in Figure 11. These terminals are in high-impedance state during power-on reset. |

PRODUCT PREVIEW

## Terminal Functions (Continued)

| TERMINAL NAME | TERMINAL NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| RX_CLK | 41 | O | Recovered clock (low on power up). Output clock that is synchronized to RXD, RX_ER, RX_DV/LOS. RX_CLK is the recovered serial data rate clock divided by 20. RX_CLK is held low during power-on reset. |
| RX_ER/ PRBS_PASS | 29 | O | Receive error (Hi-Z on power up). When RX_ER and RX_DV/LOS are asserted, indicates that an error was detected somewhere in the frame presently being output on the receive data bus. When RX_ER is asserted and RX_DV/LOS is deasserted, indicates that carrier extension data is being presented. RX_ER is in high impedance state during power-on reset.<br>When PRBSEN= low (deasserted), this terminal is used to indicate receive error (RX_ER). When PRBSEN = high (asserted), this terminal indicates status of the PRBS test results (High=pass). |
| RX_DV/LOS | 30 | O | Receive data valid (Hi-Z on power up). RX_DV/LOS is output by the transceiver to indicate that recovered and decoded data is being output on the receive data bus. RX_DV/LOS shall be asserted low continuously from the first recovered word of the frame through the final recovered word and shall be negated prior to the first rising edge of RX_CLK that follows the final word. RX_DV/LOS is in high-impedance state during power-on reset.<br>If, during normal operation, the differential signal amplitude on the serial receive terminals is below 200 mV, RX_DV/LOS is asserted high along with RX_ER and the receive data bus to indicate a loss of signal condition. If the device is in power-down mode, RX_DV/LOS is the output of the signal detect circuit and will be asserted low when a loss of signal condition is detected. |
| TESTEN | 27 | I | Test mode enable (w/pulldown). This terminal should be left unconnected or tied low. |
| TXD0<br>TXD1<br>TXD2<br>TXD3<br>TXD4<br>TXD5<br>TXD6<br>TXD7<br>TXD8<br>TXD9<br>TXD10<br>TXD11<br>TXD12<br>TXD13<br>TXD14<br>TXD15 | 62<br>63<br>64<br>2<br>3<br>4<br>6<br>7<br>10<br>11<br>12<br>14<br>15<br>16<br>17<br>19 | I | Transmit data bus. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of GTX_CLK as shown in Figure 10. |
| TX_EN | 20 | I | Transmit enable (w/pulldown). TX_EN in combination with TX_ER indicates the protocol device is presenting data on the transmit data bus for transmission. TX_EN shall be high with the first word of the preamble and remain asserted while all words to be transmitted are presented on the receive data bus. TX_EN is negated prior to the first rising edge of GTX_CLK following the final word of a frame. |
| TX_ER | 22 | I | Transmit error coding (w/pulldown). When TX_ER and TX_EN are high, indicates that the transceiver will generate an error somewhere in the frame presently being transferred. When TX_ER is asserted and TX_EN is deasserted, indicates the protocol device is presenting carrier extension data. When TX_ER is deasserted with TX_EN asserted, indicates that normal data is being presented. |
| $V_{DD}$ | 1, 9, 23, 38, 48 | | Digital logic power. Provides power for all digital circuitry and digital I/O buffers. |
| $V_{DDA}$ | 55, 57 | | Analog power. $V_{DDA}$ provides a supply reference for the high-speed analog circuits, receiver and transmitter |

## detailed description

### transmit interface

The transmitter portion registers valid incoming 16-bit wide data (TXD[0:15]) on the rising edge of the GTX_CLK. The data is then 8-bit/10-bit encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (GTX_CLK) by a factor of 10 times, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (D0) first. The transmitter also inserts commas at the beginning of the transmission for byte synchronization.

### transmit data bus

The transmit bus interface accepts 16-bit wide single-ended TTL parallel data at the TXD[0:15] terminals. Data is valid on the rising edge of the GTX_CLK when the TX_EN is asserted high and the TX_ER is deasserted low. The GTX_CLK is used as the word clock. The data, enable, and clock signals must be properly aligned as shown in Figure 2. Detailed timing information can be found in the electrical characteristics table**.**

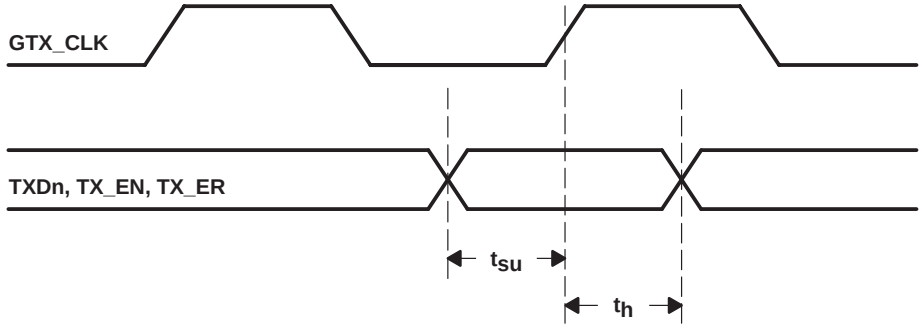



**Figure 2. Transmit Timing Waveform**

## detailed description (continued)

### transmission latency

The data transmission latency of the PCI6060 is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay will vary slightly. The minimum transmit latency ($T_{latency}$) is 34 bit times; the maximum is 38 bit times. Figure 3 illustrates the timing relationship between the transmit data bus, the GTX_CLK and serial transmit terminals.

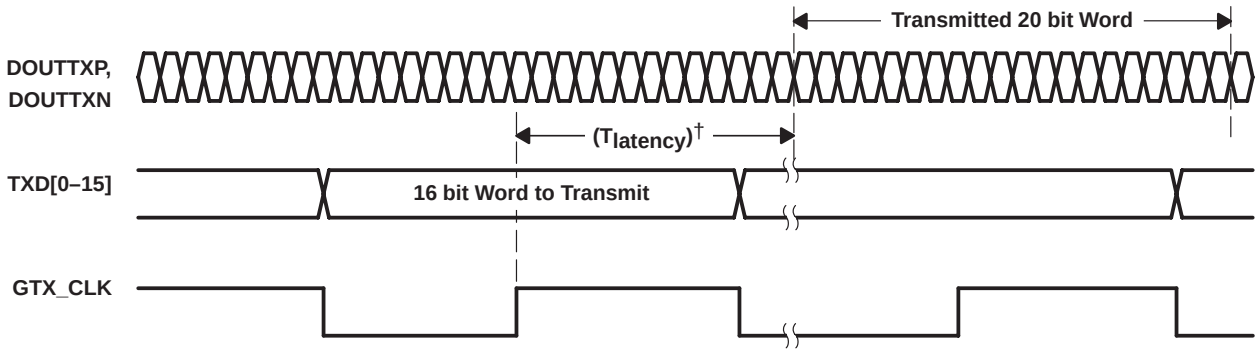



**Figure 3. Transmitter Latency**

† Non-Jedec symbol

### 8-bit/10-bit encoder

All true serial interfaces require a method of encoding to insure minimum transition density so that the receiving PLL has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The PCI6060 uses the 8-bit/10-bit encoding algorithm that is used by fibre channel and the gigabit ethernet. This is transparent to the user, as the PCI6060 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-bit/10-bit encoder converts 8-bit wide data to a 10-bit wide encoded data character to improve its transmission characteristics. Since the PCI6060 is a 16-bit wide interface, the data is split into two 8-bit wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependant upon two additional input signals, the TX_EN and TX_ER. When the TX_EN is asserted and the TX_ER deasserted then the data bits TXD[0:15] are encoded and transmitted normally. When the TX_EN is deasserted, and TX_ER is asserted, then the encoder will generate a carrier extend consisting of two K23.7 (F7F7) codes. If the TX_EN and the TX_ER are both asserted, then the encoder will generate a K30.7 (FEFE) code. Table 1 provides the transmit data control decoding. Since the data is transmitted in 20-bit serial words, K codes indicating carrier extend and transmit error propagation are transmitted as two 10-bit K-codes.

**Table 1. Transmit Data Controls**

| TX_EN | TX_ER | ENCODED 20 BIT OUTPUT |
|---|---|---|
| 0 | 0 | IDLE (<K28.5, D5.6> or <K28.5, D16.2>) |
| 0 | 1 | Carrier extend (K23.7, K23.7) |
| 1 | 0 | Normal data character |
| 1 | 1 | Transmit error propagation (K30.7, K30.7) |

## detailed description (continued)

### IDLE insertion

The encoder inserts the IDLE character set when no payload data is available to be sent. IDLE consists of a K28.5 (BC) code and either a D5.6 (C5) or a D16.2 (50) character. The K28.5 character is defined by IEEE802.3z as a pattern consisting of 0011111010 ( a negative number beginning disparity) with the 7 MSBs (0011111) referred to as the comma character. Since data is latched into the PCI6060 16 bits at a time, this in turn is converted into two 10-bit codes that are transmitted sequentially. This means IDLE consists of two 10-bit codes, 20 bits wide, that are transmitted during a single GTX_CLK cycle.

### PRBS generator

The PCI6060 has a built-in $2^7$-1 PRBS (pseudorandom bit stream) function. When the PRBSEN terminal is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a BERT (bit error rate tester), the receiver of another PCI6060, or can be looped back to the receive input. Since the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

### parallel-to-serial

The parallel-to-serial shift register takes in the 20-bit wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the GTX_CLK input frequency. The LSB (D0) is transmitted first.

### high-speed data output

The high-speed data output driver consists of a current-mode logic (CML) differential pair that can be optimized for a particular transmission line impedance and length. The line can be directly-coupled or ac-coupled. Refer to Figure 15 and Figure 16 for termination details.

## receive interface

The receiver portion of the PCI6060 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit will lock to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10-bit decoded and output on a 16-bit wide parallel bus synchronized to the extracted receive clock.

### receive data bus

The receive bus interface drives 16-bit wide single-ended TTL parallel data at the RXD[0:15] terminals. Data is valid on the rising edge of the RX_CLK when the RX_DV/LOS is asserted high and the RX_ER is deasserted low. The RX_CLK is used as the recovered word clock. The data, enable, and clock signals are aligned as shown in Figure 4. Detailed timing information can be found in the switching characteristics table**.**

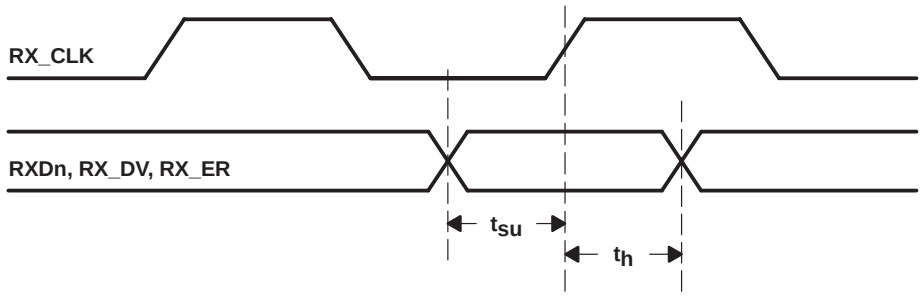



**Figure 4. Receive Timing Waveform**

PRODUCT PREVIEW

## detailed description (continued)

### data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output in the aligned parallel word with RXD0 received as first bit. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay will vary slightly. The minimum receive latency ($R_{latency}$) is 76 bit times; the maximum is 107 bit times. Figure 5 illustrates the timing relationship between the serial receive terminals, the recovered word clock (RX_CLK), and the receive data bus.

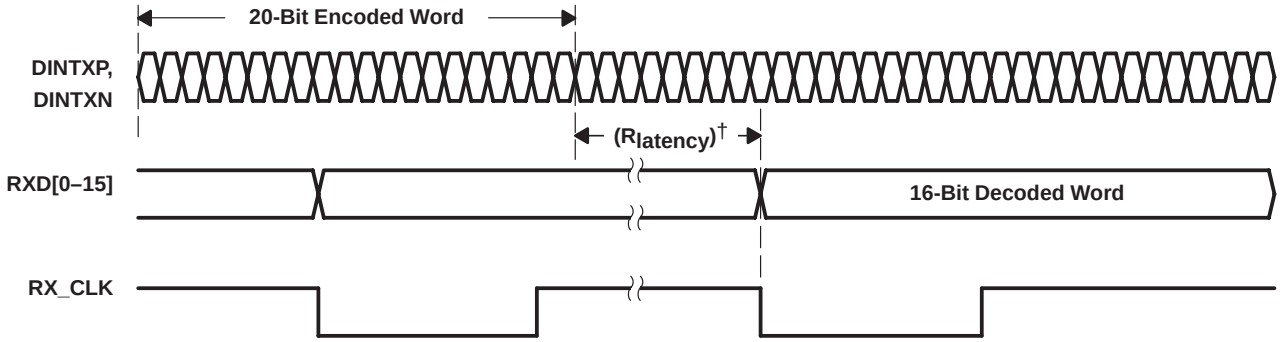



**Figure 5. Receiver Latency**

† Non-Jedec symbol

### serial-to-parallel

Serial data is received on the DINRXP and DINRXN terminals. The interpolator and clock recovery circuit will lock to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit wide parallel data is then multiplexed and fed into two separate 8-bit/10-bit decoders where the data is then synchronized to the incoming data steam word boundary by detection of the K28.5 synchronization pattern.

### comma detect and 8-bit/10-bit decoding

The PCI6060 has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10 bit encoded data (half of the 20 bit received word) back into 8-bits. The comma detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel to serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a way is needed to recognize the byte boundary. Generally this is accomplished through the use of a synchronization pattern. This is generally a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8-bit/10-bit encoding contains a character called the comma (b0011111 or b1100000), which is used by the comma detect circuit on the PCI6060 to align the received serial data back to its original byte boundary. The decoder detects the K28.5 comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data, removing the control words. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (RX_CLK) and output valid on the rising edge of the RX_CLK.

To prevent a data bit error from causing a valid data packet to be interpreted as a comma and thus cause the erroneous word alignment by the comma detection circuit, the comma word alignment circuit is turned off after receiving a properly aligned comma after the link is properly established. The link is established after three idle patterns or one valid data pattern is properly received. The comma alignment circuit is re-enabled when the synchronization state machine detects a loss of synchronization condition (see Synchronization and Initialization).

**comma detect and 8-bit/10-bit decoding (continued)**

Two output signals, RX_DV/LOS and RX_ER, are generated along with the decoded 16-bit data output on the RXD[0:15] terminals. The output status signals are asserted as shown in Table 2. When the PCI6060 decodes normal data and outputs the data on RXD[0:15], RX_DV/LOS is asserted (logic high) and RX_ER is deasserted (logic low). When the PCI6060 decodes a K23.7 code (F7F7) indicating carrier extend, RX_DV/LOS is deasserted and RX_ER is asserted. If the decoded data is not a valid 8-bit/10-bit code, an error is reported by the assertion of both RX_DV/LOS and RX_ER. If the error was due to an error propagation code, the RXD bits will output hex FEFE. If the error was due to an invalid pattern, the data output on RXD will be undefined. When the PCI6060 decodes an IDLE code, both RX_DV/LOS and RX_ER are deasserted and a K28.5 (BC) code followed by either a D5.6 (C5) or D16.2 (50) code are output on the RXD terminals.

**Table 2. Receive Status Signals**

| RECEIVED 20 BIT DATA | RX_DV/LOS | RX_ER |
|---|---|---|
| IDLE (<K28.5, D5.6>, <K28.5, D16.2>) | 0 | 0 |
| Carrier extend (K23.7, K23.7) | 0 | 1 |
| Normal data character (DX.Y) | 1 | 0 |
| Receive error propagation (K30.7, K30.7) | 1 | 1 |

**loss of signal detection**

The PCI6060 has a loss of signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is intended to be an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The PCI6060 reports this condition by asserting, the RX_DV/LOS, RX_ER and RXD[0:15] all to a high state. As long as the signal is above 200 mV in differential magnitude, the LOS circuit will not signal an error condition.

**synchronization and initialization**

The PCI6060 has a synchronization-state machine which is responsible for handling link initialization and synchronization. Upon power up or reset, the state machine enters the acquisition (ACQ) state and searches for IDLE. Upon receiving three consecutive IDLEs or a carrier extend, the state machine will enter the synchronization (SYNC) state. If, during the acquisition process, the state machine receives valid data or an error propagation code, it will immediately transition to the SYNC state. The SYNC state is the state for normal device transmission and reception. The initialization and synchronization state diagram is provided in Figure 6.

**synchronization and initialization (continued)**

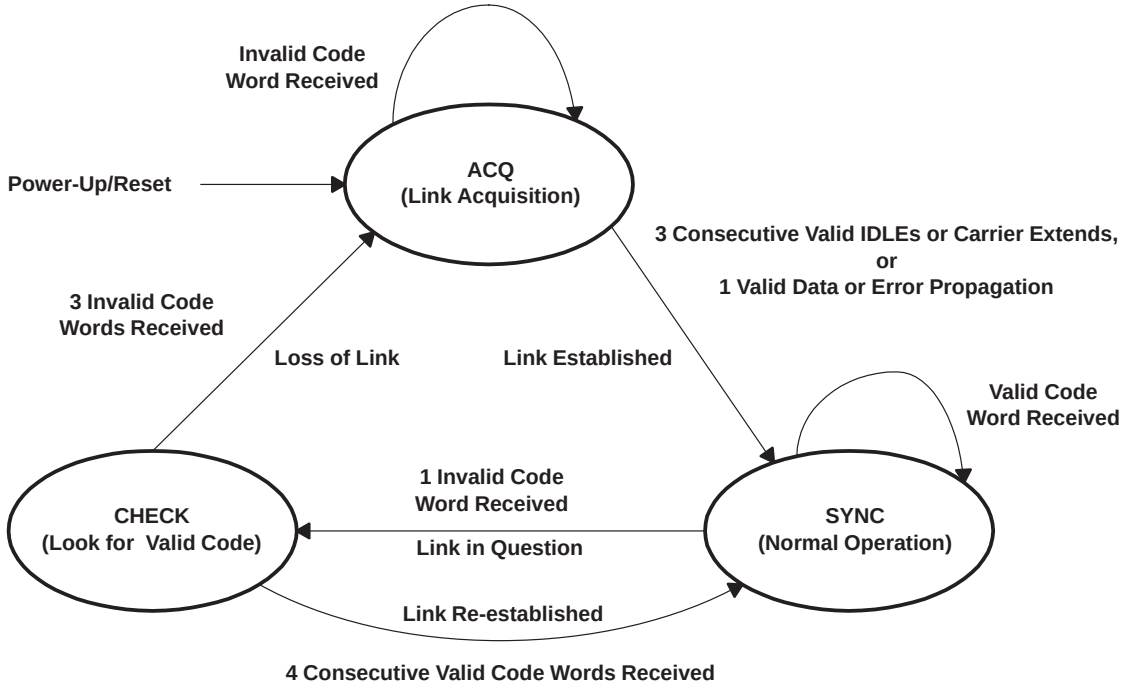



**Figure 6. Initialization and Synchronization State Diagram**

If during normal transmission and reception, an invalid code is received, the PCI6060 will notify the attached system or protocol device as described in comma detect and 8-bit/10-bit decoding. The synchronization state machine will transition to the CHECK state. The CHECK state will determine whether the invalid code received was caused by a spurious event or a loss of the link. If, in the CHECK state, the decoder sees 4 consecutive valid codes, the state machine will determine the link is good and transition back to the SYNC state for normal operation. If, in the CHECK state, the decoder sees 3 invalid codes (not required to be consecutive), the PCI6060 will determine a loss of the link has occurred and transition the synchronization-state machine back to the link-acquisition state (ACQ).

The state of the transmit data bus, control terminals, and serial outputs during the link acquisition process is illustrated in Figure 7.

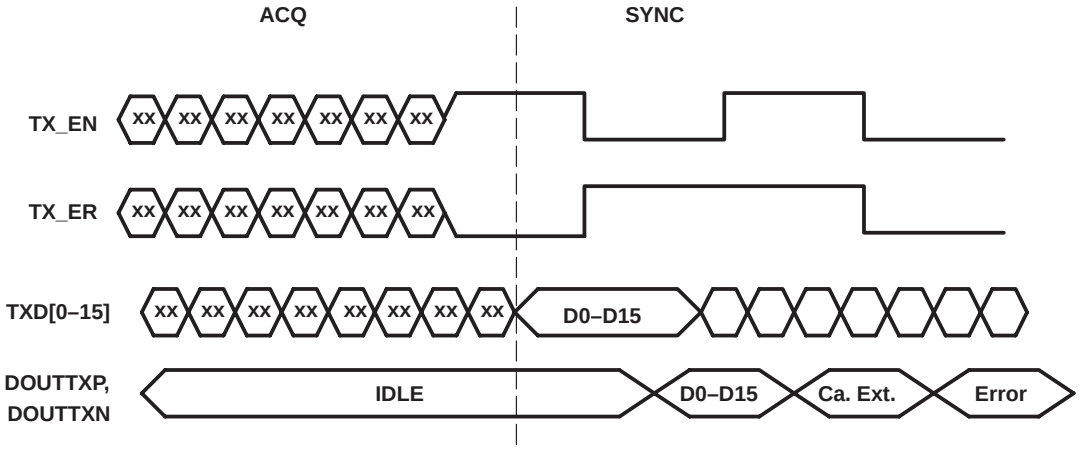



**Figure 7. Transmit Side Timing Diagram**

PRODUCT PREVIEW

**synchronization and initialization (continued)**

The state of the receive data bus, status terminals, and serial inputs during the link acquisition process is illustrated in Figure 8 and Figure 9.

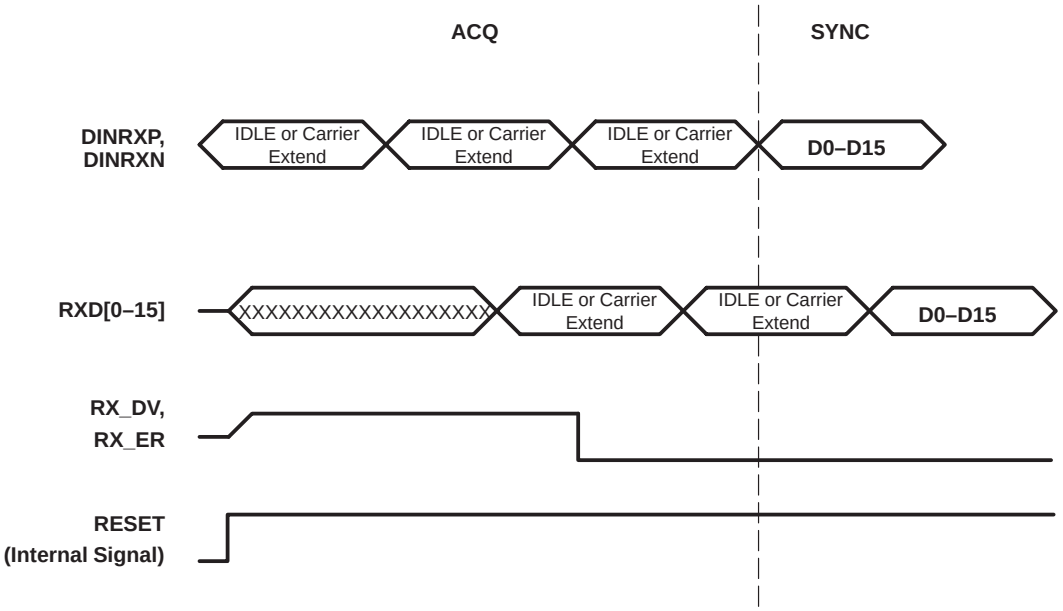



**Figure 8. Receive Side Timing Diagram (Idle or Carrier Extend)**

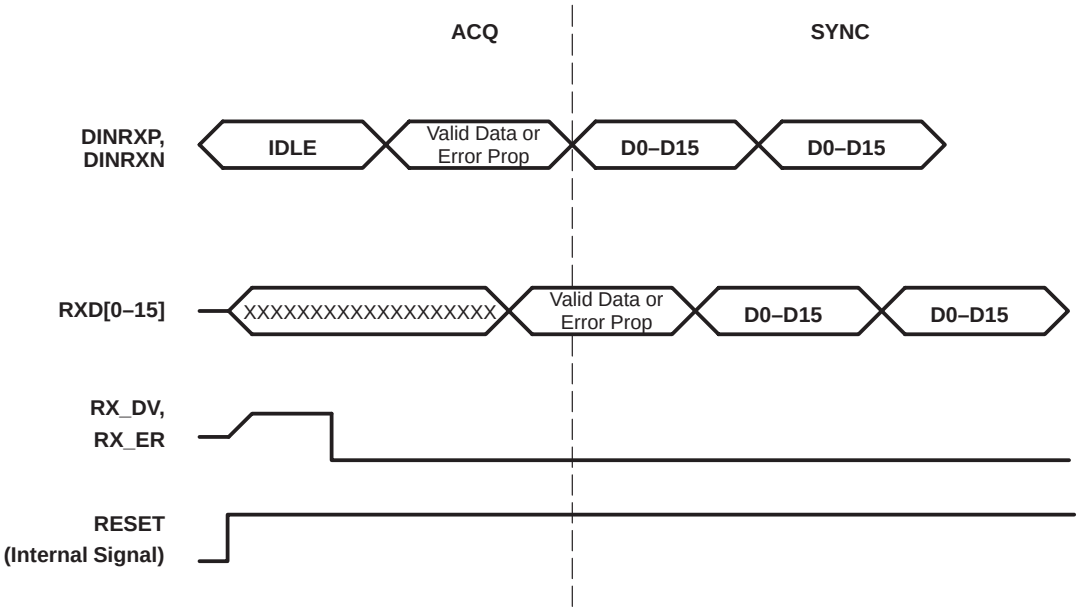



**Figure 9. Receive Side Timing Diagram (Valid Data or Error Propagation)**

**redundant port operation**

The PCI6060 allows users to design a redundant port by connecting receive data bus terminals from two PCI6060 devices together. Asserting the LCKREFN to a low state will cause the receive data bus terminals, the RXD[0:15], RX_CLK and RX_ER, and RX_DV/LOS to go to a high-impedance state.

PRODUCT PREVIEW

**PRBS verification**

The PCI6060 also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the RX_ER/PRBSPASS terminal low.

**reference clock input**

The reference clock (GTX_CLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency-locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edge clock, providing a serial data rate that is 20 times the reference clock.

**operating frequency range**

The PCI6060 is optimized for operation at a serial data rate of 2.5 Gbps. The PCI6060 may operate at a serial data rate between 1.6 Gbps to 2.5 Gbps. The GTX_CLK must be within ±100 PPM of the desired parallel data rate clock.

**testability**

The PCI6060 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable terminal allows for all circuitry to be disabled so that an $I_{DDQ}$ test can be performed. The PRBS function allows for a BIST (built-in self-test).

**loopback testing**

The transceiver can provide a self-test function by enabling (LOOPEN) the internal loop-back path. Enabling this terminal will cause serial-transmitted data to be routed internally to the receiver. The parallel data output can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loopback testing.)

**built-in self-test (BIST)**

The PCI6060 has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the RX_ER/PRBS_PASS terminal.

**power-on reset**

Upon application of minimum valid power, the PCI6060 generates a power-on reset. During the power-on reset the RXD, RX_ER, and RX_DV/LOS signal terminals go to a high-impedance state. The RX_CLK is held low. The length of the power-on reset cycle is dependent upon the REFCLK frequency, but will be less than 1 ms.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1) . . . . . –0.3 to 3 V
Voltage range at TXD, ENABLE, GTX_CLK, TX_EN, TX_ER, LOOPEN, PRBS_PASS . . . . . –0.3 to 4 V
Voltage range at any other terminal except above . . . . . –0.3 to $V_{CC}$+0.3 V
Package power dissipation, $P_D$ . . . . . See Dissipation Rating Table
Storage temperature, $T_{stg}$ . . . . . –65°C to 150°C
Electrostatic discharge . . . . . HBM:3 KV, CDM:1.5 KV
Characterized free-air operating temperature range, $T_A$ . . . . . –40°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR‡ ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| RCP64§ | 5.25 W | 46.58 mW/°C | 2.89 W |
| RCP64¶ | 3.17 W | 23.70 mW/°C | 1.74 W |
| RCP64# | 2.01 W | 13.19 mW/°C | 1.11 W |

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
§ 2 oz. Trace and copper pad with solder.
¶ 2 oz. Trace and copper pad without solder.
# Standard JEDEC High-K board.

For more information, refer to TI application note *PowerPAD™ Thermally Enhanced Package,* TI literature number SLMA002.

## electrical characteristics over recommended operating conditions

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 2.3 | 2.5 | 2.7 | V |
| Supply current, $I_{CC}$ | $V_{DD}$ = 2.5 V, Frequency = 1.6 Gbps, PRBS pattern | | 95 | | mA |
| | $V_{DD}$ = 2.5 V, Frequency = 2.5 Gbps, PRBS pattern | | 135 | | |
| Power dissipation, $P_D$ | $V_{DD}$ = 2.5 V, Frequency = 1.6 Gbps, PRBS pattern | | 238 | | mW |
| | $V_{DD}$ = 2.5 V, Frequency = 2.5 Gbps, PRBS pattern | | 337 | | mW |
| | $V_{DD}$ = 2.5 V, Frequency = 2.5 Gbps, worst case pattern‖ | | | 461 | mW |
| Shutdown current | Enable = 0, $V_{DDA}$, $V_{DD}$ terminals, $V_{DD}$ = MAX | | 2 | | mA |
| PLL startup lock time | $V_{DD}$,$V_{DDA}$ = 2.3V, EN ↑ to PLL acquire | | 0.1 | 0.4 | ms |
| Data acquisition time | | | 1024 | | bits |
| Operating free-air temperature, $T_A$ | | –40 | | 85 | °C |

‖ Worst case pattern is a pattern that creates a maximum transition density on the serial transceiver.

## reference clock (GTX_CLK) timing requirements over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency | Minimum data rate | Typ–0.01% | 80 | Typ+0.01% | MHz |
| Frequency | Maximum data rate | Typ–0.01% | 125 | Typ+0.01% | MHz |
| Frequency tolerance | | –100 | | | ppm |
| Duty cycle | | 40% | 50% | 60% | % |
| Jitter | Peak-to-peak | | | 40 | ps |

PRODUCT PREVIEW

**TTL input electrical characteristics over recommended operating conditions (unless otherwise noted), TTL signals: TXDO–TXD15, GTX_CLK, LOOPEN, LCKREFN, PRBS_PASS**

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | Figure 10 | 2 | | 3.6 | V |
| $V_{IL}$ | Low-level input voltage | Figure 10 | | | 0.80 | V |
| $I_{IL}$ | Input high current | $V_{DD}$ = MAX, $V_{IN}$ = 2 V | | | 40 | μA |
| $I_{IH}$ | Input low current | $V_{DD}$ = MAX, $V_{IN}$ = 0.4 V | –40 | | | μA |
| $C_I$ | | 0.8 V to 2 V | | | 4 | pF |
| $t_r$ | Rise time, GTX_CLK, TX_EN, TX_ER, TXD | 0.8 V to 2 V, C = 5 pF<br>See Figure 10 | | 1 | | ns |
| $t_f$ | Fall time, GTX_CLK, TX_EN, TX_ER, TXD | 2 V to 0.8 V, C = 5 pF<br>See Figure 10 | | 1 | | ns |
| $t_{su}$ | TXD, TX_EN, TX_ER setup to ↑ GTX_CLK | See Figure 10 | 1.5 | | | ns |
| $t_h$ | TXD, TX_EN, TX_ER hold to ↑ GTX_CLK | See Figure 10 | 0.4 | | | ns |

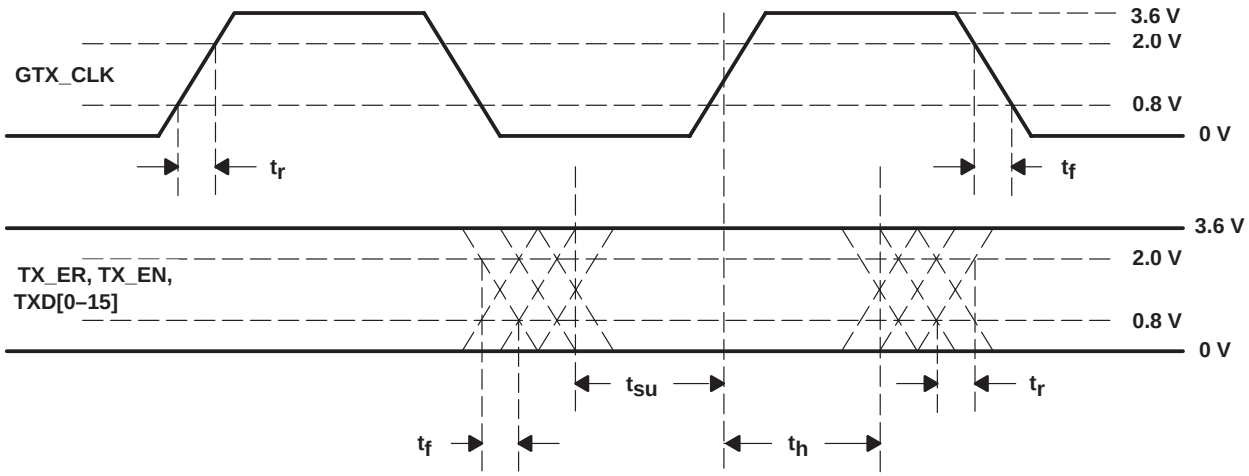



**Figure 10. TTL Data Input Valid Levels for ac Measurements**

## TTL output switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –1 mA, $V_{DD}$ = MIN | 2.10 | 2.3 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1 mA, $V_{DD}$ = MIN | GND | 0.25 | 0.5 | V |
| $t_{r(slew)}$ | Slew rate (rising), magnitude of RX_CLK, RX_ER, RX_DV/LOS, RXD | 0.8 V to 2 V, See Figure 11, C = 5 pF | 0.5 | | | V/ns |
| $t_{f(slew)}$ | Slew rate (falling), magnitude of RX_CLK, RX_ER, RX_DV/LOS, RXD | 0.8 V to 2 V, See Figure 11, C = 5 pF | 0.5 | | | V/ns |
| $t_{su}$ | RXD, RX_DV/LOS, RX_ER setup to ↑ RX_CLK | See Figure 11, 50% voltage swing, GTX_CLK = 125 MHz | 3 | | | ns |
| | | See Figure 11, 50% voltage swing, GTX_CLK = 80 MHz | 5.8 | | | ns |
| $t_h$ | RXD, RX_DV/LOS, RX_ER hold to ↑ RX_CLK | See Figure 11, 50% voltage swing, GTX_CLK = 125 MHz | 3 | | | ns |
| | | See Figure 11, 50% voltage swing, GTX_CLK = 80 MHz | 5.8 | | | ns |

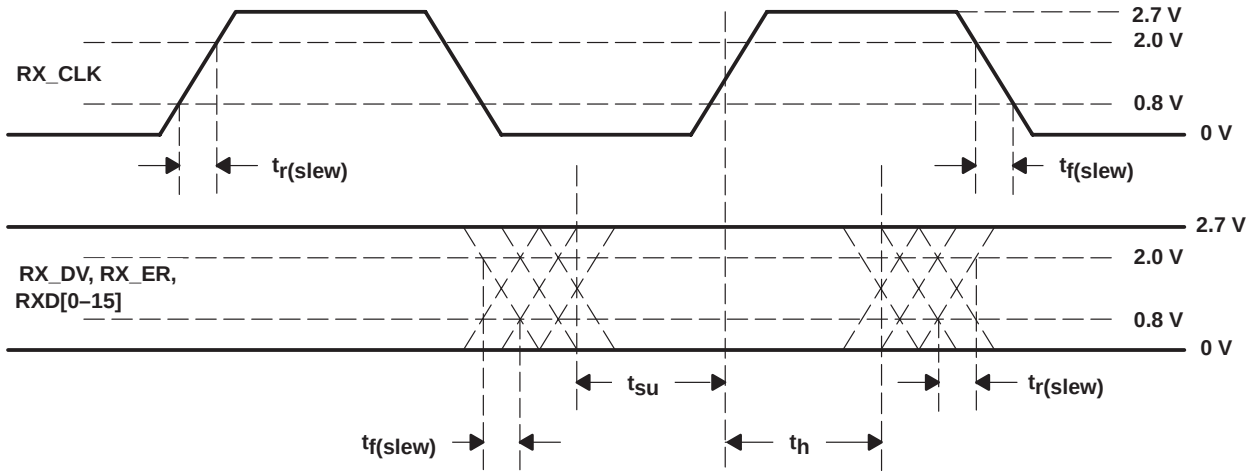



**Figure 11. TTL Data Output Valid Levels for AC Measurements**

PRODUCT PREVIEW

## transmitter/receiver characteristics

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Vodp = $\|VTXP–VTXN\|$, Pre-emphasis $V_{OD}$, direct | $R_t$ = 50 Ω, RREF = 200 Ω, dc-coupled, See Figure 12 | 840 | 1050 | 1260 | mV |
| | Vodd = $\|VTXP–VTXN\|$, De-emphasis $V_{OD}$, direct | $R_t$ = 50 Ω, RREF= 200 Ω, dc-coupled, See Figure 12 | 760 | 950 | 1140 | mV |
| | Transmit termination voltage range, (VTXP + VTXN)/2 | | 1500 | | 2500 | mV |
| | Receiver input voltage requirement, $V_{ID}$=\|RXP – RXN\| | | 200 | | | mV |
| | Receiver common mode voltage range, (VRXP + VRXN)/2 | | | 1500 | | mV |
| $L_{IN}$ | Receiver input leakage | | –10 | | 10 | mA |
| $C_{IN}$ | Receiver input capacitance | | | | 2 | pF |
| | Serial data total jitter (peak-to-peak) | Differential output jitter at 2.5 Gbps, random + deterministic, PRBS pattern | | 0.10 | | UI† |
| | Serial data total jitter (peak-to-peak) | Differential output jitter at 1.6 Gbps, random + deterministic, PRBS pattern | | 0.10 | | UI† |
| $t_r$, $t_f$ | Differential output signal rise, fall time (20% to 80%) | $R_L$ = 50 Ω, $C_L$ = 5 pF, See Figure 12 | | TBD | | ps |
| | Jitter tolerance | Zero crossing | 40% | | | UI† |
| ($T_{latency}$) | Tx latency | | 34 | | 38 | bits |
| ($R_{latency}$) | Rx latency | | 76 | | 107 | bits |

† UI is the time interval of one serialized bit.

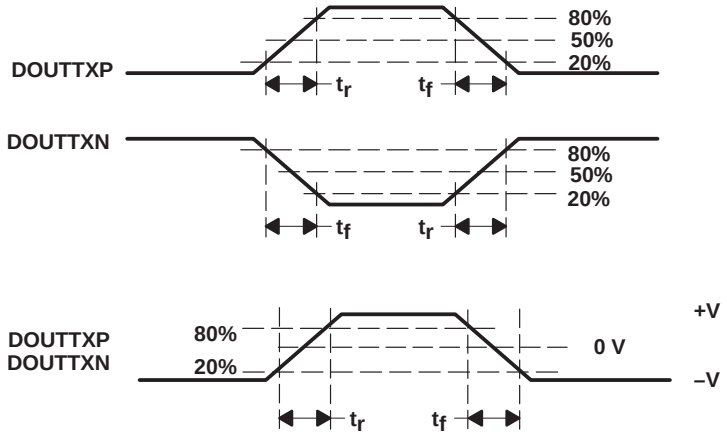



**Figure 12. Differential and Common-Mode Output Voltage Definitions**

## THERMAL INFORMATION

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land | | 21.47 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case-thermal resistance | Board-mounted, no air flow, high conductivity TI recommended test board, chip soldered or greased to thermal land | | 0.38 | | °C/W |
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land | | 42.20 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case-thermal resistance | Board-mounted, no air flow, high conductivity TI recommended test board with thermal land but no solder or grease thermal connection to thermal land | | 0.38 | | °C/W |
| $R_{\theta JA}$ | Junction-to-free-air thermal resistance | Board-mounted, no air flow, JEDEC test board | | 75.83 | | °C/W |
| $R_{\theta JC}$ | Junction-to-case-thermal resistance | Board-mounted, no air flow, JEDEC test board | | 7.8 | | °C/W |

## APPLICATION INFORMATION

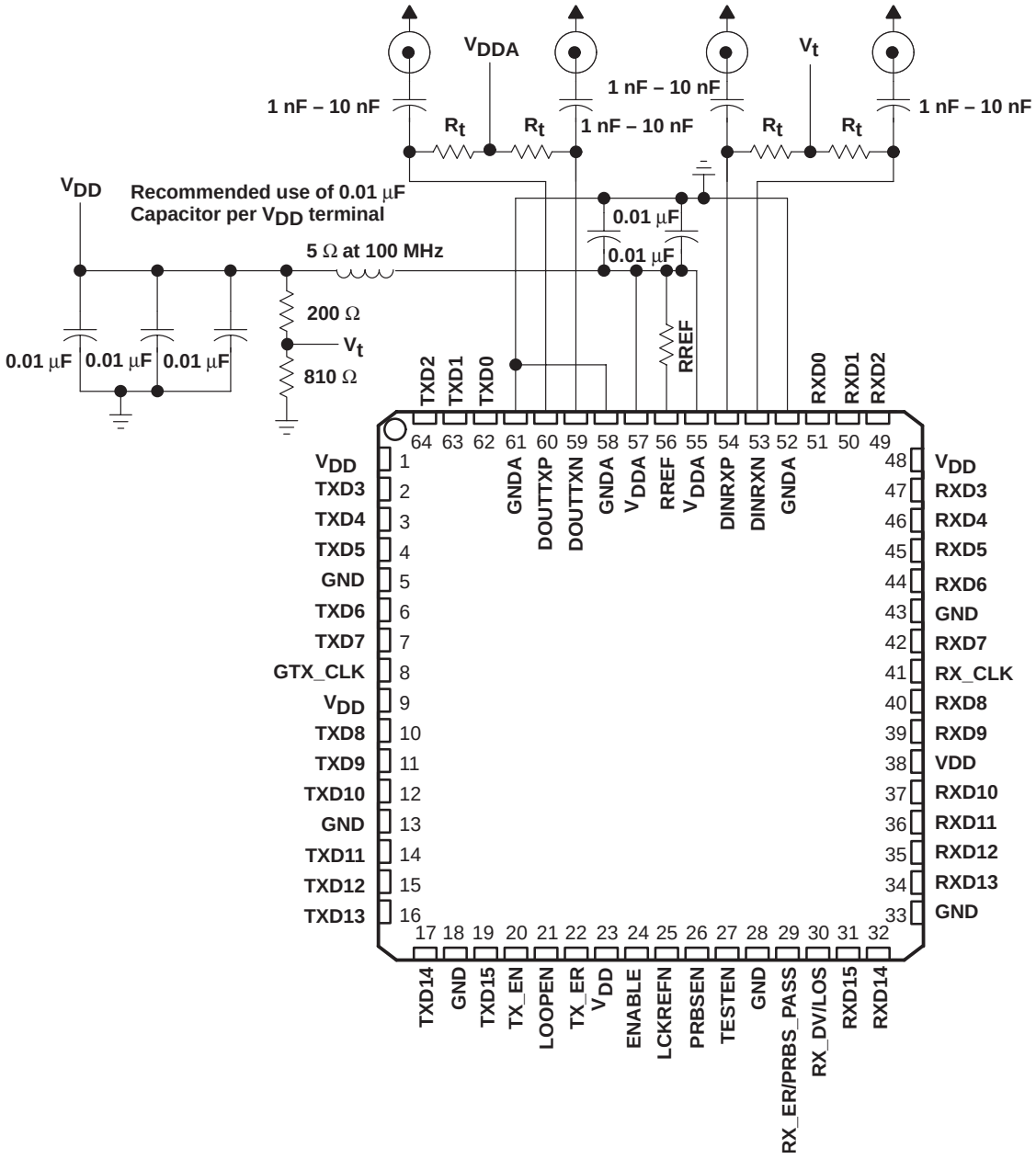



**Figure 13. External Component Interconnection**

## APPLICATION INFORMATION

### recommended values of external resistors (1% tolerance)

| PARAMETER | TEST CONDITIONS | RECOMMENDED | UNIT |
|---|---|---|---|
| $R_{(t)}$, Termination resistor | 50 Ω environment | 50 | Ω |
| | 75 Ω environment | 75 | |
| $R_{(REF)}$, Reference resistor | 50 Ω environment | 200 | Ω |
| | 75 Ω environment | 300 | |

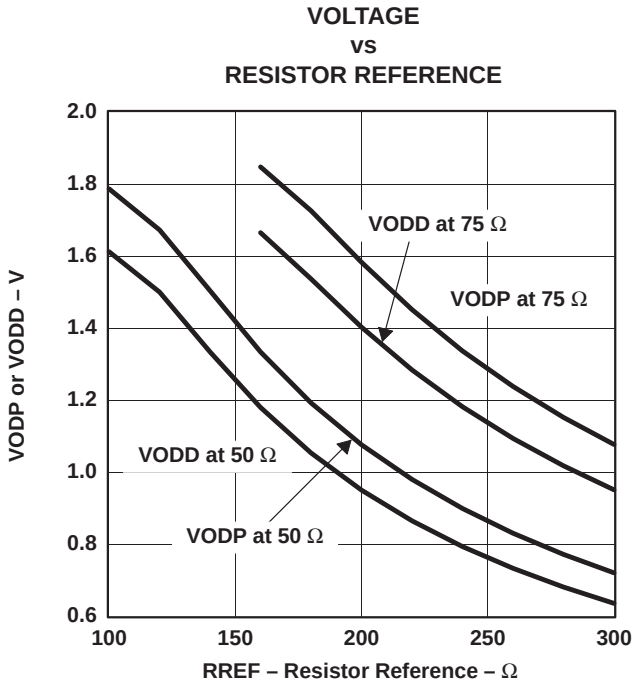



**Figure 14. Differential Transmitter Voltage**

### choosing resistor values

PCI6060 offers the flexibility to customize the voltage swing and transmission line termination by adjusting the reference resistor, RREF, and termination resistor, $R_t$. By choosing particular resistor values, the system can be optimized for a particular transmission line impedance, length, and controlling the output swing for EMI and attenuation concerns. Refer to Figure 14 to determine the nominal voltage swing and driver current as a function of resistor values. It is recommended that 1% tolerance resistors be used. Refer to Figure 15 for high-speed I/O directly coupled mode and Figure 16 for high-speed I/O ac-coupled mode.

PRODUCT PREVIEW

## APPLICATION INFORMATION

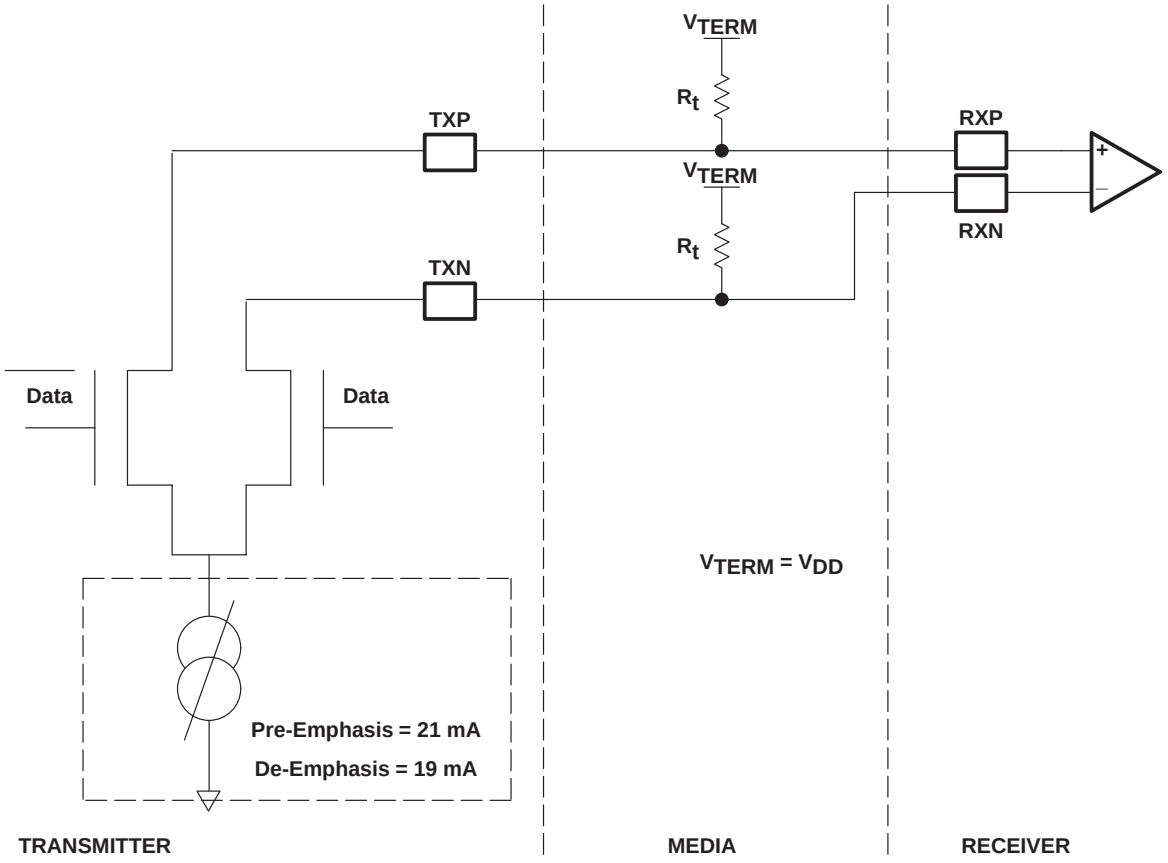



**Figure 15. High-Speed I/O Directly Coupled Mode**

PRODUCT PREVIEW

## APPLICATION INFORMATION

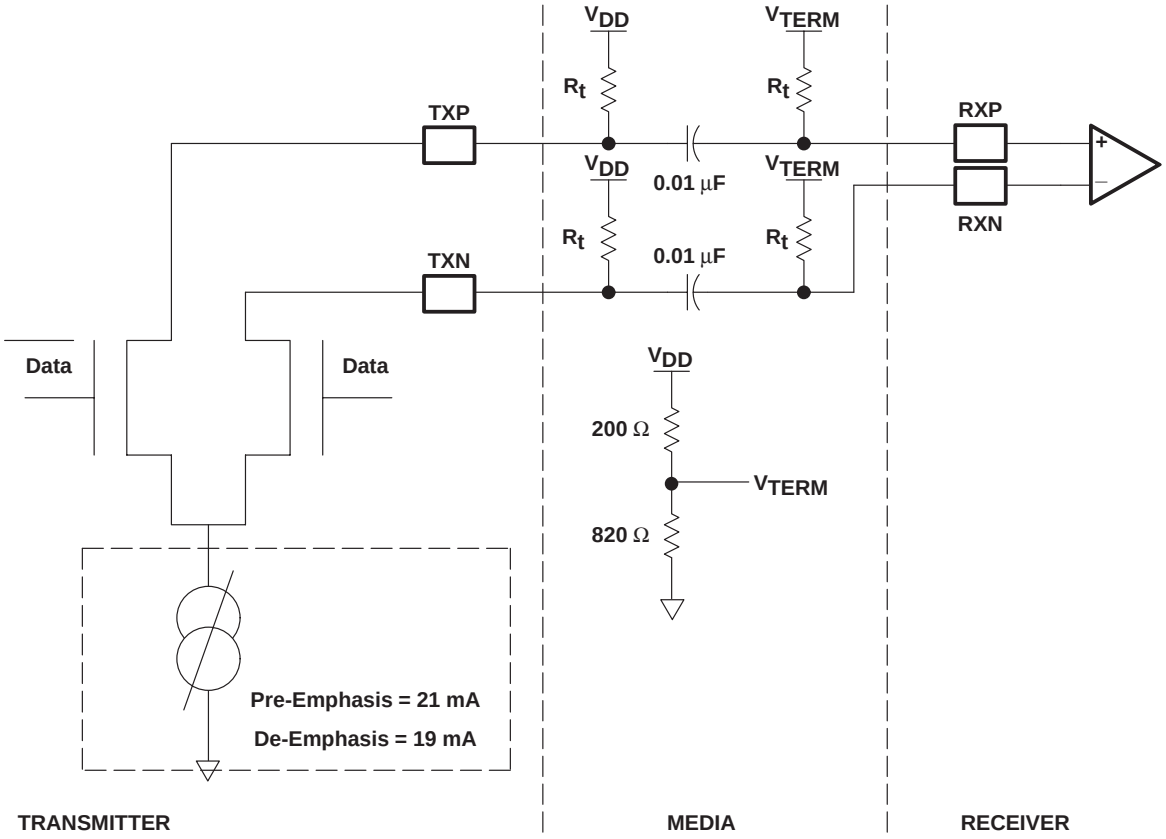



**Figure 16. High-Speed I/O AC Coupled Mode**

PRODUCT PREVIEW

## APPLICATION INFORMATION

### designing with PowerPAD™

The PCI6060 is housed in a high-performance, thermally enhanced, 64-pin VQFP (RCP64) PowerPAD™ package. Use of the PowerPAD™ package does not require any special considerations except to note that the PowerPAD™, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD™ PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD™ of connection etches or vias under the package. It is strongly recommended that the PowerPAD™ be soldered to the thermal land. The recommended convention, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keep-out area for the 64-pin PFP PowerPAD™ package is 8 mm X 8 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD™ package. The thermal land will vary in size depending on the PowerPAD™ package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD™ Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com.

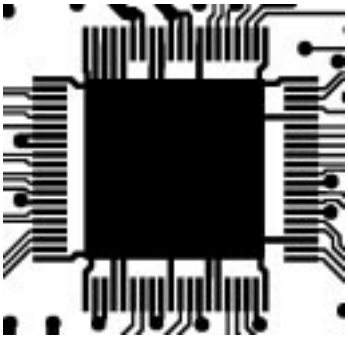


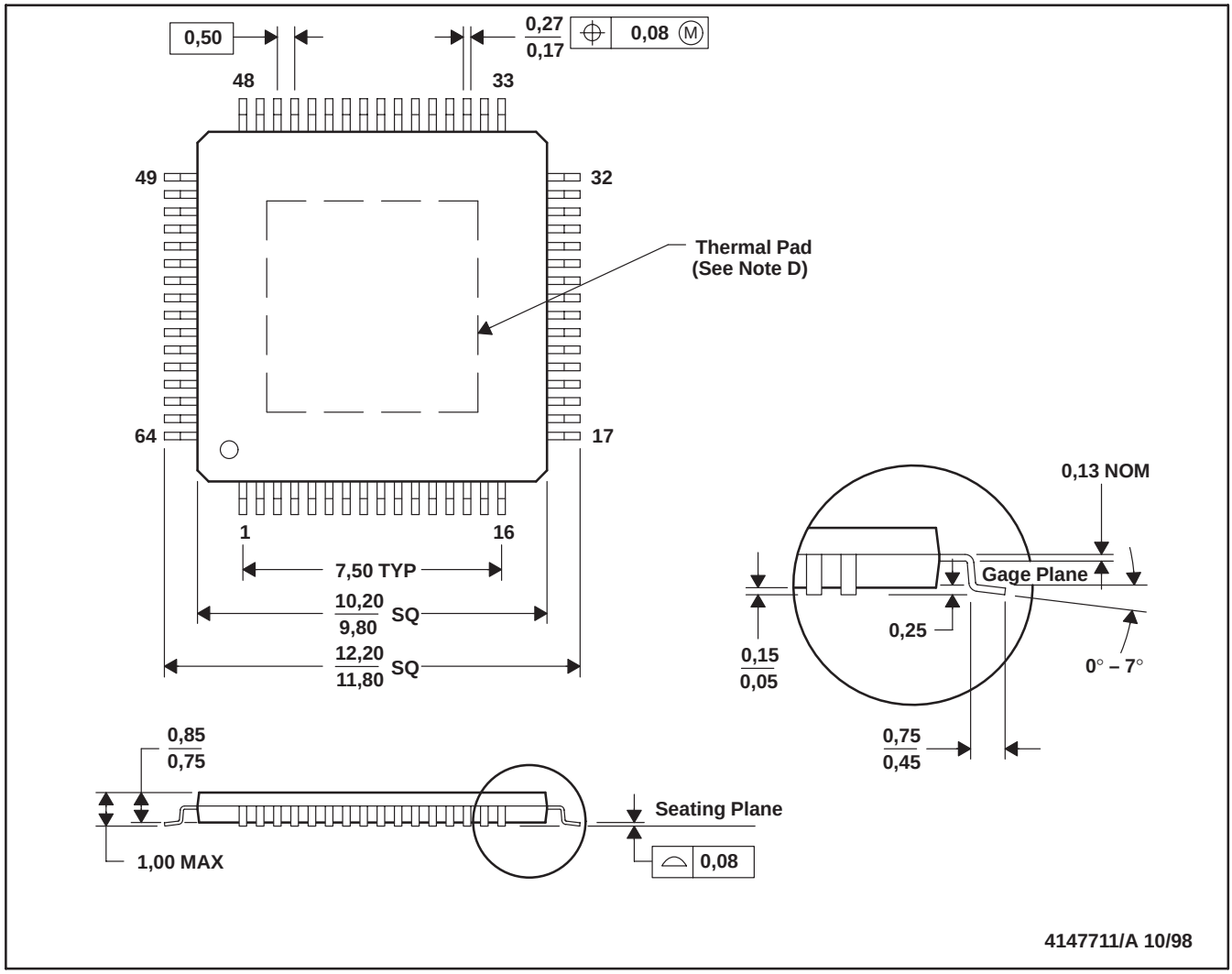
**Figure 17. Example of a Thermal Land**

For the PCI6060, this thermal land should be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD™ using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

## MECHANICAL DATA

**RCP (S-PQFP-G64)** **PowerPAD™ PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.