Application Note, DS1, May 2002

IPAC-X, ISAC-SX, ISAC-SX TE and SBCX-X

PSB 21150, PEB 3086, PSB 3186 and PEB 3081

Test Functions of new S-Transceiver family

Wired Communications

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Application Note

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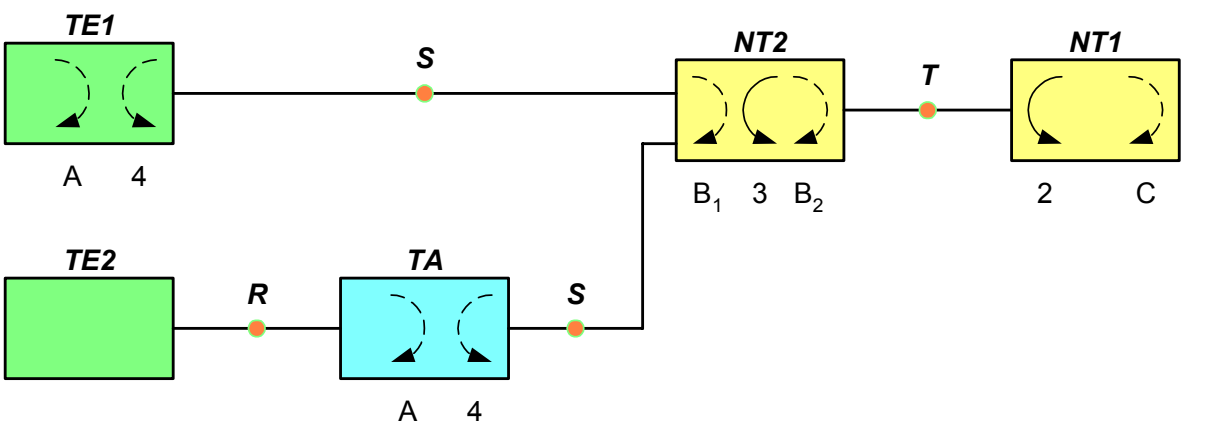
1 Test Functions

The following chapters describe the test functions which can be realized with our S-transceivers. Every sub-chapter consists of a short description of the corresponding function based on the new 3.3 V S-transceivers and of a detailed programming example.

1.1 Test Loops According to ETS 300 012-1

The focus of this chapter is to get an overview of the defined test loops and how to realize that loops with our S-transceivers.

In the ETS 300 012-1 (Oct. 1998), chapter C.2, the loopback mechanism is defined. Furthermore, the test loopback reference configuration is defined in chapter C.3. There is written: **Figure 1** shows the possible locations of test loopbacks pertaining to the maintenance of the ISDN basic UNI. Recommended and desirable loopbacks are drawn in solid lines. Optional loopbacks are drawn with dashed lines. These optional loopbacks may not be provided by all equipments. The characteristics of each of these loopbacks are given in tables C.1 and C.2, respectively. These tables are not implemented in this Application Note, but can be found in the ETS 300 012-1 (Oct. 1998), chapter C.4.



NOTE 1: Loopbacks B_1 and 3 are applicable to each individual interface at reference point S.

NOTE 2: Loopbacks A, B_1, B_2, C and 4 are optional. The definition of these loopbacks is outside the scope of this ETS.

ETS300012_FigureC-3

Figure 1 Location of Loopbacks (Source: ETS300012-1, Figure C.3)

In the following chapters the loopbacks which are possible with our S-transceivers are explained and shown in more detail.

1.1.1 Internal Loops

1.1.1.1 Loop A for TE1 (TE Mode) & TA

Test loop A (ref. **Figure 2**) is a non-transparent or transparent loop (bit TR_CONF2.DIS_TX) with the forward data path is blocked. It allows to loop back all three channels (B1, B2, D). Test loop A is activated by the C/I channel command *Activate*

Request Loop (ARL, C/I command code 1010_b) or by setting the bit LP_A (Loop Analog) in the TR_CMD register if the layer-1 state machine is disabled (TR_CONF0.L1SW = 1). A physical S/T interface is not required. When the receiver has synchronized itself to this signal, the C/I indication AIL or ARL is delivered in the C/I channel.

In this test loop mode, the S/T interface awake detector is enabled, i.e. if a level is detected (e.g. INFO2 / INFO4) this will be reported by the ReSYnchronization Indication (RSY, C/I indication code 0100_b). The loop function is not effected by this condition and the internally generated 192-kHz line clock does not depend on the signal received at the S/T interface.

Note: As long as a level is detected, the LD bit in TR_STA and ISTA_TR is active and generates an interrupt if enabled by software. Once a level was detected, the RSY C/I indication is stable in the CIR0 register even if the detected signal was switched off. The RSY indication will be changed only, if the ARL C/I command will be released.

Depending on the TR_CONF2.DIS_TX bit the internal local loop can be transparent (DIS_TX = 0) or non-transparent (DIS_TX = 1) to the S/T line.

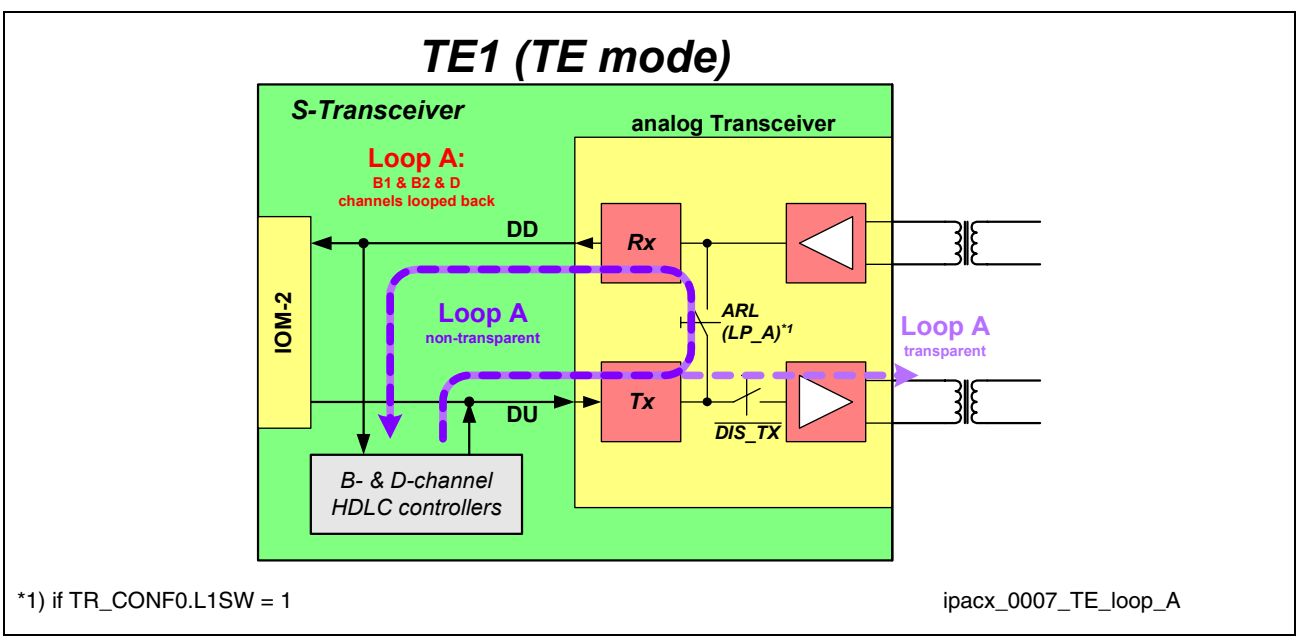


Figure 2 Loop A

Programming examples for 3.3 V S-transceivers for TE and LT-T mode.

Note: In LT-T mode MODED.DIM1 = 1 must be set first.

Table 1 Programming Example for Non-Transparent Loop A (Hardware State Machine)

Description	3.3 V S-transceivers (IPAC-X)
Disable Transmitter (default)	w TR_CONF2.DIS_TX = 1
Activation of Loop A with CI-command ARL	w CIX0 = **1010** 0001_b
Check if loop is closed	r CIR0 = **1110** 0010_b

Table 2 Programming Example for Non-Transparent Loop A (Software State Machine)

Description	3.3 V S-transceivers (IPAC-X)
Disable Transmitter (default)	w TR_CONF2.DIS_TX = 1
Enable Software State Machine	w TR_CONF0.L1SW = 1
Activation of Loop A	w TR_CMD.LP_A = 1 & w TR_CMD.XINF = 011_b

Table 3 Programming Example for Transparent Loop A (Hardware State Machine)

Description	3.3 V S-transceivers (IPAC-X)
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Loop A with CI-command ARL	w CIX0 = **1010** 0001_b

Table 4 Programming Example for Transparent Loop A (Software State Machine)

Description	3.3 V S-transceivers (IPAC-X)
Enable Software State Machine	w TR_CONF0.L1SW = 1
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Loop A	w TR_CMD.LP_A = 1 & w TR_CMD.XINF = 011_b

1.1.1.2 Loop 2 for NT mode (NT1) and Loop 3 for LT-S mode (NT2 / PBX)

Test loop 2 (ref. **Figure 3**) and test loop 3 (ref. **Figure 4**) is likewise activated over the IOM-2 interface with *Activate Request Loop* (ARL, 1010_b), but for loop 2 the *Activation Indication Loop* (AIL, 1110_b) command must follow additionally. No S line is required.

INFO4 is looped back internally to the receiver and also sent to the S/T interface. When the receiver is synchronized, the message AI is sent in the C/I channel.

Depending on the TR_CONF2.DIS_TX bit the test loops can be transparent (DIS_TX = 0) or non-transparent (DIS_TX = 1) to the S/T line.

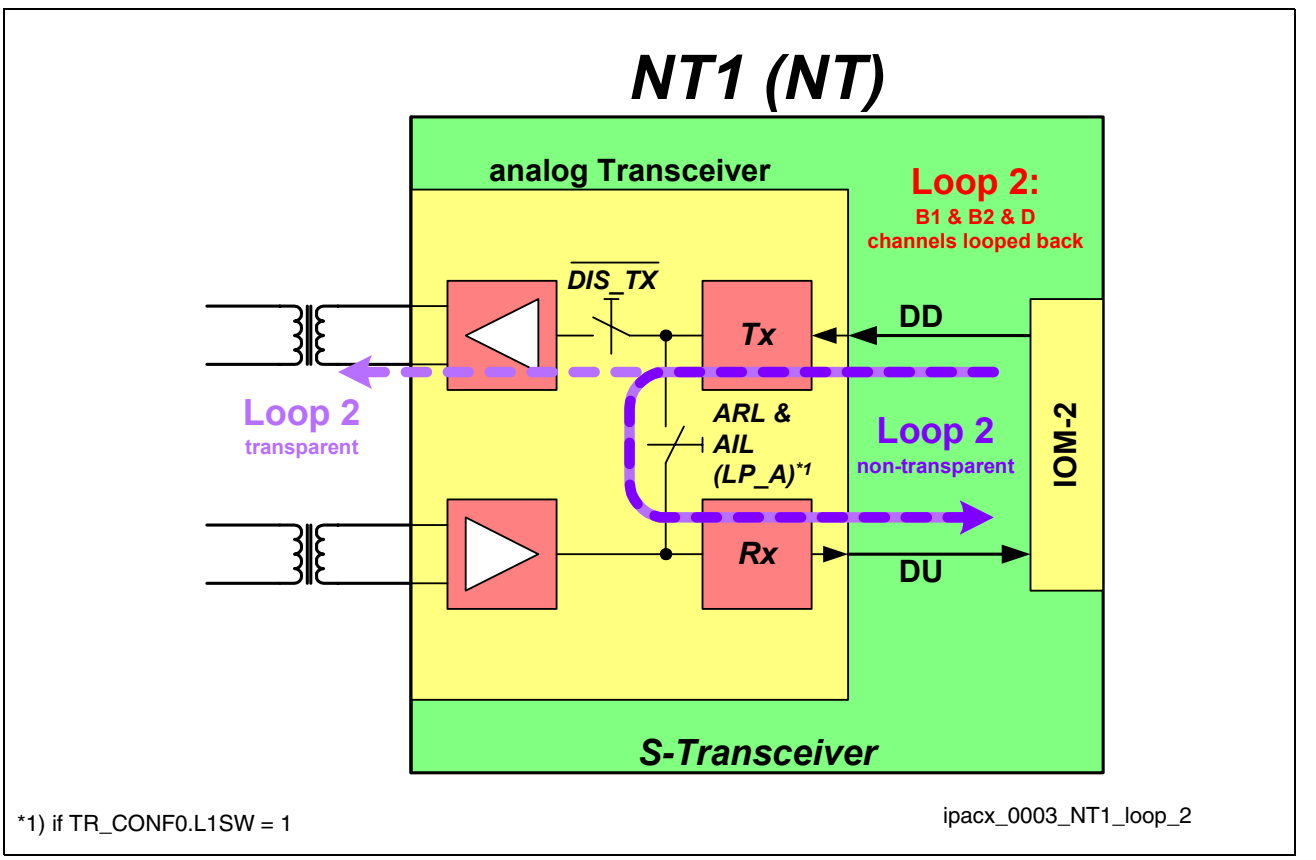


Figure 3 Loop 2

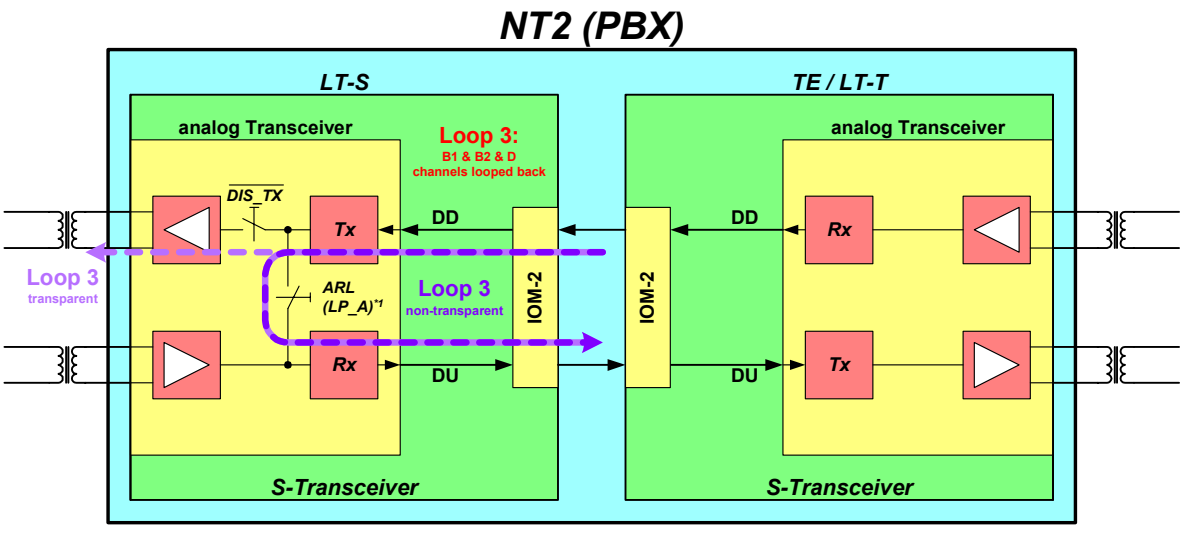


Figure 4 Loop 3

Table 5 Programming Example for Non-Transparent Loop 2 & 3 (Hardware State Machine)

Description	3.3 V S-Transceivers (IPAC-X)
Disable Transmitter (default)	w TR_CONF2.DIS_TX = 1
Activation of Loop A with CI-command ARL	w CIX0 = **1010** 1110_b
For NT only: Finish loop activation with CI-command AIL	w CIX0 = **1110** 1110_b

Table 6 Programming Example for Non-Transparent Loop 2 & 3 (Software State Machine)

Description	3.3 V S-Transceivers (IPAC-X)
Disable Transmitter (default)	w TR_CONF2.DIS_TX = 1
Enable Software State Machine	w TR_CONF0.L1SW = 1
Activation of Loop A	w TR_CMD.LP_A = 1 & w TR_CMD.XINF = 011_b

Table 7 Programming Example for Transparent Loop 2 & 3 (Hardware State Machine)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Loop A with CI-command ARL	w CIX0 = **1010** 1110_b
For NT only: Finish loop activation with CI-command AIL	w CIX0 = **1110** 1110_b

Table 8 Programming Example for Transparent Loop 2 & 3 (Software State Machine)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Software State Machine	w TR_CONF0.L1SW = 1
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Loop A	w TR_CMD.LP_A = 1 & w TR_CMD.XINF = 011_b

1.1.1.3 Loop 4 for TE1 Side

The test loop 4 as described in the ETS 300 012-1 (Oct. 1998) specification can be realized with our 3.3 V S-transceivers by using the implemented CDA handler (ref. **Figure 5**). The B-channel informations (B1 & B2) received from the line card is transparently forwarded to the output IOM-2 channels. After then, this B-channel data will be looped from the Data Downstream (DD) line back to the Data Upstream (DU) line of the IOM-2 interface by the CDA handler and therefore, the received data is looped back to the S/T interface.

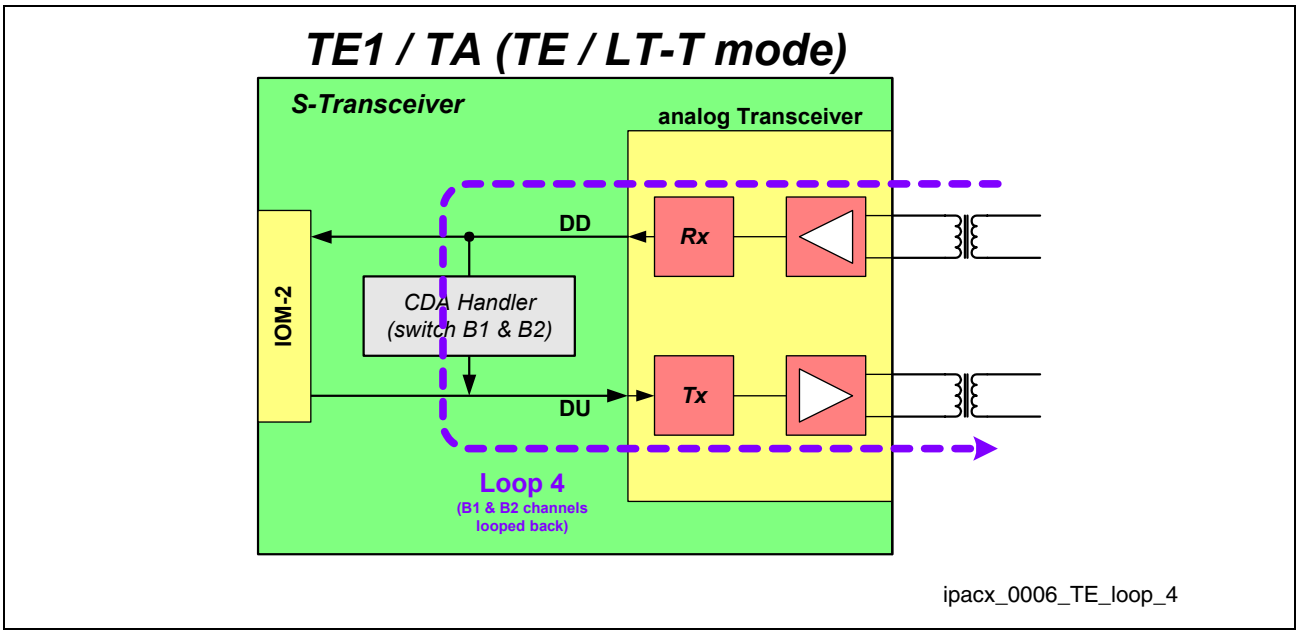


Figure 5 Loop 4

Programming examples for new S-transceivers for TE and LT-T mode.

Note: In LT-T mode MODED.DIM1 = 1 must be set first.

Table 9 Programming Example for Loop 4

Description	3.3 V S-Transceivers (IPAC-X)
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Enable Data Buffer (AR8 command)	w CIX0 = **1000** 0001_b
Check if default values is CDA handler are valid. If not: write values into registers.	r CDA_TSDP20 = 80h
	r CDA_TSDP21 = 81h
Enable Loop 4	w CDA2_CR = 1Eh

1.1.2 External Local Loop

The external local loop (external Loop A) is activated in the same way as the internal local loop described above (**Chapter 1.1.1.1**). Additionally the EXLP bit in the TR_CONF0 register has to be programmed and the loop has to be closed externally as described in **Figure 6**. This allows complete system diagnostics.

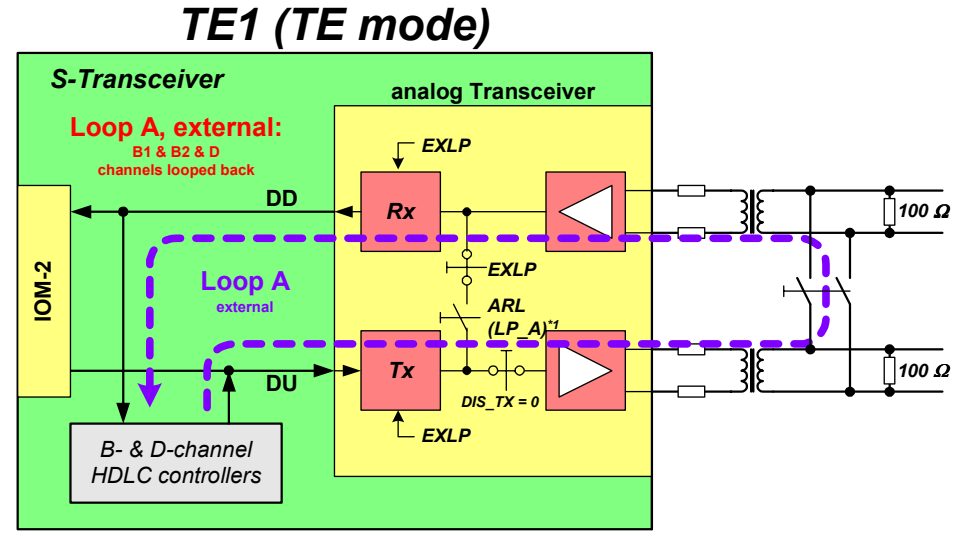


Figure 6 External Loop at the S/T-Interface

Table 10 Programming Example for External Loop A (Hardware State Machine)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Loop A with CI-command ARL	w CIX0 = **1010** 0001_b
Enable external local loop (external Loop A)	w TR_CONF0.EXLP = 1

Table 11 Programming Example for External Loop A (Software State Machine)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Software State Machine	w TR_CONF0.L1SW = 1
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Loop A	w TR_CMD.LP_A = 1 & w TR_CMD.XINF = 011_b
Enable external local loop (external Loop A)	w TR_CONF0.EXLP = 1

1.2 Remote Line Loop

In remote line loop (RLP) mode received data is looped back to the S/T interface. The D-channel information received from the line card is transparently forwarded to the output IOM-2 D-channel. The output B-channel information on IOM-2 is fixed to FFh while this test loop is active. The remote loop is programmable in TR_CONF2.RLP.

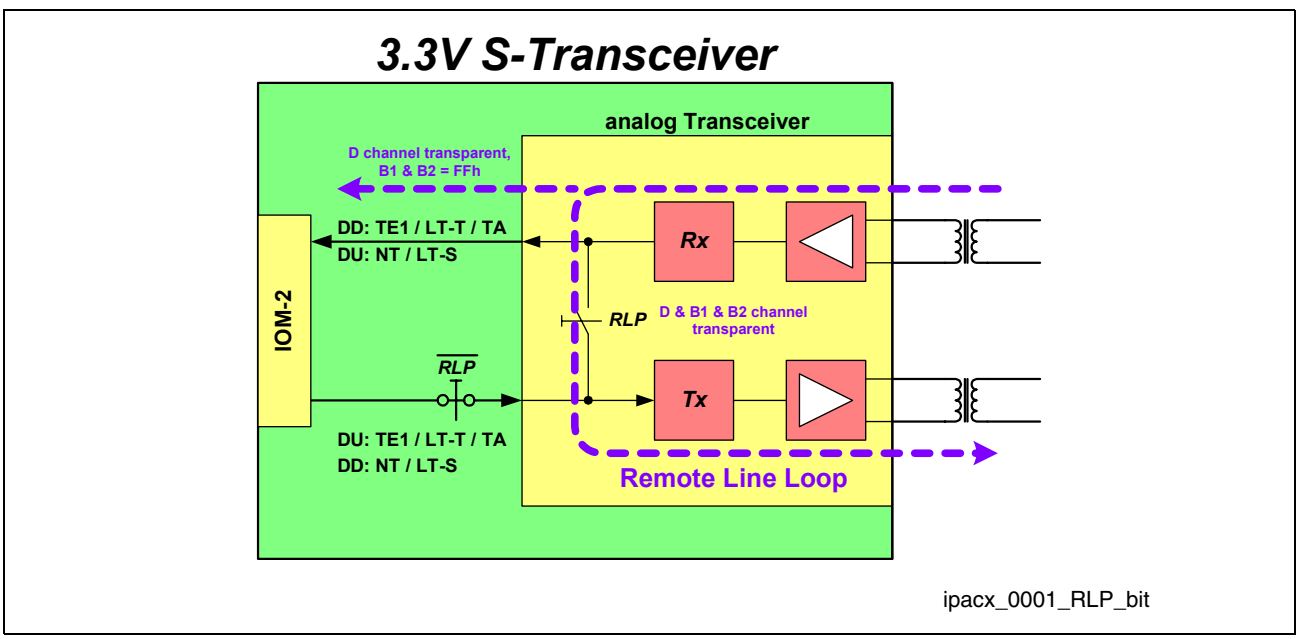


Figure 7 Remote Line Loop

Table 12 Programming Example for Remote Line Loop (TE Mode)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Data Buffer (AR8 command)	w CIX0 = **1000** 0001_b
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Remote Line Loop	w TR_CONF2.RLP = 1

Table 13 Programming Example for Remote Line Loop (NT Mode)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Data Buffer (AR command followed by AI command)	w CIX0 = **1000** 1110_b w CIX0 = **1100** 1110_b
Enable Transmitter	w TR_CONF2.DIS_TX = 0
Activation of Remote Line Loop	w TR_CONF2.RLP = 1

1.3 Layer-2 Function-Test

Test of HDLC (layer-2) functions while disabling all S/T transceiver (layer-1) functions and pins associated with them (including clocking) via bit TR_CONF0.DIS_TR. The HDLC controllers can still operate if DCL and FSC clock signals are available independent from the TR_CONF0.DIS_TR bit setting.

Note: In TE mode the DCL and FSC pins become input if the transceiver was disabled (TR_CONF0.DIS_TR = 1).

*Note: The IOM-2 Loop via TLP (**Chapter 1.3.1**) is not supported by SBCX-X!*

1.3.1 IOM-2 Loop via TLP

This is used for testing IPAC-X functionality excluding layer 1 (loopback between XFIFOx and RFIFOx) by setting command bit TLP (Test Loop, TMD and TMB registers). The Tx path of layer-2 is internally connected with the Rx path of layer 2. Data coming from the layer 1 controller will not be forwarded to the layer 2 controller. The output from layer 1 (S/T) on DD is ignored. However, the setting of TLP is only valid if the IOM-2 clocks are available.

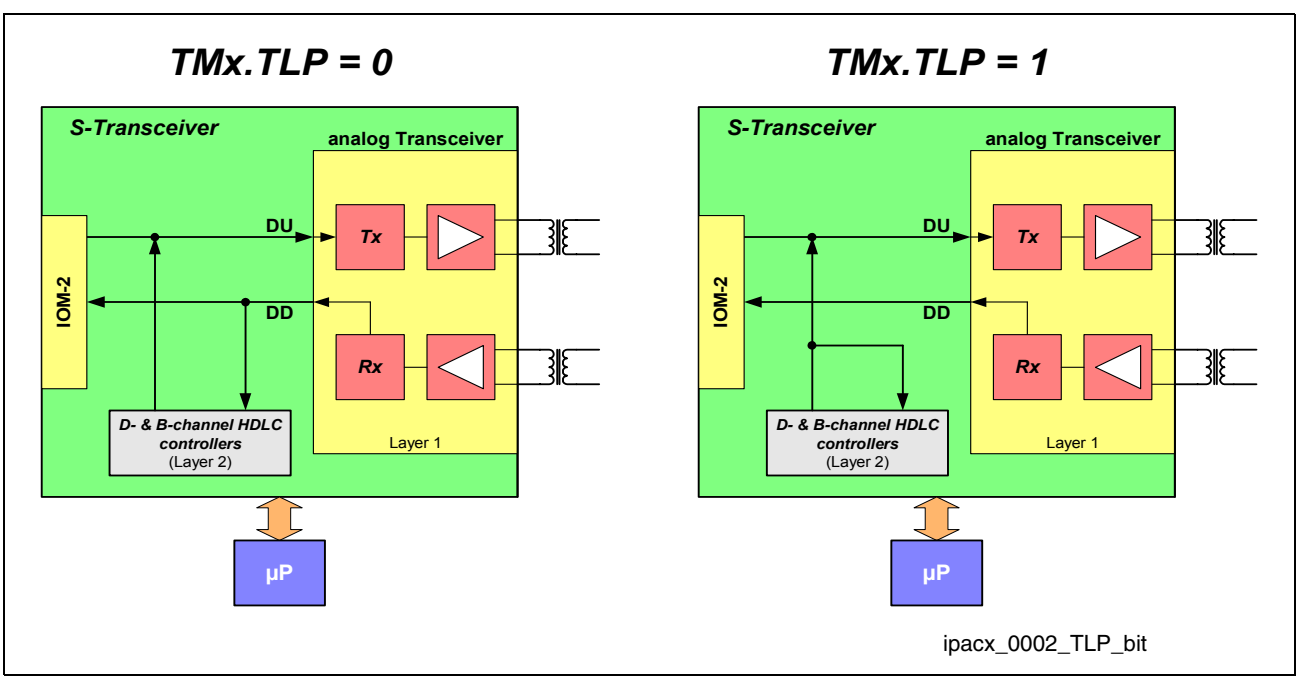


Figure 8 Layer-2 Test Loops

Table 14 Programming Example for Layer 2 Test Loops

Description	3.3 V S-Transceivers (IPAC-X)
Enable D-channel Test Loop (Layer 2)	w TMD.TLP = 1
Enable B-channel Test Loop (Layer 2)	w TMB.TLP = 1

Table 14 Programming Example for Layer 2 Test Loops (cont'd)

Description	**3.3 V S-Transceivers (IPAC-X)**
For **transparent** Loop enable Transmitter	w TR_CONF2.DIS_TX = 0
For **non-transparent** Loop disable Transmitter	

1.4 Transmission of Special Test Signals to the S/T-Interface

Transmission of special test signals to the S/T interface according to the modified AMI code are initiated via a C/I command written in CIX0 register. Two kinds of test signals may be sent by the IPAC-X:

1.4.1 Single Pulses

The single pulses are of alternating polarity, one S/T interface bit period wide, 0.25ms apart, with a repetition frequency of 2 kHz. Single pulses can be sent in all applications. The corresponding C/I command in TE, LT-S and LT-T applications is SSP (Send Single Pulses).

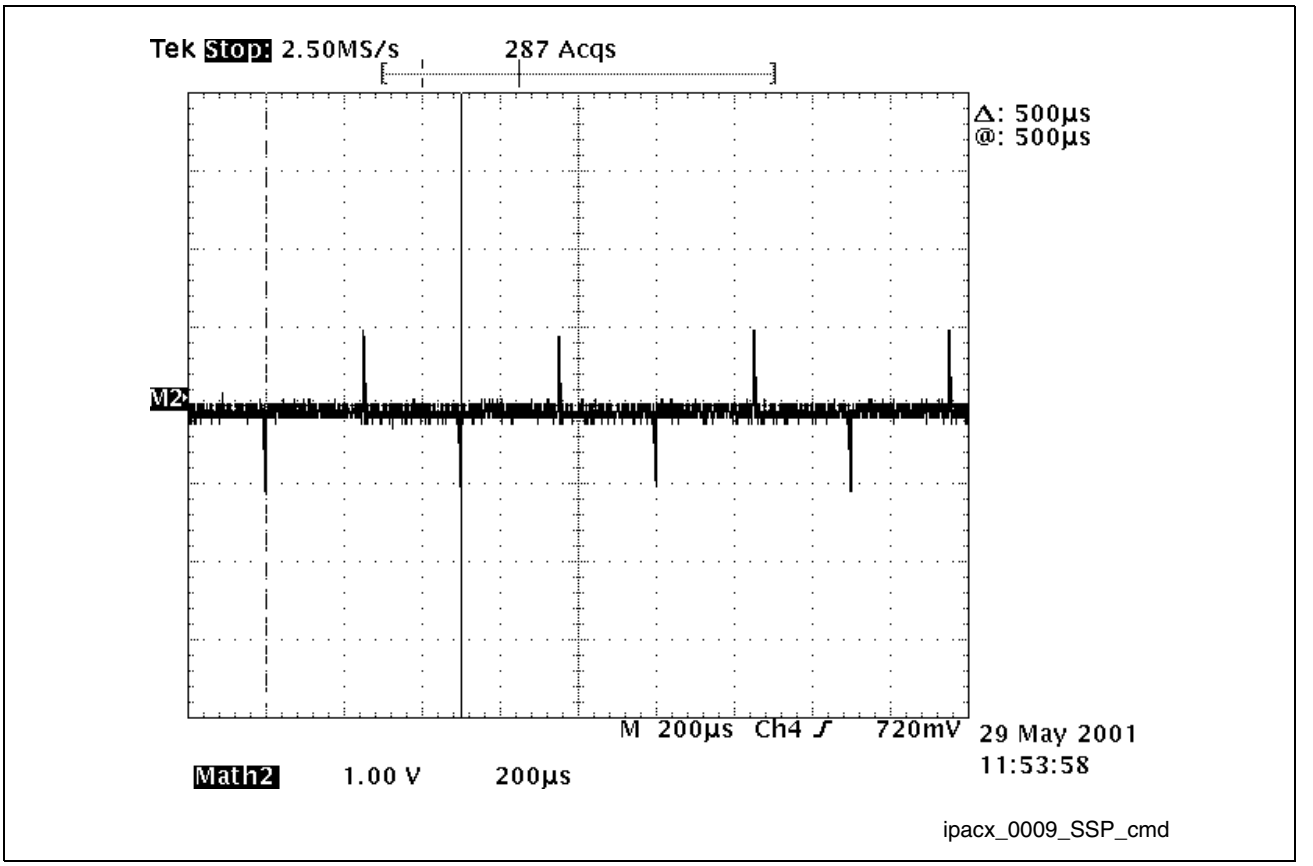


Figure 9 Screenshot of Single Pulses (C/I Command: SSP)

Table 15 Programming Example for Single Pulses (unconditional command)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Single Pulse generation (TE / LT-T mode)	w CIX0 = **0010** 0001
Enable Single Pulse generation (NT / LT-S mode)	w CIX0 = **0010** 1110

1.4.2 Continuous Pulses

Continuous pulses are of alternating polarity, one S-interface bit period wide, but they are sent continuously. 48 pulses are transmitted in each frame resulting in a frequency of the fundamental mode of 96 kHz. Continuous pulses may be transmitted in all applications. The corresponding C/I command in TE, LT-S and LT-T applications is SCP (Send Continuous Pulses).

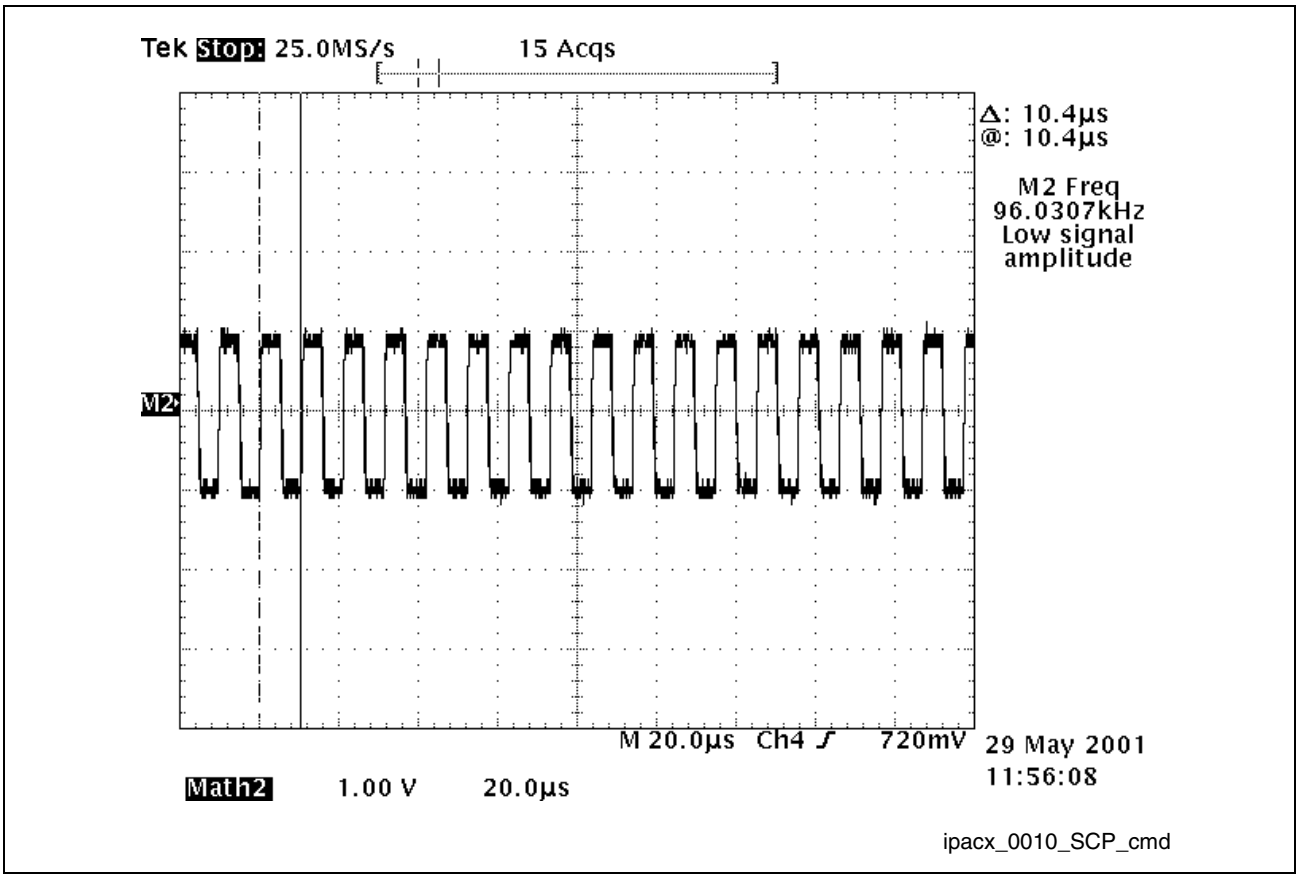


Figure 10 Screenshot of Continuous Pulses (C/I command: SCP)

Table 16 Programming Example for Continuous Pulses (unconditional command)

Description	3.3 V S-Transceivers (IPAC-X)
Enable Continuous Pulse generation (TE / LT-T mode)	w CIX0 = **0011** 0001
Enable Continuous Pulse generation (NT / LT-S mode)	w CIX0 = **0011** 1110