

## **Low Power Spread Spectrum Clock Multiplier**

### **FEATURES**

- FCC approved method of EMI attenuation
- Generates a **4X** low EMI spread spectrum signal of the input clock frequency
- Optimized for input frequency range from 10 to 35 MHz
- Internal loop filter minimizes external components and board space
- 2 selectable spread ranges
- Low inherent cycle-to-cycle jitter
- 3.3V operating voltage
- CMOS/TTL compatible inputs and outputs
- ***Ultra low power*** CMOS design  
TBD mA @3.3V, 40 MHz  
TBD mA @3.3V, 80 MHz  
TBD mA @3.3V, 120 MHz
- Pinout compatible to Cypress CY25814
- SSON/SBM pin for Spread Spectrum On/Off and Standby Mode controls
- Available in 8 pin SOIC and TSSOP

### **PRODUCT DESCRIPTION**

The P1814A is a spread spectrum frequency multiplier designed specifically to accept externally generated clock, crystal and ceramic resonator for input frequency range from 10 – 35MHz and outputs a 4X low EMI clock with frequency range from 40 – 140MHz. The P1814A reduces EMI at the clock source, allowing system wide reduction of EMI of down stream (clock and data dependent signals). The P1814A allows significant system cost savings by eliminating the use of expensive high frequency OSC and reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

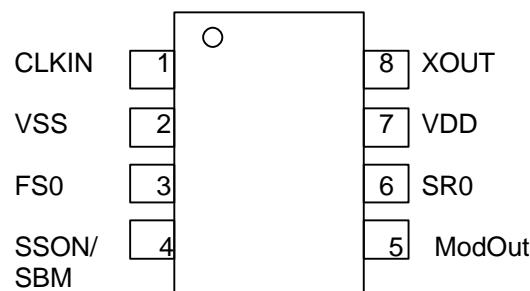
The P1814A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most clock generators. Lowering EMI by increasing a signal’s bandwidth is called “spread spectrum clock generation”.

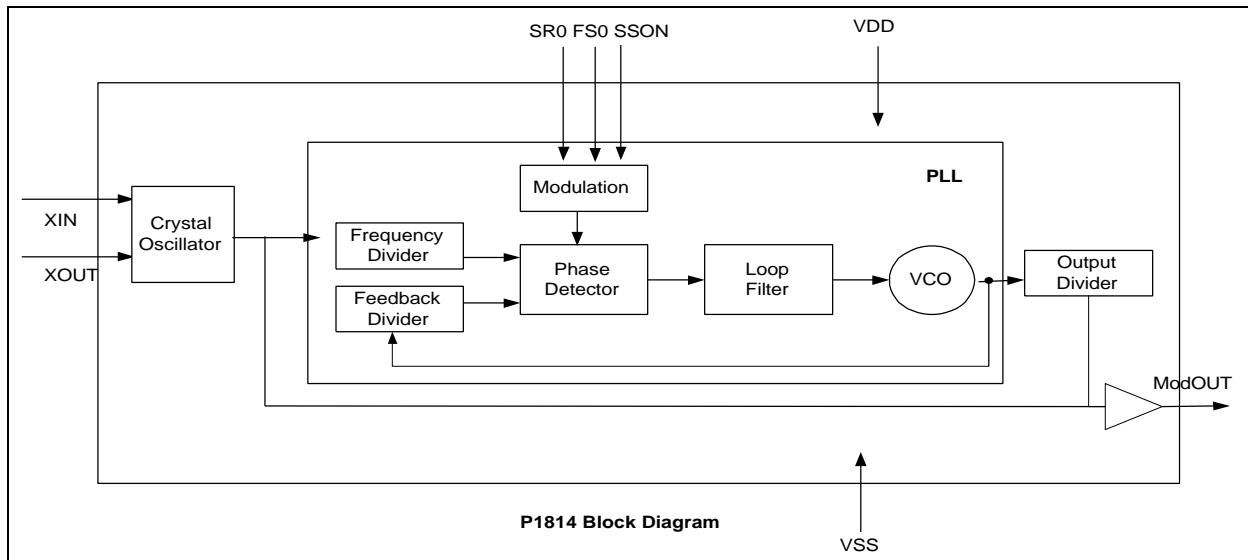
The P1814A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all-digital method.

### **APPLICATIONS**

The P1814A is targeted towards printers, MFPs, LCD scalers, Copiers, PDAs, storage devices, scanners, faxes, embedded processor, and DSP applications

**Figure 1 - P1814 Pin Diagram**



**Figure 2 - P1814A Block Diagram**

**Table 1- Standby Mode Selection**

<b>CLKIN</b>	<b>SSON/SBM</b>	<b>Spread Spectrum</b>	<b>ModOut</b>	<b>PLL</b>	<b>Mode</b>
Disabled	0	N/A	Disabled	Disabled	Standby
Disabled	1	N/A	Disabled	Free Running	Free Running
Enabled	0	OFF	Reference	Disabled	Buffer Out
Enabled	1	ON	4X	Normal	Normal

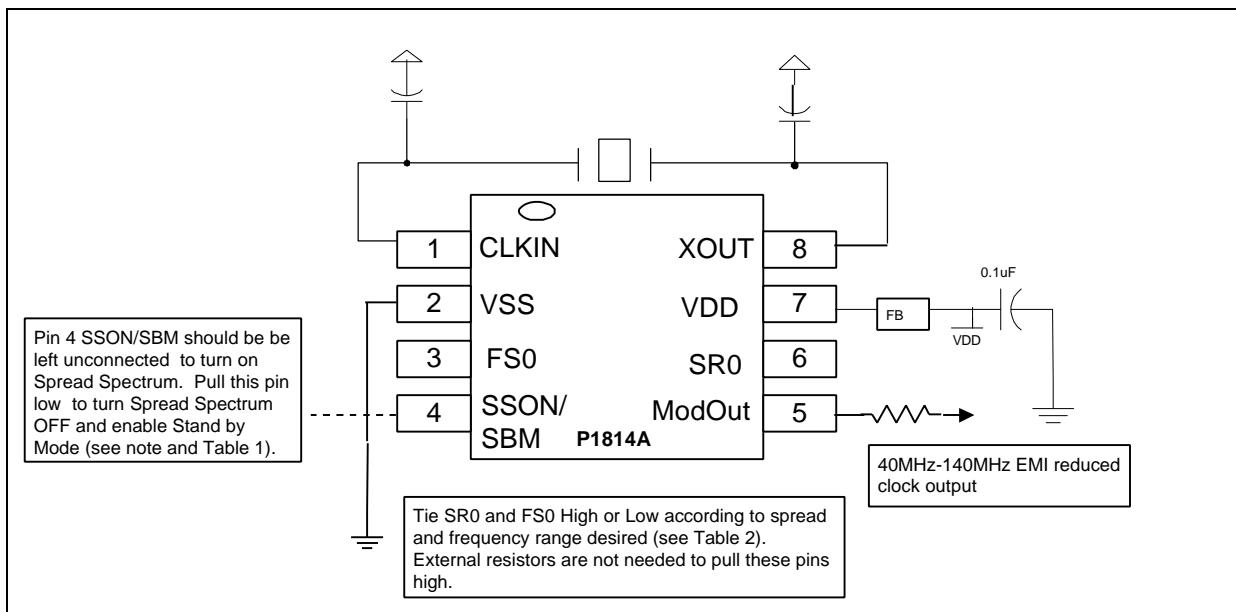
**Table 2 - Spread Range Selection**

<b>FS0</b>	<b>SR0</b>	<b>Spreading Range</b>	<b>Input Frequency</b>	<b>Output Frequency</b>	<b>Modulation rate</b>
1	0	+/- 1.25%	10 MHz to 20 MHz	40 MHz to 80 MHz	(Fin/10)*20.83 KHz
1	1	+/- 2.00%	10 MHz to 20 MHz	40 MHz to 80 MHz	(Fin/10)*20.83 KHz
0	0	+/- 1.25%	20 MHz to 35 MHz	80 MHz to 140 MHz	(Fin/10)*20.83 KHz
0	1	+/- 2.00%	20 MHz to 35 MHz	80 MHz to 140 MHz	(Fin/10)*20.83 KHz

#### PIN DESCRIPTION

<b>PIN #</b>	<b>Name</b>	<b>Type</b>	<b>Description</b>
1	CLKIN	I	Connect to externally generated clock signal. To put the part into Standby Mode, disable the input clock signal to this pin and pull SSON/SBM (Pin 4) low (see Table 1).
2	VSS	P	Ground Connection. Connect to system ground.
3	FS0	I	Digital logic input used to select Frequency Range (see Table 2). This pin has an internal pull-up resistor.
4	SSON/SBM	I	Spread Spectrum On / Off and Standby Mode control (see Table 1). This pin has an internal pull-up resistor.
5	ModOUT	O	4X Spread Spectrum clock output or Reference output of the input frequency (see Table 1).
6	SR0	I	Digital logic input used to select Spreading Range (see Table 2). This pin has an internal pull-up resistor.
7	VDD	P	Connect to +3.3V
8	XOUT	I	Connect to crystal. No connect if externally generated clock signal is used.

**Figure 3 - Schematic for General Application**



**Note:** To set the P1814A into Standby Mode, disable the input clock (CLKIN, Pin1) and also pull SSON/SBM (Pin 4) low (see Table 1).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V <sub>DD</sub> , V <sub>IN</sub>	Voltage on any pin with respect to GND	-0.5 to +7.0	V
T <sub>STG</sub>	Storage Temperature	-65 to +125	°C
T <sub>A</sub>	Operating Temperature	0 to +70	°C

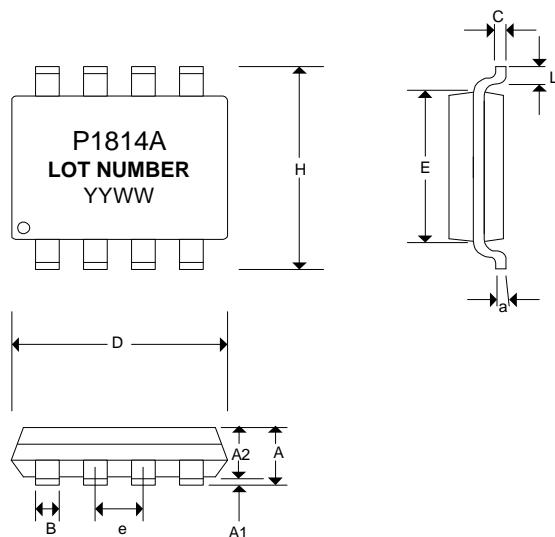
DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>IL</sub>	Input Low Voltage	GND – 0.3	-	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>DD</sub> + 0.3	V
I <sub>IL</sub>	Input Low Current (pull-up resistor on inputs SR0, 1)	-	-	-35	µA
I <sub>IH</sub>	Input High Current (pull-down resistor on input SSON)	-	-	35	µA
I <sub>XOL</sub>	XOUT Output Low Current (@ 0.4V, V <sub>DD</sub> = 3.3V)	-	3	-	mA
I <sub>XOH</sub>	XOUT Output High Current (@ 2.5V, V <sub>DD</sub> = 3.3V)	-	3	-	mA
V <sub>OL</sub>	Output Low Voltage (V <sub>DD</sub> =3.3V, I <sub>OL</sub> = 20 mA)	-	-	0.4	V
V <sub>OH</sub>	Output High Voltage (V <sub>DD</sub> =3.3V, I <sub>OH</sub> = 20 mA)	2.5	-	-	V
I <sub>DD</sub>	Static Supply Current Standby Mode	-	TBD	-	mA
I <sub>CC</sub>	Dynamic Supply Current Normal Mode (3.3V and 10 pF loading)	TBD f <sub>OUT</sub> -min	TBD f <sub>OUT</sub> -typ	TBD f <sub>OUT</sub> -max	mA
V <sub>DD</sub>	Operating Voltage	2.7	3.3	3.7	V
t <sub>ON</sub>	Power Up Time (First locked clock cycle after power up)	-	0.18	-	µs
Z <sub>OUT</sub>	Clock Output Impedance	-	50	-	Ω

AC ELECTRICAL CHARACTERISTICS

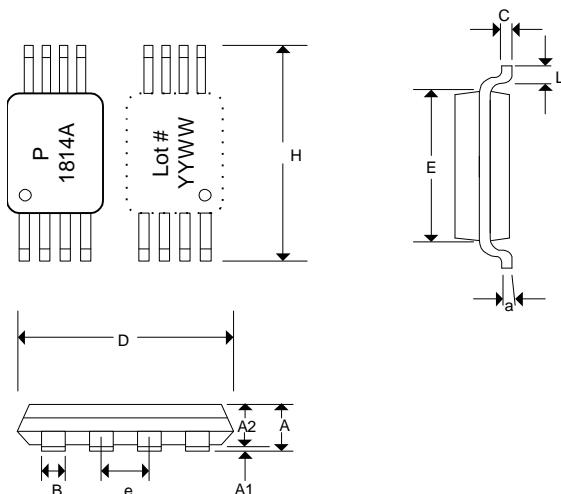
Symbol	Parameter	Min	Typ	Max	Unit
f <sub>IN</sub>	Input Frequency	10	20	35	MHz
f <sub>OUT</sub>	Spread Spectrum Output Frequency	40	80	140	MHz
t <sub>LH</sub> Note 1	Output Rise Time (measured at 0.8V to 2.0V)	0.7	0.9	1.1	ns
t <sub>HL</sub> Note 1	Output Fall Time (measured at 2.0V to 0.8V)	0.6	0.8	1.0	ns
t <sub>JC</sub>	Jitter (cycle to cycle)	-	-	360	ps
t <sub>D</sub>	Output Duty Cycle	45	50	55	%

Note1: t<sub>LH</sub> and t<sub>HL</sub> are measured into a capacitive load of 15pF

**Figure 4 - Mechanical Package Outline (8 Pin SOIC)**


SYMBOL	INCHES			MILLIMETERS		
	MIN	NOR	MAX	MIN	NOR	MAX
A	0.057	0.064	0.071	1.45	1.63	1.80
A1	0.004	0.007	0.010	0.10	0.18	0.25
A2	0.053	0.061	0.069	1.35	1.55	1.75
B	0.012	0.016	0.020	0.51	0.41	0.31
C	0.004	0.006	0.001	0.10	0.15	0.25
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.164	3.75	3.95	4.15
e	0.050 BSC			1.27 BSC		
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.012	0.020	0.028	0.30	0.50	0.70
a	0°	5°	8°	0°	5°	8°

Note: Controlling dimensions are millimeters.

**Figure 5 - Mechanical Package Outline (8 Pin TSSOP)**


SYMBOL	INCHES			MILLIMETERS		
	MIN	NOR	MAX	MIN	NOR	MAX
A	-	-	0.047	-	-	1.10
A1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.012	0.19	-	0.30
C	0.004	-	0.008	0.09	-	0.20
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0°	-	8°	0°	-	8°

Note: Controlling dimensions are millimeters.



**PRELIMINARY Specification**

**P1814A**

---

**ORDERING INFORMATION**

---

Ordering Number	Marking	Package Type	Qty. / Reel	Temperature
P1814A-08ST	P1814A	8 PIN SOIC, TUBE		0°C TO 70°C
P1814A-08SR	P1814A	8 PIN SOIC, TAPE & REEL	2,500	0°C TO 70°C
P1814A-08TT	P1814A	8 PIN TSSOP, TUBE		0°C TO 70°C
P1814A-08TR	P1814A	8 PIN TSSOP, TAPE & REEL	2,500	0°C TO 70°C

"Licensed under U.S. Patent Nos. 5,488,627 and 5,631,920"