PDSP16350

I/Q Splitter/NCO

DS3711 ISSUE 2.3 September 1996

The PDSP16350 provides an integrated solution to the need for very accurate, digitised, sine and cosine waveforms. Both these waveforms are produced simultaneously, with 16 bit amplitude accuracy, and are synthesised using a 34 bit phase accumulator. The more significant bits of this provide 16 bits of phase accuracy for the sine and cosine look up tables.

With a 20 MHz system clock, waveforms up to 10 MHz can be produced, with 0.001 Hz resolution. If frequency modulation is required with no discontinuities, the phase increment value can be changed linearly on every clock cycle. Alternatively absolute phase jumps can be made to any phase value.

The provision of two output multipliers allows the sine and cosine waveforms to be amplitude modulated with a 16 bit value present on the input port. This option can also be used to generate the in-phase and quadrature components from an incoming signal. This I/Q split function is required by systems which employ complex signal processing.

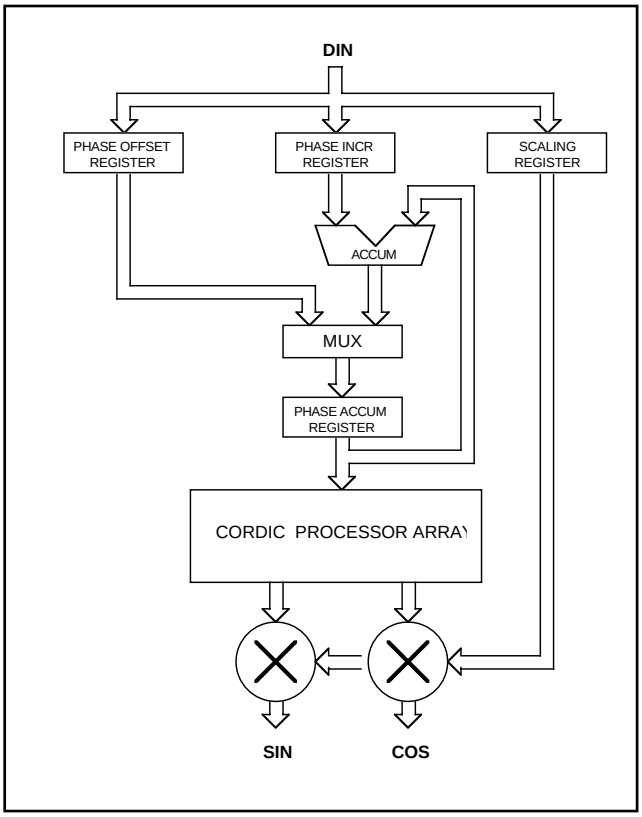

Fig. 1 Block Diagram

FEATURES

- Direct Digital Synthesiser producing simultaneous sine and cosine values
- 16 bit phase and amplitude accuracy, giving spur levels down to - 90 dB
- Synthesised outputs from DC to 10 MHz with accuracies better than 0.001 Hz
- Amplitude and Phase modulation modes
- 84 pin PGA or 132 pin QFP

APPLICATIONS

- Numerically controlled oscillator (NCO)
- Quadrature signal generator
- FM, PM, or AM signal modulator
- Sweep Oscillator
- High density signal constellation applications with simultaneous amplitude and phase modulation
- VHF reference for UHF generators
- Signal demodulator

ASSOCIATED PRODUCTS

PDSP16256/A Programmable FIR Filter

PDSP16510A FFT Processor

PDSP16488A 2D Convolver

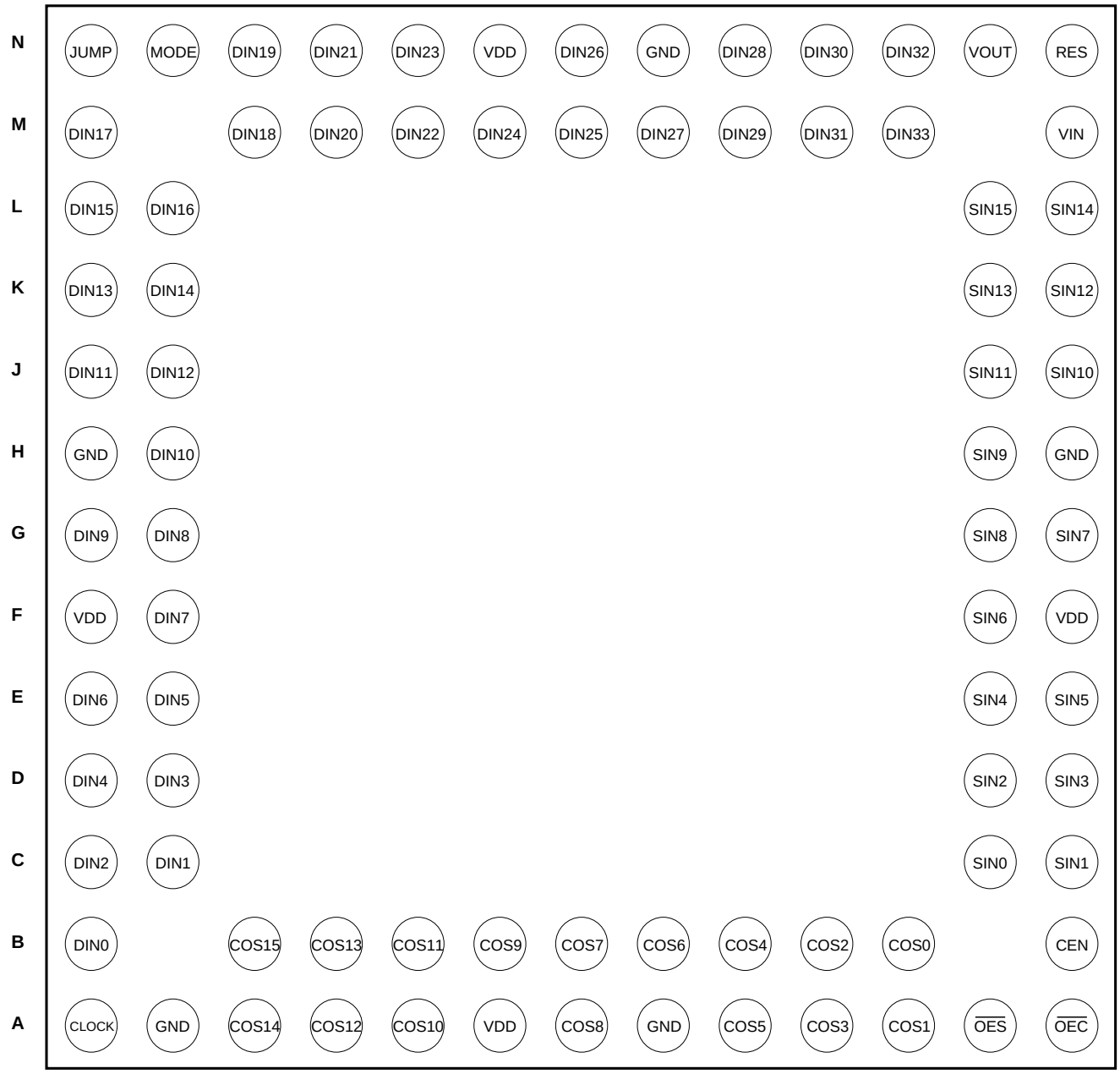

Fig. 2 A. Pin out - bottom view (84 pin PGA - AC84)

GC	SIG	GC	SIG	GC	SIG	GC	SIG
1	N/C	34	N/C	67	GND	100	GND
2	$\overline{\text{CEN}}$	35	VOUT	68	DIN17	101	VDD
3	N/C	36	DIN33	69	N/C	102	GND
4	SIN0	37	GND	70	DIN16	103	N/C
5	SIN1	38	VDD	71	DIN15	104	COS15
6	SIN2	39	DIN32	72	GND	105	COS14
7	GND	40	N/C	73	VDD	106	N/C
8	VDD	41	DIN31	74	DIN14	107	COS13
9	SIN3	42	DIN30	75	DIN13	108	COS12
10	SIN4	43	N/C	76	DIN12	109	N/C
11	N/C	44	DIN29	77	N/C	110	COS11
12	SIN5	45	DIN28	78	DIN11	111	N/C
13	SIN6	46	N/C	79	DIN10	112	COS10
14	N/C	47	DIN27	80	N/C	113	COS9
15	SIN7	48	GND	81	DIN9	114	VDD
16	SIN8	49	VDD	82	GND	115	GND
17	VDD	50	DIN26	83	VDD	116	COS8
18	GND	51	DIN25	84	DIN8	117	COS7
19	SIN9	52	DIN24	85	DIN7	118	N/C
20	N/C	53	DIN23	86	DIN6	119	COS6
21	SIN10	54	VDD	87	N/C	120	COS5
22	SIN11	55	DIN22	88	DIN5	121	N/C
23	N/C	56	GND	89	N/C	122	COS4
24	SIN12	57	DIN21	90	DIN4	123	N/C
25	SIN13	58	VDD	91	DIN3	124	COS3
26	SIN14	59	DIN20	92	VDD	125	COS2
27	VDD	60	DIN19	93	GND	126	N/C
28	GND	61	GND	94	DIN2	127	COS1
29	SIN15	62	VDD	95	DIN1	128	VDD
30	VIN	63	DIN18	96	N/C	129	GND
31	N/C	64	MODE	97	DIN0	130	COS0
32	N/C	65	JUMP	98	N/C	131	$\overline{\text{OES}}$
33	RESET	66	VDD	99	CLK	132	$\overline{\text{OEC}}$

Fig.2B Pin out (132 pin ceramic QFP - GC132)

SIGNAL	DESCRIPTION
DIN33:0	Data bus for the input register. This input register provides a 34 bit, incremental or absolute, phase value, if the mode pin is low. Alternatively if the mode pin is high, it provides either an 18 bit phase increment value, via D17:0, and a 16 bit scale value via D33:18 or a 34 bit phase increment value depending on the JUMP input see below.
SIN15:0	16 bit sine output data in fractional two's complement format.
COS15:0	16 bit cosine output data in fractional two's complement format.
$\overline{CEN}$	Clock enable for the data input register. When low, data will be latched on the rising edge of the clock. When high data will be retained in the input register.
MODE	Mode control input. When low, data in the input register is interpreted as either a 34 bit phase increment value or a 34 bit absolute phase value. When high, the output multipliers are enabled and will scale the waveforms with the upper 16 bits in the input register. The phase increment is loaded from the the lower 18 bits. The full 34 bit phase increment register can also be loaded using JUMP see below.
JUMP	With MODE low (Frequency or Phase Modulation) When low JUMP will allow normal phase incrementing to occur. When high, the data on the input pins will be interpreted as a 34 bit absolute phase value to replace the present value in the accumulator. JUMP is internally latched to match the delay through the data input register, and to allow data in the internal pipeline to be correctly processed. $\overline{CEN}$ must also be low to latch the required data from DIN. When Mode is high (Amplitude Modulation) When low JUMP will allow normal phase incrementing to occur, with the phase increment value taken from the lower 18 data inputs. When high, the data on the input pins will replace the full 34 bits of the phase increment register. $\overline{CEN}$ must also be low to latch the required data.
RES	When high will clear the phase accumulator and phase increment registers, after data in the internal pipeline has been correctly processed.
CLK	Input clock.
$\overline{OES}$	Output enable for SIN 15:0. Outputs are high impedance when $\overline{OES}$ is high.
$\overline{OEC}$	Output enable for COS15:0. Outputs are high impedance when $\overline{OEC}$ is high.
VIN	Valid input flag. A delayed version of this input is available on the VOUT pin, with the delay matching the data processing pipeline delay. This input has no other internal function.
VOUT	Valid output flag. See above.
GND	Five ground pins. All must be connected.
VCC	Four +5V pins. All must be connected.

Table 1. Pin Description

DEVICE OPERATION

Sine and cosine are simultaneously produced by the Cordic processor, which is addressed by the upper 16 bits of the output from a 34 bit phase accumulator. The accumulator divides the digital phase circle into a number of steps, one step for each state of the accumulator. When the accumulator reaches its maximum value it overflows back to zero and the sequence is repeated.

The accumulator is incremented once per incoming clock cycle, by an amount which defines the frequency which is to be generated. The increment required is defined by :

$$\text{Increment} = \frac{\text{Desired O/P Frequency}}{\text{Incoming Clock Frequency}} \times 2^N$$

where N is the number of bits in the accumulator. Since the Nyquist criteria for proper waveform reconstruction must still be obeyed, the maximum output frequency is half the incoming frequency. In practice, when a return is made to the analog world, just meeting the minimum Nyquist requirement would require a 'brick wall' low pass filter to remove the alias signals. A more useful 'rule of thumb' is to limit the generated waveforms to less than 40% of the clock frequency.

The resolution, or tuning sensitivity, of the waveform generator is given by :

$$\text{Resolution} = \frac{\text{Incoming Clock Frequency}}{2^N} \text{ Hz}$$

These equations illustrate some very important features of direct digital synthesisers :-

1) Tuning sensitivity is defined by both the number of bits in the accumulator and the incoming time base frequency.
2) The oscillator tunes linearly over its entire range.
3) The frequency accuracy matches the accuracy of the incoming increment value.
4) DC can be generated since the increment value can be zero.
5) Frequency stability will match the stability of the incoming frequency when the increment is fixed.

The residual noise characteristics of an oscillator are very important in modern communication systems. This parameter defines how well the device maintains its set frequency for very short periods (nanoseconds to seconds) of time. Poor figures will significantly affect the system signal to noise ratio and limit the dynamic range.

The PDSP16350 will, of course, inherit the residual noise characteristics of the source of the incoming frequency. The output frequency is, however, always less than half the incoming frequency in order to satisfy the Nyquist criterion. This is in contrast to a phase locked loop synthesiser, when a small input frequency controls a high output frequency.

The commonly used 20 log N rule states that the phase noise at the output of a synthesiser will be no better than twenty times the log of the ratio of the output frequency to the input frequency. In a phase locked loop synthesiser N is large, in the PDSP16350 it is less than half. Log N is thus less than zero and phase noise improvement is obtained.

The output waveforms are produced after a pipeline delay with respect to the DIN inputs. The effects of the JUMP or RES commands are delayed such that all data in the internal pipe will be processed before the discontinuity occurs. New data may be presented to the device on the cycle following the JUMP or RES and a valid result will be obtained after 31 clock cycles.

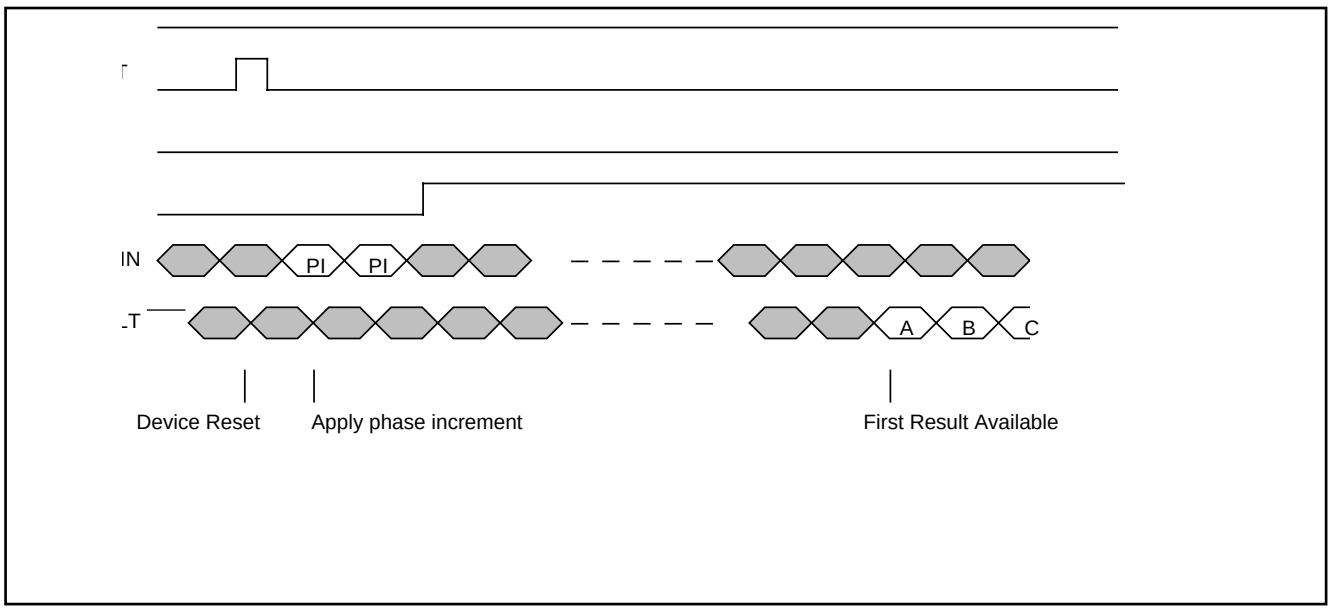

Fig. 3 Fixed Frequency Timing Diagram

USING THE PDSP16350

Frequency, phase, and amplitude modulation are all possible with the PDSP16350. The former two requirements are satisfied by the ability to change the phase increment value on every clock cycle. The latter needs the addition of two multipliers, which allow both sine and cosine to be modified by an incoming waveform.

Fixed Frequency, Constant Amplitude

To generate sine and cosine outputs at a fixed frequency, the MODE pin should be tied low, see Fig. 3. The phase increment value required to generate the desired frequency should be clocked into the internal phase increment register. This value is entered via the DIN port with $\overline{CEN}$ low. If $\overline{CEN}$ subsequently goes inactive (high), the value need not be maintained on the input pins.

The correct phase increment value can be calculated as follows :

$$\text{DIN value} = \frac{\text{Desired O/P Frequency}}{\text{Clock Frequency}} \times 2^{34}$$

This will give a decimal value which must be converted to a 34 bit binary number. The frequency resolution of the generated waveforms will be :

$$\text{Resolution} = \frac{\text{Clock Frequency}}{2^{34}} \quad \text{Hz}$$

With a 20 MHz clock this results in a frequency resolution of 0.001 Hz. This can be improved by reducing the clock frequency, with the Nyquist restraint being the limiting factor. The latter states that the frequency of the generated waveform must be no more than 50% of the input clock. In practice 40% is a better limit to use, as previously discussed.

A practical example can be used to illustrate the calculation. With a clock frequency of 10.73864 MHz, and the need to generate an output frequency of 20 kHz, then the above equation tells us we need a DIN value of 31996359. This corresponds to a binary value of:

DIN33:0 = 00 0000 0001 1110 1000 0011 1001 1100 0111

The resolution would be 0.0006 Hz. It should be noted that the accuracy of the PDSP16350 cannot be any better than the accuracy of the incoming clock, and these resolutions are based on perfect incoming waveforms.

Fixed Frequency, Modulated Amplitude

The MODE pin should be high if modulation of the output waveforms is required. In this mode each of the output waveforms is multiplied by the 16 bit, two's complement, value, present on the most significant 16 bits of the DIN port. The phase increment register is normally loaded with the 18 bit value on the least significant portion of the DIN bus. It is also possible to load the full 34 bits of the phase increment register when greater accuracy is required, this is explained below. When using the full 34 bits it is possible to obtain the same frequency resolution as in the fixed amplitude mode described earlier. When using 18 bit accuracy directly from the DIN bus the correct phase increment value can be calculated as follows :

$$\text{DIN value} = \frac{\text{Desired O/P Frequency}}{\text{Clock Frequency}} \times 2^{18}$$

The frequency resolution is correspondingly reduced and given by :

$$\text{Resolution} = \frac{\text{Clock Frequency}}{2^{18}} \quad \text{Hz}$$

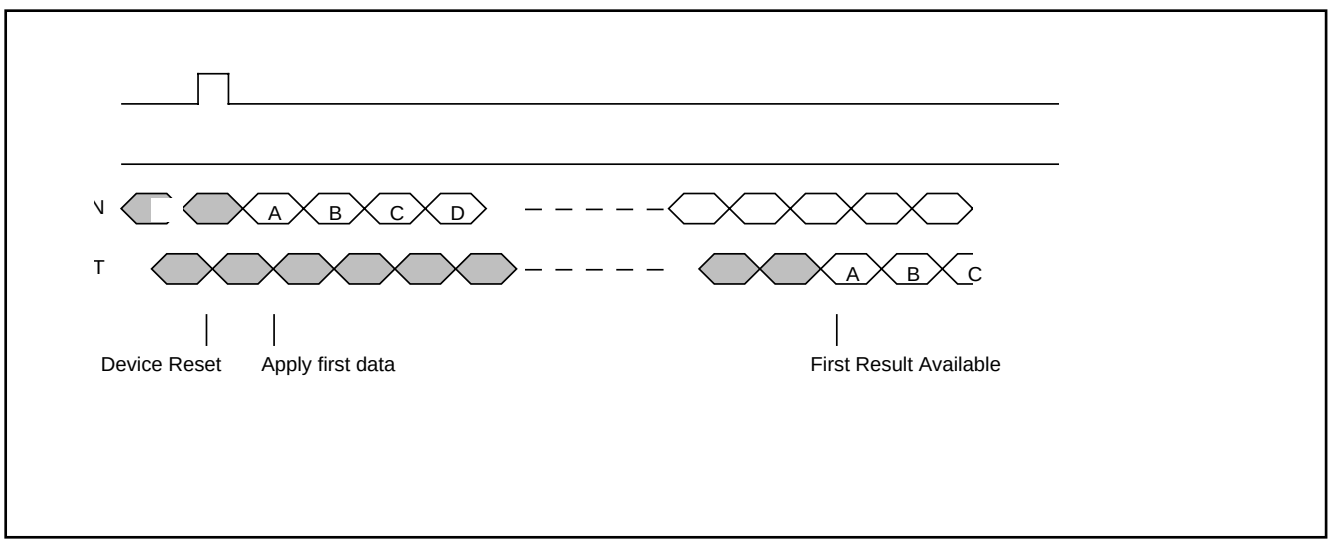

Fig. 4 Amplitude Modulation (18bit frequency accuracy)

Fig. 4 shows the operation of the device when loading the phase increment directly from the DIN bus. First the device must be reset then data is presented on each clock cycle. The amplitude modulation value is presented on the most significant 16 bits while the phase increment is presented on the least significant 18 bits. The first valid result is obtained after 31 cycles. (In this mode the least significant 16 bits of the phase increment register remain low).

Fig.6 shows the operation of the device when using the full 34 bits of the phase increment register. First the device must be reset, then the full 34 bits of the phase increment register are loaded from the DIN bus by taking signal JUMP high before the rising edge of the clock. Following this new data can be presented on each cycle of the clock. The amplitude modulation value is presented on the most significant 16 bits while the phase increment is presented on the least significant 18 bits. The least significant 16 bits of the phase increment register remain fixed at the value loaded using JUMP. The first valid result is obtained after 31 cycles. When using JUMP to load the phase increment register, normal operation cannot be maintained. This is because the amplitude modulation value normally presented on the most significant 16 bits of the DIN bus are replaced by part of the new phase increment value.

The AM mode is useful in systems requiring frequency sweeps. By varying the amplitudes at different frequencies, it is possible to compensate for the analog gain characteristics of amplifiers further along in the system.

It can also be used to generate the in-phase and quadrature components of an analog waveform, which has been digitized and which is to be processed using complex techniques. Such a quadrature heterodyning system, alternatively known as an IQ splitter, is shown in Fig. 5.

The output from an A/D converter drives the D33:18 inputs of the PDSP16350. If all sixteen inputs are not required, the unused least significant bits should be tied to ground, and the more significant inputs connected to the A/D converter. Multiplying an input signal with a local oscillator in this manner produces both sum and difference components. The former can be removed by using the PDSP16256 Programmable FIR Filter.

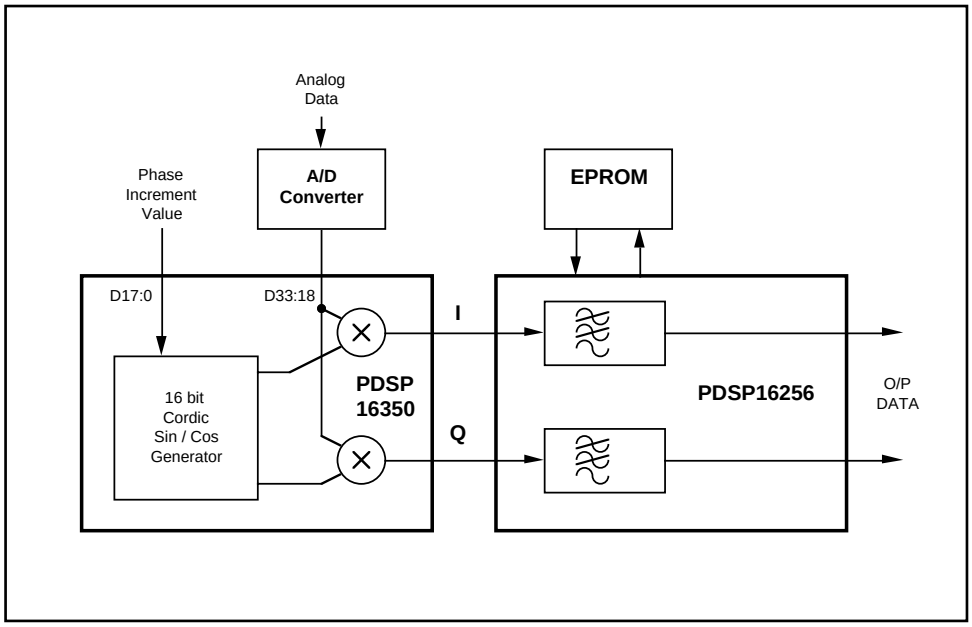

Fig. 5 IQ Split Function

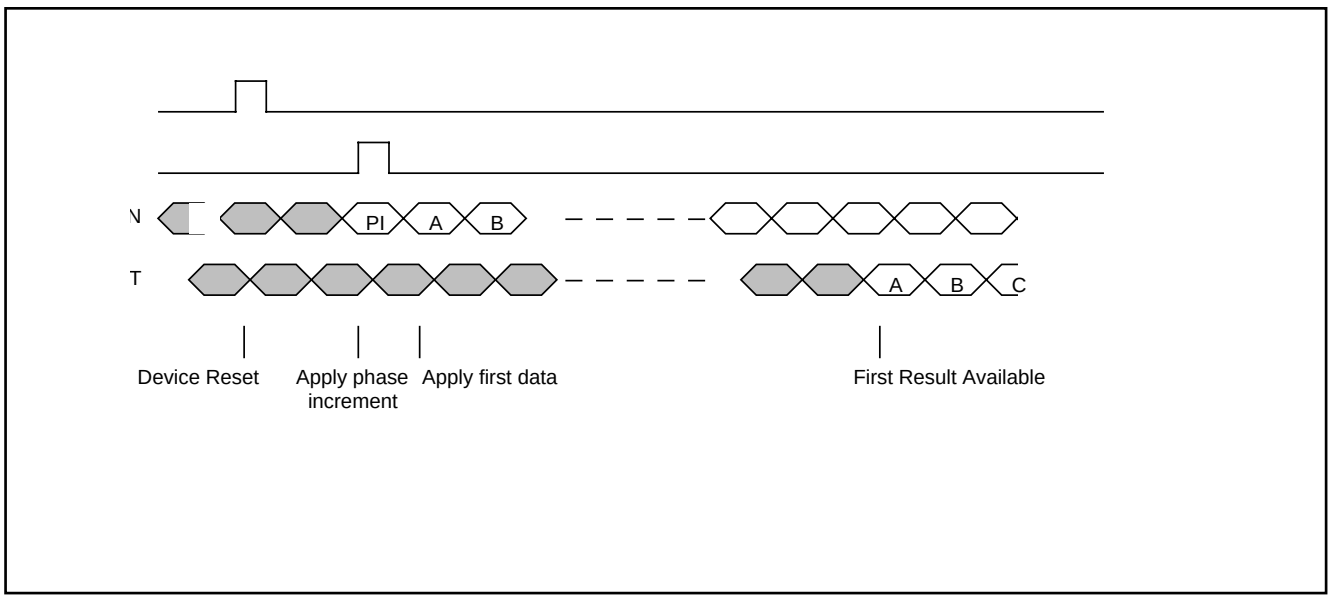

Fig. 6 Amplitude Modulation (34bit frequency accuracy)

Modulated Frequency

The output frequency can be modulated very simply, see Fig 8. Since the phase increment value can be loaded as a complete word every cycle, there is no need to provide internal double buffering to prevent spurious frequencies being generated during the load operation. Binary Frequency Shift Keyed (BFSK) modulation can easily be implemented by externally multiplexing between two phase increment values representing the two frequencies to be used. The value to be used can be instantaneously changed, thus maintaining phase coherence, whilst the bit to be transmitted changes from a mark to a space. Frequency hopping could also be simply effected by clocking a new random number into the DIN port once every thousand cycles, for instance. The output will reflect any change in the frequency after 31 system clock cycles.

If the phase increment value on the DIN port is changed on each clock cycle, then the output frequency will change without introducing any discontinuities. Thus, a linear frequency sweep can be achieved by incrementing the value on the DIN port by a fixed amount each cycle. Alternatively, a logarithmic sweep could be implemented by 'walking' a one across the DIN port. Shifting the input one place to the left every hundred cycles, for example, would double the frequency every time.

Chirp generation for FM - CW Radar systems is a typical example of the need for linear frequency sweeps. This application requires the generation of quadrature chirp waveforms and is illustrated in simplified form by Fig. 7. One waveform is needed for the transmitter, and the other for the receiver. The phase increment value is supplied by the counter block which simply increments at a rate determined by dividing down the time base clock. The synthesised frequency thus increases during the sweep period.

A number of the more significant phase increment bits are used to supply the addresses to a PROM. The output of this PROM is used to amplitude modulate the sine and cosine waveforms. In this manner it is possible to compensate, at the source, for any poor frequency versus gain characteristics of analog circuits further along in the system.

The digital outputs directly drive two D/A converters. Once in the analog world, it is necessary to remove the alias frequencies with low pass filters. The phase linearity and pass band ripple characteristics of these filters are very important, if the correct phase relationships are to be maintained between the two waveforms.

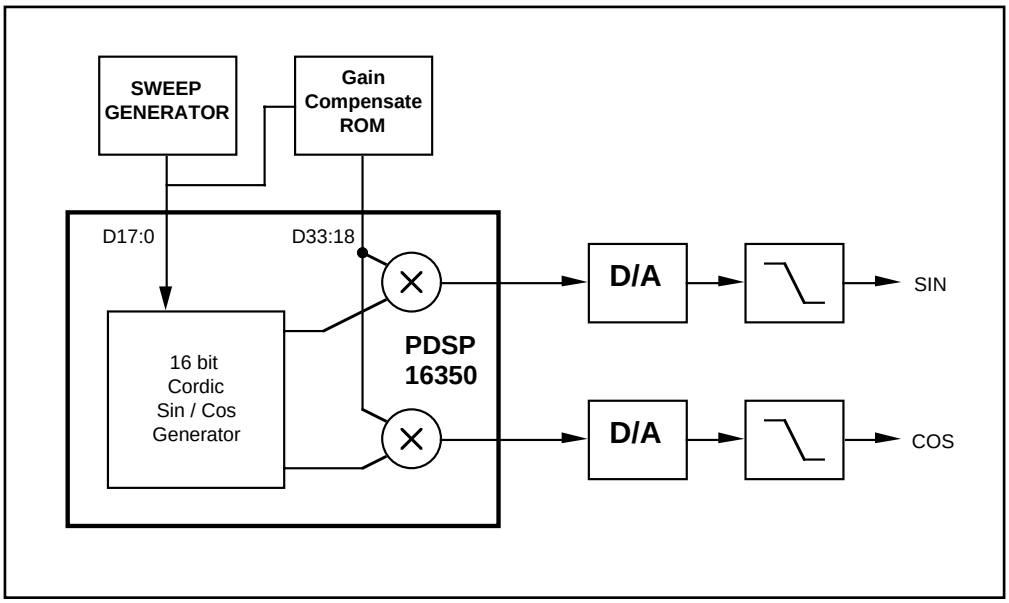

Fig. 7 Quadrature Chirp Generator

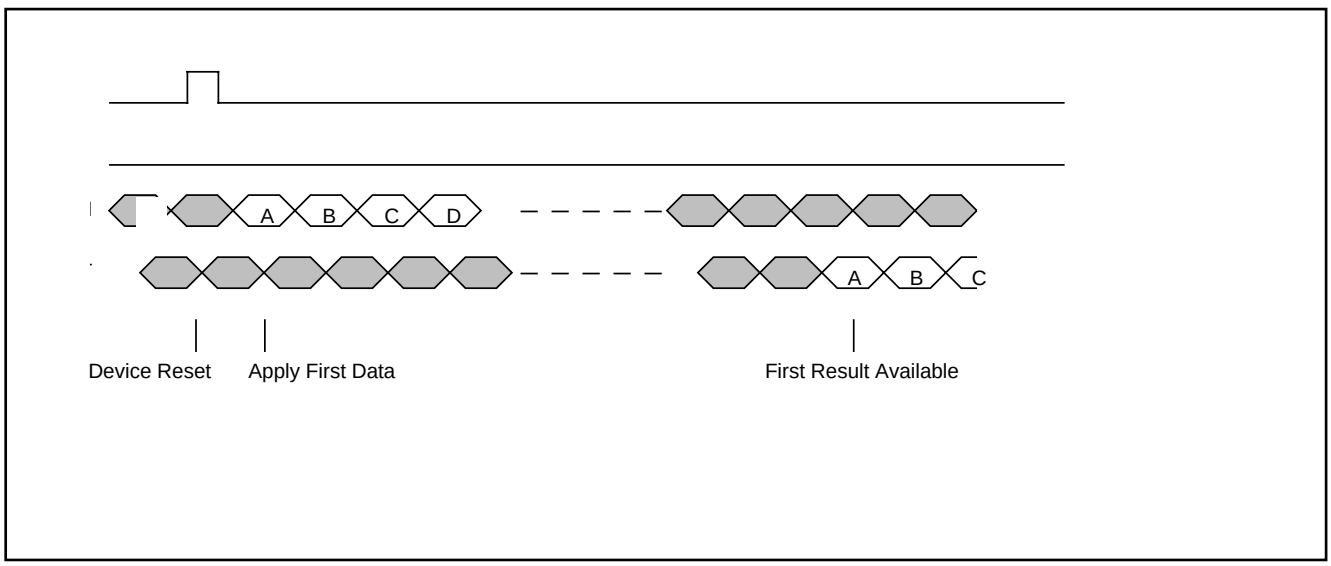

Fig. 8 Frequency Modulation Timing Diagram

Modulated Phase

Relative phase jumps may be made with or without amplitude modulation. For example, if a jump of 180 degrees is required, this can be done with a value of :

DIN33:0 = 10 0000 0000 0000 0000 0000 0000 0000 0000

This is loaded into the phase increment register for one cycle, then the normal increment value is re-loaded in the following cycle.

Alternatively, if no amplitude modulation is needed, an absolute jump to a phase value can be made, see Fig. 9. This can be done by activating the JUMP input during one cycle and also presenting the new phase value at the same time. For example, if a jump to 270 degrees is required :

DIN33:0 = 11 0000 0000 0000 0000 0000 0000 0000 0000

The RES (reset) input can alternatively be used if a jump to 0 degrees is needed. This avoids using the DIN inputs and can be used with or without amplitude modulation. The reset function is internally synchronised to the input clock.

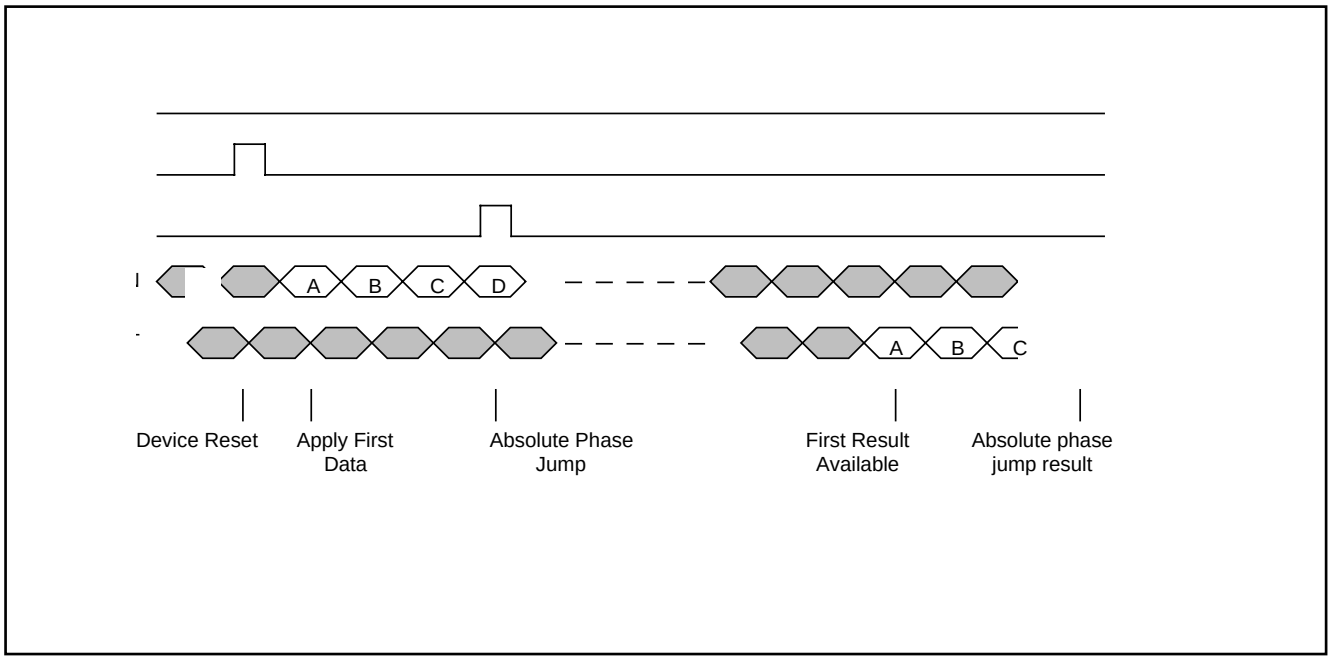

Fig. 9 Phase Modulation Timing Diagram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage Vcc	-0.5V to 7.0V
Input voltage V_{IN}	-0.5V to Vcc + 0.5V
Output voltage V_{OUT}	-0.5V to Vcc + 0.5V
Clamp diode current per pin I_K (see note 2)	18mA
Static discharge voltage (HMB)	500V
Storage temperature T_S	-65°C to 150°C
Ambient temperature with power applied T_{AMB}	
Military	-55°C to +125°C
Industrial	-40°C to 85°C
Junction temperature	150°C
Package power dissipation	3500mW
Thermal resistances	
Junction to Case $ø_{JC}$	5°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Vcc = Max, Outputs Unloaded, Clock Freq = Max.
5. CMOS levels are defined as
   $V_{IH} = V_{DD} - 0.5v$
   $V_{IL} = +0.5v$
6. Current is defined as positive into the device.
7. The $ø_{JC}$ data assumes that heat is extracted from the top face of the package.

ELECTRICAL CHARACTERISTICS

Operating Conditions (unless otherwise stated)

Commercial: T_{AMB} = 0°C to +70°C $T_{J(MAX)}$ = 95°C V_{CC} = 5.0V±5% Ground = 0V
Industrial: T_{AMB} = -40°C to +85°C $T_{J(MAX)}$ = 110°C V_{CC} = 5.0V±10% Ground = 0V
Military: T_{AMB} = -55°C to +125°C $T_{J(MAX)}$ = 150°C V_{CC} = 5.0V±10% Ground = 0V

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL} = -4mA
Input high voltage	V_{IH}	3.0		-	V	
Input low voltage	V_{IL}	-		0.8	V	
Input leakage current	I_{IN}	-10		+10	µA	GND < V_{IN} < V_{CC}
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	-50		+50	µA	GND < V_{OUT} < V_{CC}
Output S/C current	I_{SC}	40		250	mA	V_{CC} = Max

Switching Characteristics

Characteristic	Industrial			Military			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
D33:0 signal setup to clock rising edge	15		-	15		-	ns	
D33:0 signal hold after clock rising edge	4		-	4		-	ns	
CEN setup to clock rising edge	20		-	20		-	ns	
CEN hold after clock rising edge	0		-	0		-	ns	
JUMP, RES setup to clock rising edge	10		-	10		-	ns	
JUMP hold after clock rising edge	6		-	6		-	ns	
RES hold after clock rising edge	8		-	8		-	ns	
Clock rising edge to output valid	5		30	5		30	ns	30pF
Clock freq	DC		20	DC		20	MHz	
Clock High Time	15		-	15		-	ns	
Clock Low Time	20		-	20		-	ns	
$\overline{OES}$,$\overline{OEC}$ low to data valid	-		20	-		20	ns	30pF
$\overline{OES}$,$\overline{OEC}$ high to data high impedance	-		20	-		20	ns	30pF
Pipeline delay VIN to VOUT	31		31	31		31	CLKs	
Vcc Current (CMOS inputs)	-		430	-		450	mA	See Note 4
Vcc Current (TTL inputs)	-		460	-		500	mA	See Note 4

ORDERING INFORMATION

Industrial (-40°C to +85°C)

PDSP16350 / B0 / AC (20MHz - PGA)
PDSP16350 / B0/ GC (20MHz - QFP)

Military (-55°C to +125°C)

PDSP16350 / A0 / AC (20MHz - PGA)
PDSP16350 / A0/ GC (20MHz - QFP)

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