Precision 8-Ch, Diff. 4-Ch, Latchable Analog Multiplexers

Features

- Low On-Resistance (60Ω typ.) Minimizes Distortion and Error Voltages
- Low Glitching Reduces Step Errors and Improves Settling Times. Charge Injection, < 5pC
- Split-Supply Operation (±3V to ±8V)
- On-chip TTL Compatible Address Latches
- On-Resistance Matching Between Channels, < 6Ω
- On-Resistance Flatness, < 11Ω
- Low Off-Channel Leakage, $I_{NO(OFF)}$ < 1nA @ +85°C, $I_{COM(ON)}$, < 2.5nA @ +85°C
- TTL/CMOS Logic Compatible
- Fast Switching Speed, t_{TRANS} < 250ns
- Break-Before-Make action eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Range
- Low Power Consumption, < 300µW
- QSOP Package Minimizes Board Area

Applications

- Data Acquisition Systems
- Audio Switching and Routing
- Automatic Test Equipment
- Telecommunication Systems
- Medical Instrumentation

Description

The PS328/PS329 are improved high precision analog multiplexers. The PS328, an 8-channel single-ended mux, selects one of eight inputs to a common output as determined by a 3-bit address A0-A2. An EN (enable) pin when low disables all switches, useful when stacking several devices. The PS329 is a 4-channel differential multiplexer. It selects one of four differential inputs to a common differential output as determined by a 2-bit address A0, A1. An EN pin may be driven low to disable all switches.

On-chip address latches simplify interface in microprocessor controlled applications.

These multiplexers operate with dual supplies from +3V to +8V. Single-supply operation is possible from +3V to +15V.

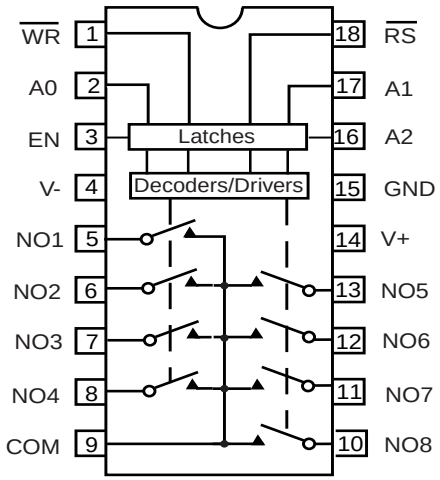
With +5V power supplies, the PS328/PS329 guarantee < 100Ω on-resistance. On-resistance matching between channels is within 6Ω. On-resistance flatness is less than 11Ω over the specified signal range.

Each switch conducts current equally well in either direction when on. In the off state each switch blocks voltages up to the power-supply rails.

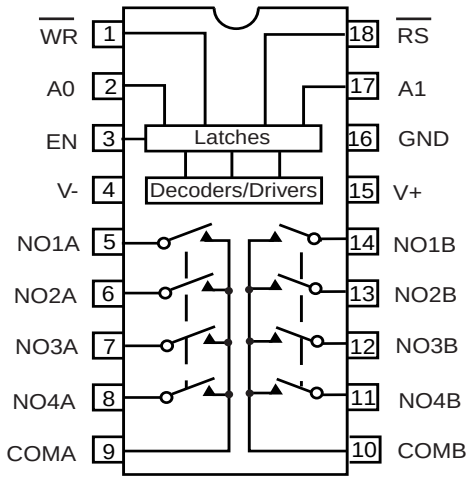
Both devices guarantee low leakage currents (< 2.5nA at +85°C) and fast switching speeds (t_{TRANS} < 250ns). Break-before-make switching action protects against momentary crosstalk between channels.

Functional Block Diagrams and Pin Configurations

Top View
PS328



Top View
PS329



Truth Tables

PS328						
A2	**A1**	**A0**	**EN**	**$\overline{WR}$**	**$\overline{RS}$**	**On Switch**
Latching						
X	X	X	X	↓	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	None (Latches cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Truth Tables

PS329					
A1	**A0**	**EN**	**$\overline{WR}$**	**$\overline{RS}$**	**On Switch**
Latching					
X	X	X	↓	1	Maintains previous switch condition
Reset					
X	X	X	X	0	None (latches cleared)
Transparent Operation					
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0", $V_{AL} \leq 0.8V$
Logic "1", $V_{AH} \geq 2.4V$
X = Don't Care

Ordering Information

Part Number	Temperature Range	Package
PS328EPE	-40ºC to +85ºC	18 Plastic DIP
PS328ESE		20 Wide SO
PS328EEE		20 QSOP

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PS329EPE	-40ºC to +85ºC	18 Plastic DIP
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Absolute Maximum Ratings

Voltages Referenced to V-

V+ ..... -0.3V to + 17V
GND ..... -0.3V to + 17V
GND ..... -0.3V to (V+) + 0.3V
V_{IN}, V_{COM}, V_{NO} (Note 1) ..... (V-) -2V to (V+) + 2V
or 30mA, whichever occurs first
Current (any terminal) 30mA
Peak Current, COM, NO, NC (pulsed at 1ms, 10% duty cycle) . 100mA
ESD per method 3015.7 ..... > 2000V

Thermal Information

Continuous Power Dissipation
Plastic DIP (derate 10.5mW/ ºC above +70ºC) 800mW
Wide SO (derate 8.7mW/ ºC above +70ºC) 650mW
Storage Temperature ..... -65ºC to +150ºC
Lead Temperature (soldering, 10s) ..... +300ºC

Note 1:
Signals on NO, COM, or logic inputs exceeding V+ or V are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Dual Supplies

(V ± = ±5V ±10%, GND = $\overline{WR}$ = 0V, V_{AH} = V_{ENH} = $\overline{RS}$ = 2.4V, V_{AL} = V_{ENL} = 0.8V)

Parameter	Symbol	Conditions		Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch								
Analog Signal Range (3)	V_{ANALOG}			Full	V-		V+	V
On Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, V_{COM} = ±3.5V I_{NO} = 1mA,		25		60	100	Ω
				Full			125	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V_{COM} or V_{NC} = ±3.5V, I_{NO} = 1mA, V+ = 5V, V- = -5V		25			6	
				Full			8	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{NO} = 1mA, V_{COM} = ±3V, 0V		25			11	
				Full			14	
NO Off Leakage Current(6)	$I_{NO(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} = ±4.5V		25	-0.1		0.1	nA
				Full	-1.0		1.0	
COM-Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V V_{COM} = ± 4.5V, V_{NO} = ±4.5V	PS328	25	-0.2		0.2	
				Full	-2.5		2.5	
			PS329	25	-0.1		0.1	
				Full	-1.5		1.5	
COM On Leakage Current(7)	$I_{COM(ON)}$	V_{COM} = ±4.5V V_{NO} = 4.5V	PS328	25	-0.4		0.4	
				Full	-5		5	
			PS329	25	-0.2		0.2	
				Full	-2.5		2.5	
Logic Input								
Logic High Input Voltage	V_{AH}, V_{ENH}			Full	2.4			V
Logic Low Input Voltage	V_{AL}, V_{ENL}						0.8	
Input Current with Input Voltage High	I_{AH}, I_{ENH}	V_A = V_{EN} = 2.4V			-0.1		0.1	µA
Input Current with Input Voltage Low	I_{AL}, I_{ENL}	V_A = V_{EN} = 0.8V			-0.1		0.1	

Electrical Specifications - Dual Supplies

(V ± = ±5V ± 10%, GND = $\overline{WR}$ = 0V, $V_{AH} = V_{ENH} = \overline{RS}$ = 2.4V, $V_{AL} = V_{ENL}$ = 0.8V)

Parameter	Symbol	Conditions		Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Dynamic								
Transition Time	t_{TRANS}	Figure 1		25			150	ns
Break-Before-Make TimeDelay	t_{OPEN}	Figure 3			0	40		
Enable and Write Turn-OnTime	$t_{ON(EN,WR)}$	Figure 2				60	150	
				Full			250	
Enable and Reset Turn-Off Time	$t_{OFF(EN, RS)}$	Figure 2		25		40	150	
				Full			200	
Charge Injection(3)	Q	C_L= 1nF, V_S = 0V, R_S = 0Ω,		25		2	5	pC
Off Isolation(7)	OIRR	V_{EN} = 0V, R_L= 1kΩ, f = 100kHz				-101		dB
Crosstalk	X_{TALK}	R_L = 1kΩ, f = 100kHz, Figure 8				-92		
Logic Input Capacitance	C_{IN}	f=1kHz				8		pF
NO Off Capacitance	$C_{NO(OFF)}$	f=1kHz, $V_{EN} = V_{NO}$ = 0V				11		
COM Off Capacitance	$C_{COM(OFF)}$	f=1kHz, $V_{EN} = V_{COM}$ =0V	PS328			40		
			PS329			20		
COM On Capacitance	$C_{COM(ON)}$	f=1kHz, V_{COM} = 0V	PS328			54		
			PS329			34		
Minimum Input Timing Requirements								
Write Pulse Width	t_W	See Figure 4		Full	<100			ns
A_X, EN Data Set Up Time	t_S				<100			
A_X, EN Data Hold Time	t_H				10			
Reset Pulse Width	t_{RS}	V_S = 5V, See Figure 5			<100			
Supply								
Power-Supply Range				Full	±3		±8	V
Positive Supply Current	I+	$V_{EN} = V_A$ = 0V or V+, V+ =5.5V, V- = -5.5V			-1		1	µA
NegativeSupply Current	I-				-1		1	
Ground Current	I_{GND}				-1		1	

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum values of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ V_{COM} / V_{NO} . See figure 7.

Electrical Specifications - Single 5V Supply

(V± = ±5V ± 10%, GND = $\overline{WR}$ = 0V, V_{AH} = V_{ENH} = $\overline{RS}$ = 2.4V, V_{AL} = V_{ENL} = 0.8V)

Parameter	Symbol	Conditions		Temp.(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Switch								
Analog Signal Range(3)	V_{COM}, V_{NO}			Full	0		V+	V
On Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		25		150	225	
				Full			280	
R_{ON} Matching Between Channels(4)	ΔR_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		25			11	Ω
				Full			13	
On -Resistance Flatness	R_{FLAT}	I_{NO} = 1mA, V_{COM} = 1.5V, 2.5V, 3.5V, V+ = 5V		25			18	
				Full			22	
NO-Off Leakage Current(8)	$I_{NO(OFF)}$	V_{NO} = 4.5V, V_{COM} = 0V, V+ = 5.5V		25	-0.1		0.1	nA
				Full	-1.0		1.0	
COM-Off Leakage Current(8)	$I_{COM(OFF)}$	V_{COM} = 4.5V, V_{NO} =0V, V+ = 5.5V	PS328	25	-0.2		0.2	
				Full	-2.5		2.5	
			PS329	25	-0.2		0.2	
				Full	-1.5		-1.5	
COM-On Leakage Current(8)	$I_{COM(ON)}$	V_{COM} = 4.5V, V_{NO} =4.5V, V+ = 5.5V	PS328	25	-0.4		-0.4	
				Full	-5		5	
			PS329	25	-0.2		0.2	
				Full	-2.5		2.5	
Digital Logic Input								
Logic High Input Voltage	V_{AH}, V_{ENH}			Full	2.4			V
Logic Low Input Voltage	V_{AH}, V_{ENL}						0.8	
Input Current with Input Voltage High	I_{AH}, I_{ENH}	V_A= V_{EN} = 2.4V			-0.1		0.1	µA
Input Current with Input Voltage Low	I_{AH}, I_{ENL}	V_A= V_{EN} = 0.8V			-0.1		0.1	
Supply								
Power-Supply Range	V+			Full	3		15	V
Positive-Supply Current	I+	V_{EN} = V+ or 0V, V_A = 0V, V+ = 5.5V, V- = 0V			-1.0		1.0	µA
Negative-Supply Current	I-				-1.0		1.0	
Ground Current	I_{GND}				-1.0		1.0	

Electrical Specifications - Single 5V Supply

($V\pm$ = ±5V ± 10%, GND = $\overline{WR}$ = 0V, $V_{AH} = V_{ENH} = \overline{RS}$ = 2.4V, $V_{AL} = V_{ENL}$ = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Dynamic							
Transition Time	t_{TRANS}	V_{NO} = 3V	25		90	245	ns
Break-Before-Make Interval	t_{OPEN}			10	40		
Enable Turn-OnTime	$t_{ON(EN)}$				90	200	
			Full			275	
Enable Turn-Off Time	$t_{OFF(EN)}$		25		50	125	
			Full			200	
Charge Injection (3)	Q	C_L = 1nF, V_S = 0V, R_S = 0Ω	25		1.5	5	pC
Minimum Input Timing Requirements							
Write Pulse Width	t_W	See Figure 4	Full	<100			ns
A_X, EN Data Set Up Time	t_S			<100			
A_X, EN Data Hold Time	t_H			10			
Reset Pulse Width	t_{RS}	V_S = 5V, See Figure 5		<100			

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM}/V_{NO}, V_{COM} = output, V_{NO} = input to off switch
8. Leakage testing at single supply is guaranteed by testing with dual supplies.

Electrical Specifications - Single 3V Supply

(V+ = +3V ±10%, V- = 0V, GND = $\overline{WR}$ = 0V, V_{AH} = V_{ENH} = $\overline{RS}$ = +2.4, V_{AL} = V_{ENL} = +0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Switch							
Analog Signal Range(3)	V_{ANALOG}		Full	0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 1.5V, V+ = 3V	25		230	375	Ω
			Full			425	
Dynamic							
Transition Time(3)	t_{TRANS}	Figure 1, V_{IN} = 2.4V V_{NO1} = 1.5V, V_{NO8} = 0V	25		230	575	ns
Enable Turn-OnTime(3)	$t_{ON(EN)}$	Figure 2, V_{INH} = 2.4V V_{INL} = 0V, V_{NO1} = 1.5V			200	500	
Enable Turn-Off Time(3)	$t_{OFF(EN)}$	Figure 2, V_{INH} = 2.4V V_{INL} = 0V, V_{NO1} = 1.5V			75	400	
Charge Injection (3)	Q	C_L = 10nF, V_S = 0V, R_S = 0Ω			1	5	pC
Minimum Timing Requirements							
Write Pulse Width	t_W	See Figure 4	Full	<100			ns
AX, EN Data Set Up time	t_S			<100			
AX, EN Data Hold time	t_H			10			
Reset Pulse Width	t_{RS}	VS = 5V, See figure 5		<100			

Notes:

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2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON}$ max - R_{ON} min
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM}/V_{NO}, V_{COM} = output, V_{NO} = input to off switch
8. Leakage testing at single supply is guaranteed by testing with dual supplies.

Test Circuits/Timing Diagrams

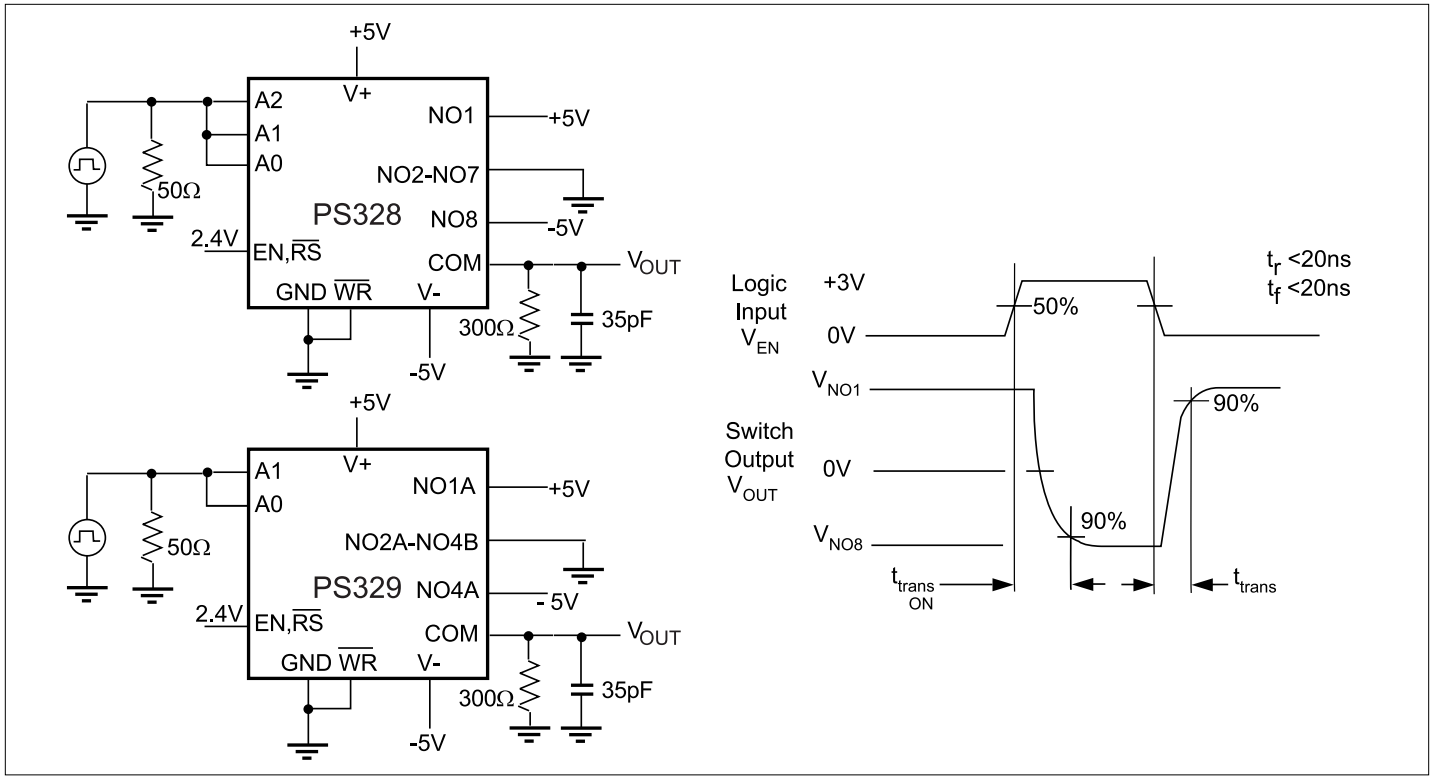

Figure 1. Transition Time

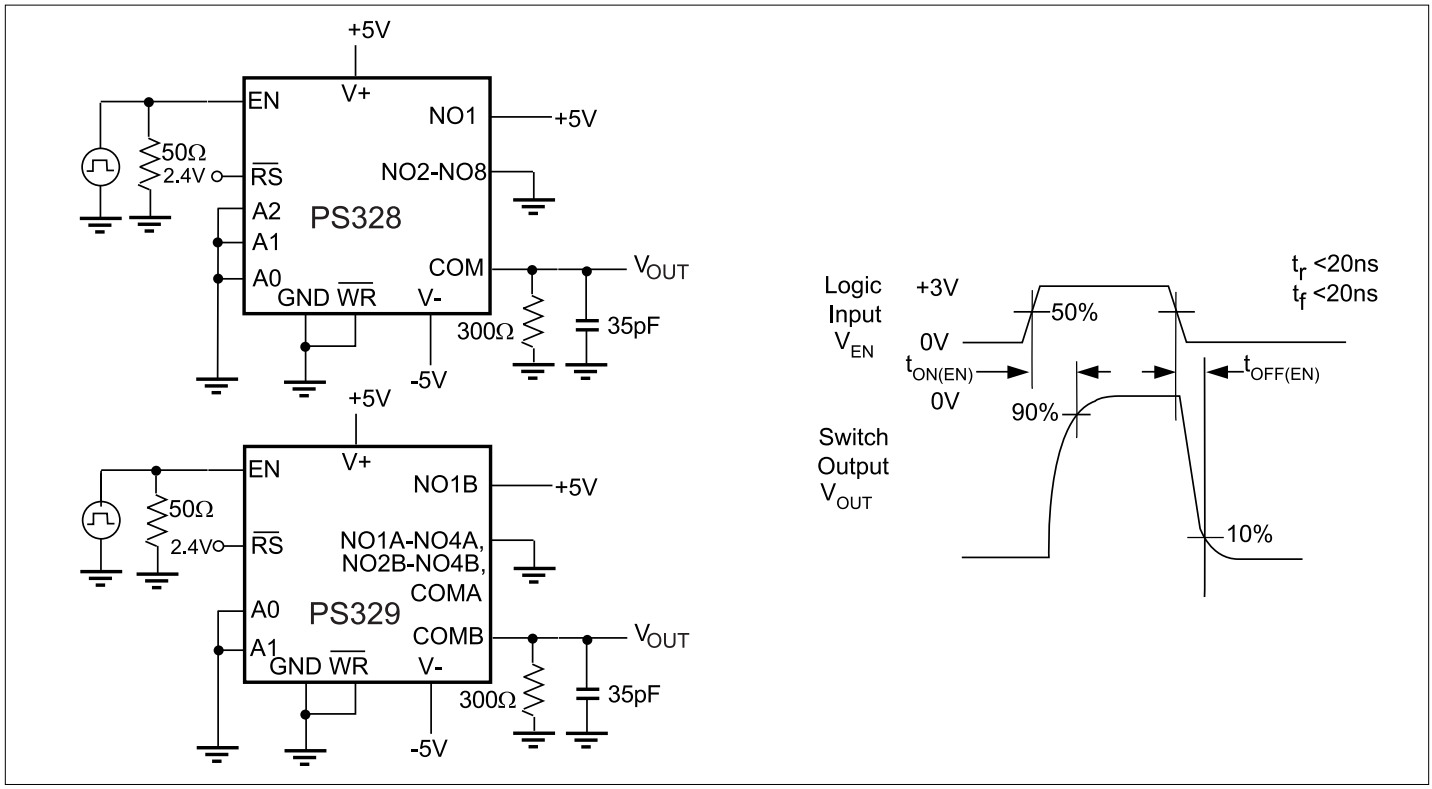

Figure 2. Enable Switching Time

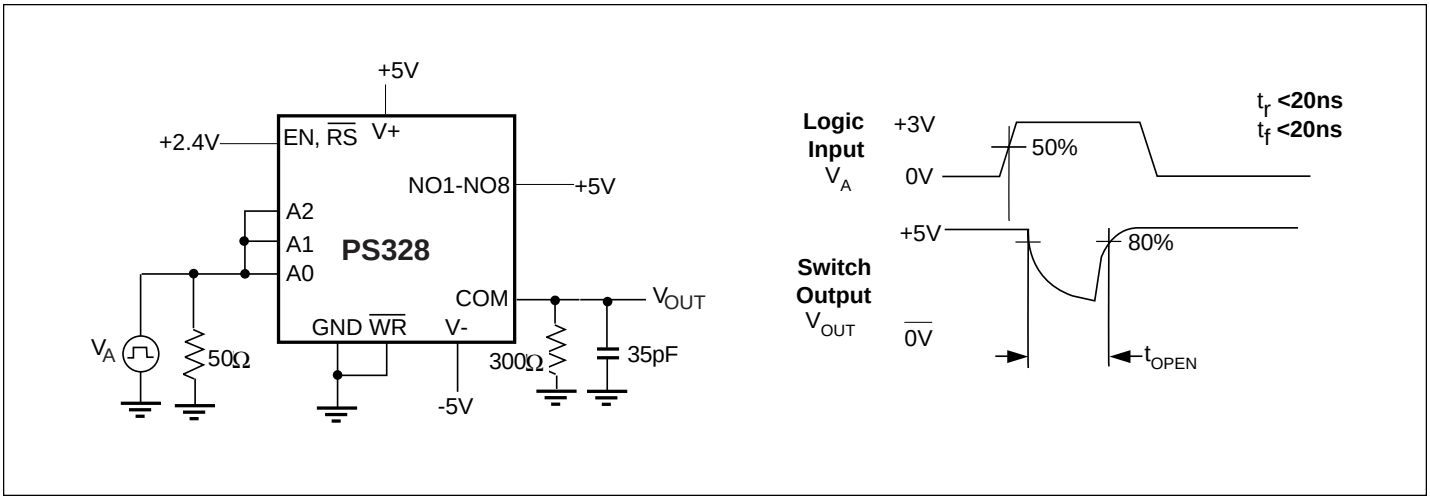

Figure 3. Break-Before-Make Interval

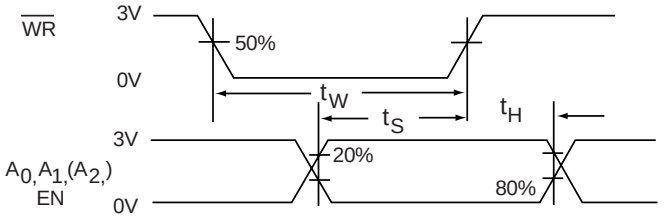

Figure 4. $\overline{WR}$ Timing

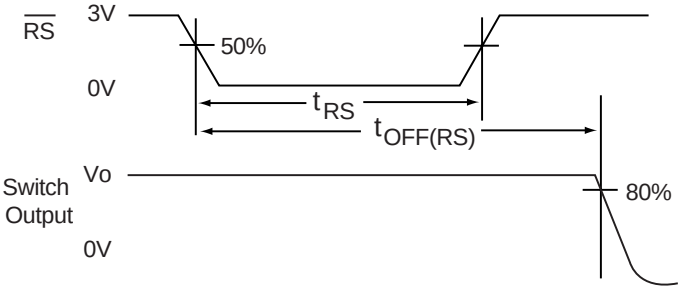

Figure 5. $\overline{RS}$ Timing

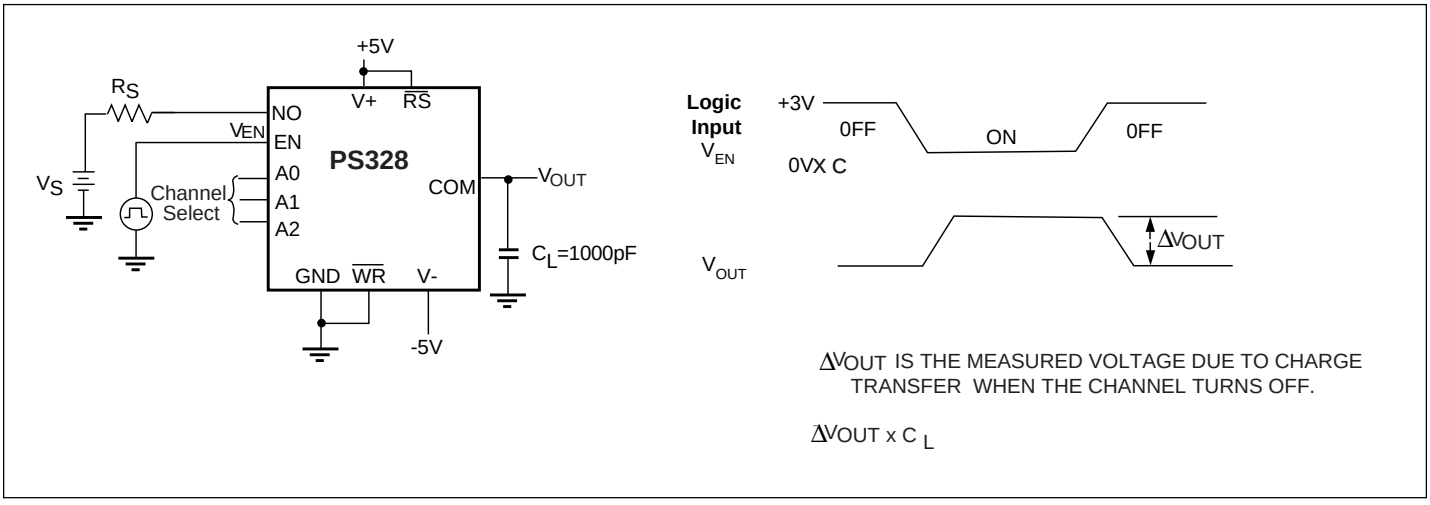

Figure 6. Charge Injection

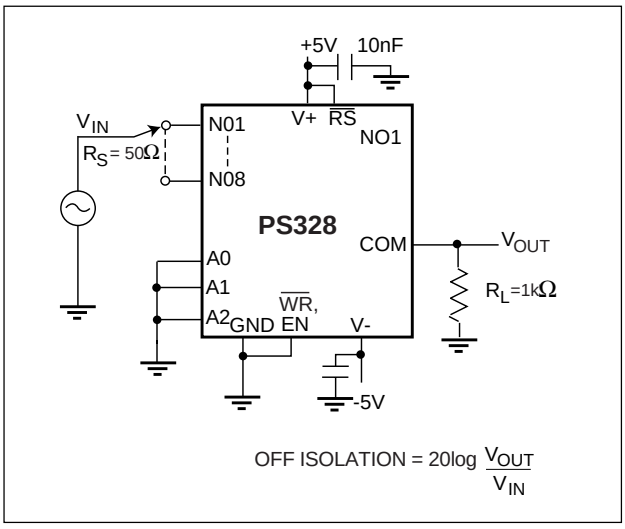

Figure 7. Off Isolation

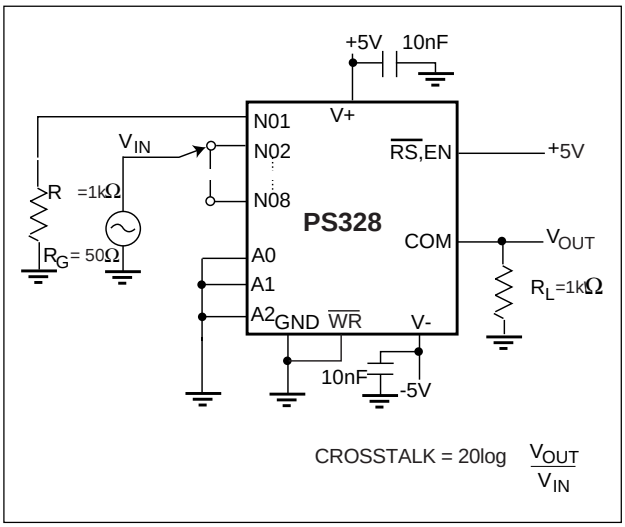

Figure 8. CrossTalk

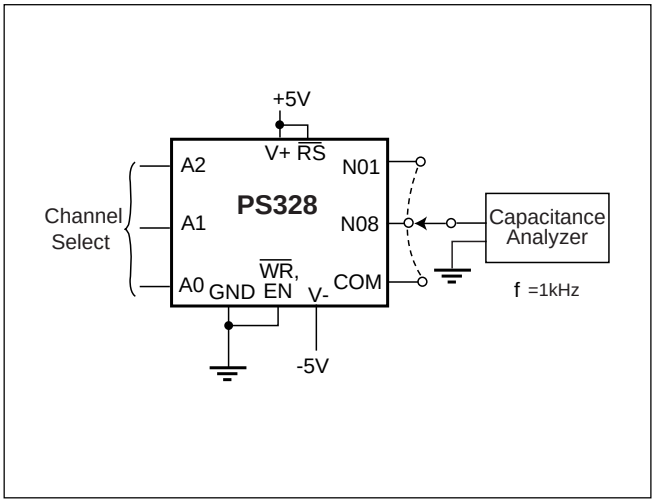

Figure 9. NO/COM Capacitance