PM4575J

Silicon N-Channel Power MOS FET Module

HITACHI

November 1996

Application

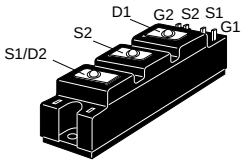
High Speed Power Switching

Features

- Equipped with Power MOS FET
- Low on-resistance
- High speed switching
- Low drive current
- Wide area of safe operation
- Inherent parallel diode between source and drain
- Isolated base from Terminal
- Suitable for motor driver, switching regulator and etc.

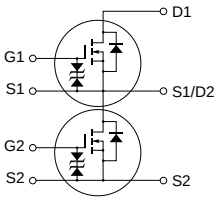
Outline

LF-J



No	Electrode	Terminals	Remarks
S1	Source 1	M5 screw	Power terminal
D1	Drain 1	M5 screw	
S2	Source 2	M5 screw	
D2	Drain 2	M5 screw	
G1	Gate 1	#110	Signal terminals
S1	Source 1	#110	
G2	Gate 2	#110	
S2	Source 2	#110	

Equivalent Circuit



Absolute Maximum Ratings (Ta = 25°C) (Per FET chip)

Item	Symbol	Rating	Unit
Drain source voltage	$V_{(BR)DSS}$	450	V
Gate source voltage	$V_{(BR)GSS}$	±30	V
Drain current	I_D	75	A
Drain peak current	$I_{D(peak)}$	180	A
Body to drain diode reverse drain current	I_{DR}	75	A
Body to drain diode reverse peak current	$I_{DR(peak)}$	180	A
Channel dissipation	Pch*[1]	300	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–45 to +125	°C
Insulation dielectric	Viso*[2]	2000	Vrms

Notes 1. Value at Ta = 25°C
2. Base to terminals AC minute

Electrical Characteristics (Ta = 25°C) (Per FET chip)

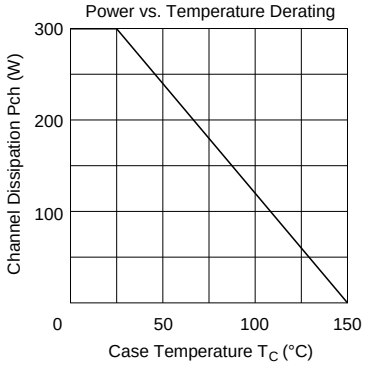
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	450	—	—	V	I_D = 10 mA, V_{GS} = 0 V
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ± 25 V, V_{DS} = 0 V
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	I_G = ±100 µA, V_{DS} = 0 V
Drain leak current	I_{DSS}	—	—	500	µA	V_{DS} = 360 V, V_{GS} = 0 V
Gate to source threshold voltage	$V_{GS(th)}$	2.0	—	3.0	V	I_D = 1 mA, V_{DS} = 10 V
Drain to source saturation voltage	$V_{DS(on)}$	—	3.7	4.44	V	I_D = 37 A, V_{GS} = 10 V*[1]
Static drain to source on state resistance	$R_{DS(on)}$	—	0.10	0.12	Ω	I_D = 37 A, V_{GS} = 10 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	—	45	—	S	I_D = 37 A, V_{DS} = 10 V*[1]
Input capacitance	Ciss	—	9600	—	pF	V_{DS} = 10 V, V_{GS} = 0 V f = 1 MHz
Output capacitance	Coss	—	2300	—		
Reverse transfer capacitance	Crss	—	330	—		
Turn-on delay time	$t_{d(on)}$	—	100	—	ns	I_D = 37 A, V_{GS} = 10 V Rg = 50 Ω R_L = 1 Ω
Rise time	t_r	—	310	—		
Turn-off delay time	$t_{d(off)}$	—	550	—		
Fall time	t_f	—	135	—		
Body to drain diode forward voltage	V_{DF}	—	1.8	—	V	I_F = 75 A, V_{GS} = 0 V
Body to drain diode reverse recovery time	t_{rr}	—	130	—	ns	I_F = 75 A, V_{GS} = 0 V di/dt = 100 A/ms

Note 1. Pulse Test

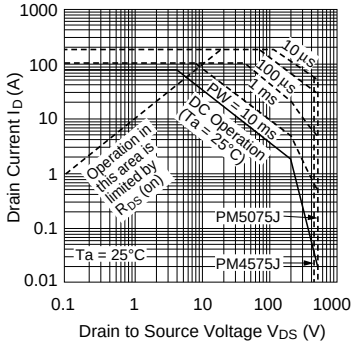
Mechanical Characteristics

Item	Symbol	Condition	Rating	Unit
Fixing strength	—	Mounting into main-terminal with M4 screw	1.45 to 1.95	N-m
	—	Mounting into heat sink with M5 screw	1.95 to 2.9	N-m
Weight	—	Typical value	200	g

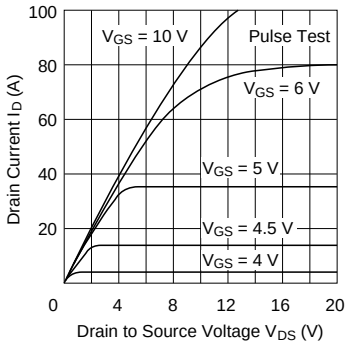
Power vs. Temperature Derating



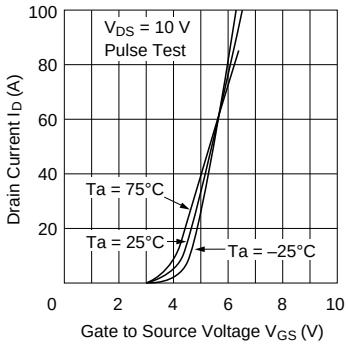
Maximum Safe Operation Area



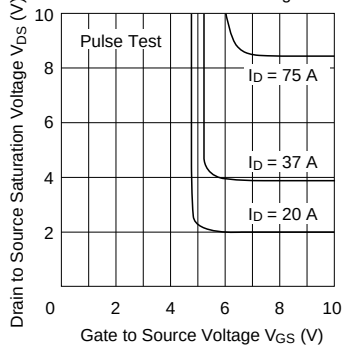
Typical Output Characteristics



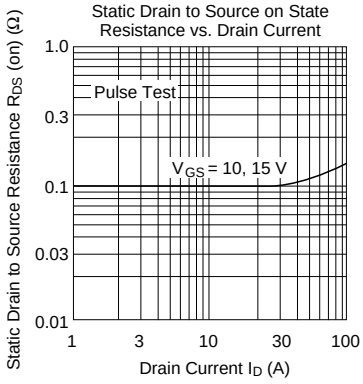
Typical Transfer Characteristics



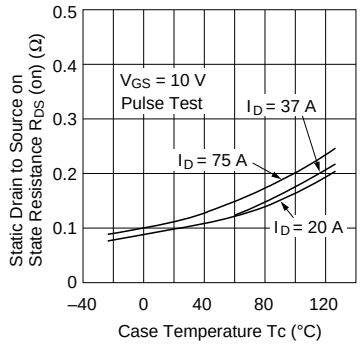
Drain to Source Saturation Voltage vs. Gate to Source Voltage



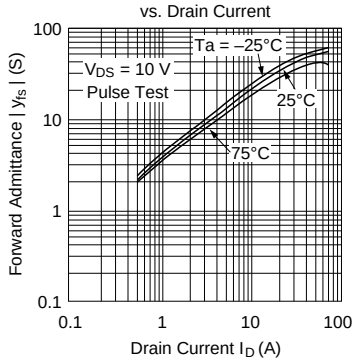
Static Drain to Source on State Resistance vs. Drain Current



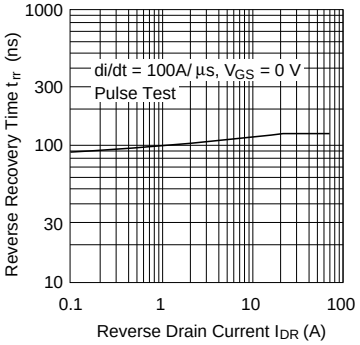
Static Drain to Source on State Resistance vs. Temperature



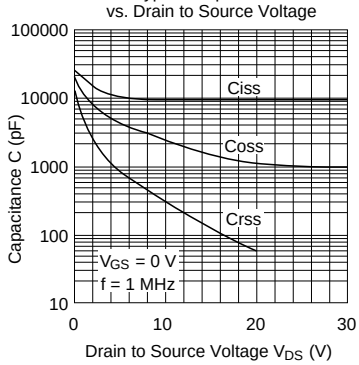
Forward Transfer Admittance vs. Drain Current



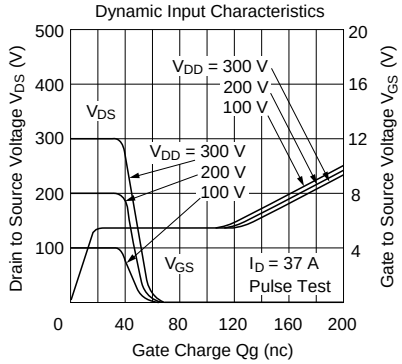
Body to Drain Diode Reverse Recovery Time



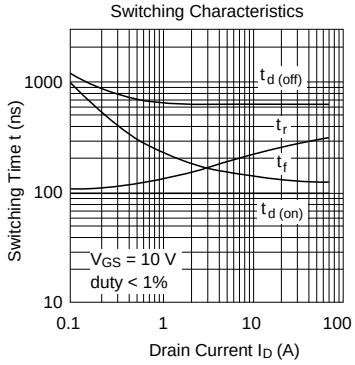
Typical Capacitance
vs. Drain to Source Voltage



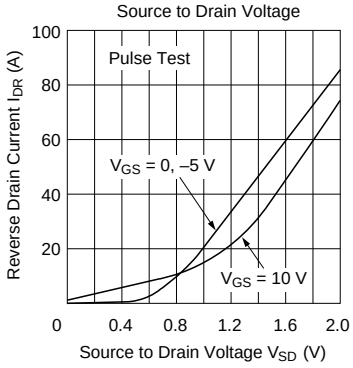
Dynamic Input Characteristics



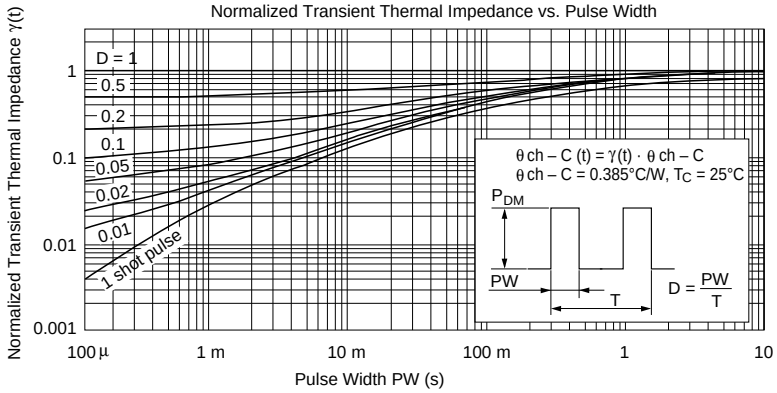
Switching Characteristics



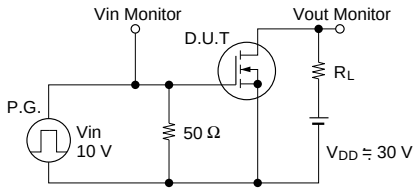
Reverse Drain Current vs.
Source to Drain Voltage



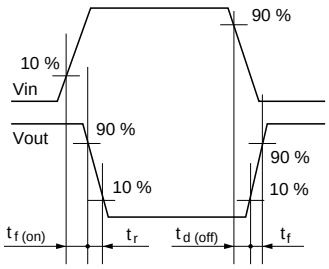
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

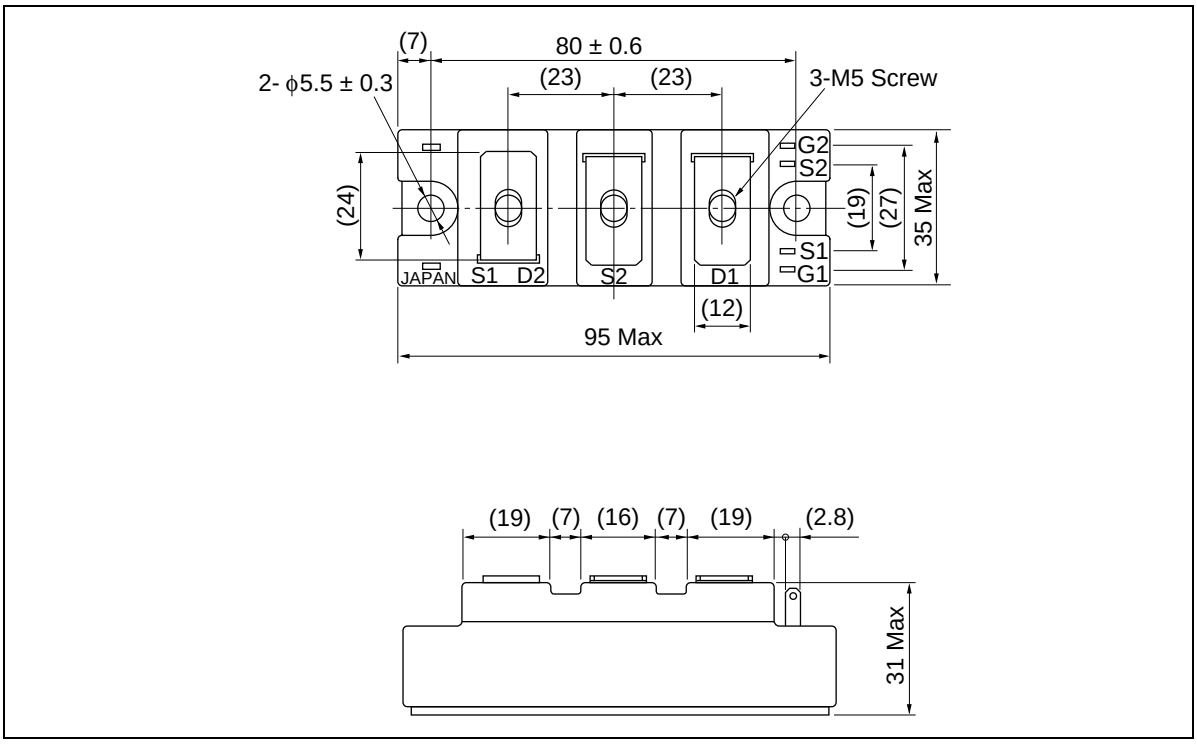


Waveforms



Package Dimensions

Unit: mm



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