BURR-BROWN®

PGA102

High Speed PROGRAMMABLE GAIN AMPLIFIER

FEATURES

- **DIGITALLY PROGRAMMABLE GAIN: G = 1, 10, 100**
- **LOW GAIN ERROR: 0.025% max**
- **FAST SETTLING: 2.8μs to 0.01%**
- **16-PIN PLASTIC AND CERAMIC DIP**

APPLICATIONS

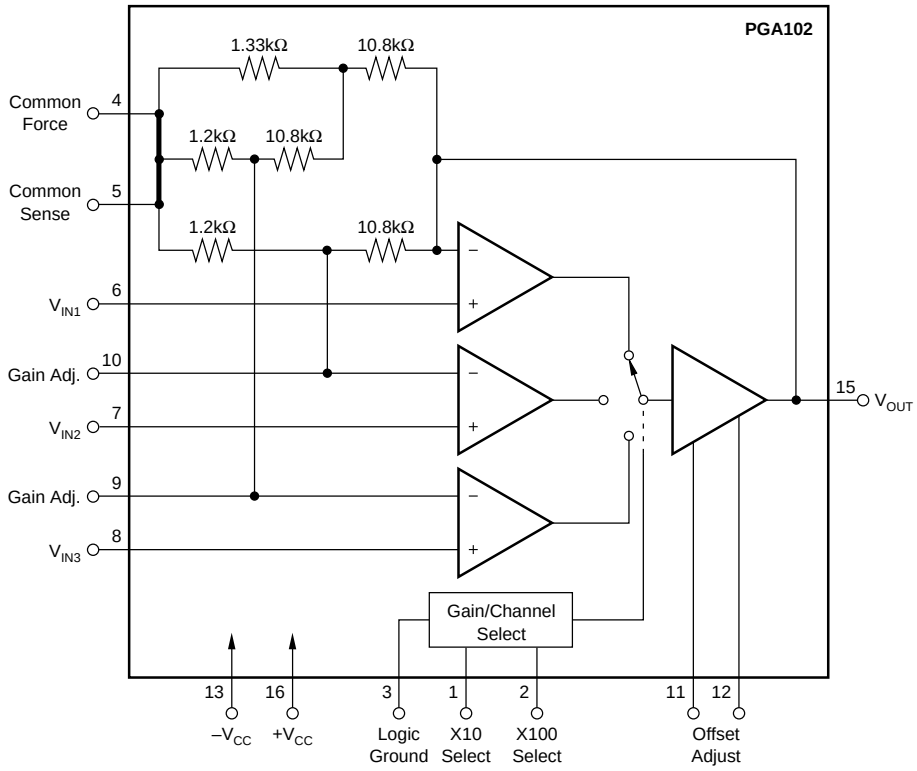
- **DATA ACQUISITION AMPLIFIER**
- **FIXED-GAIN AMPLIFIER**
- **AUTOMATIC GAIN SCALING**

DESCRIPTION

The PGA102 is a high speed, digitally programmable-gain amplifier. CMOS/TTL-compatible inputs select gains of 1, 10 or 100V/V. Each gain has an independent input terminal, providing an input multiplexer function.

On-chip metal film gain-set resistors are laser-trimmed to provide excellent gain accuracy. High speed input circuitry allows multiplexing of high speed signals.

The PGA102 is available in 16-pin plastic and ceramic DIP packages. Commercial, industrial and military temperature range models are available.



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SPECIFICATIONS

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC unless otherwise specified.

PARAMETER	CONDITIONS	PGA102AG			PGA102BG, SG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN											
Inaccuracy[1]	R_L = 2kΩ, G = 1		±0.007	±0.02		±0.003	±0.01		*	*	%
	G = 10		±0.015	±0.03		±0.01	±0.02		*	±0.05	%
	G = 100		±0.02	±0.05		±0.015	±0.025		*	±0.06	%
vs Temperature	G = 1		±0.4	±5		*	*		*	*	ppm/°C
	G = 10		±2	±7		*	*		*	*	ppm/°C
	G = 100		±7	±20		*	*		±9	*	ppm/°C
Nonlinearity	R_L = 2kΩ, G = 1		0.001	0.003		*	*		*	*	% of FS
	G = 10		0.002	0.005		*	*		*	*	% of FS
	G = 100		0.003	0.01		*	*		*	*	% of FS
RATED OUTPUT											
Voltage	R_L = 2kΩ	±10	±12.5		*	*		*	*		V
Current	V_{OUT} = 10V	±5	±10		*	*		*	*		mA
Short Circuit Current		±10	±25		*	*		*	*		mA
Output Resistance			0.01			*			*		Ω
Load Capacitance	For Stable Operation		2000			*			*		pF
INPUT OFFSET VOLTAGE											
Initial[2]	G = 1		±200	±500		±100	±250		*	±1500	µV
	G = 10		±70	±200		±50	±100		*	±600	µV
	G = 100		±70	±200		±50	±100		*	±600	µV
vs Temperature	G = 1		±5	±20		*	*		±7	±50	µV/°C
	G = 10		±1	±7		*	*		±3	±10	µV/°C
	G = 100		±0.5	±3		*	*		±2	±7	µV/°C
vs Supply Voltage	±5 < V_{CC} < ±18V										
	G = 1		±30	±70		*	*		*	*	µV/V
	G = 10		±8	±30		*	*		*	*	µV/V
	G = 100		±8	±30		*	*		*	*	µV/V
INPUT BIAS CURRENT											
Initial	T_A = +25°C		±20	±50		*	*		*	*	nA
Over Temperature	$T_{A\ MIN}$ to $T_{A\ MAX}$		±25	±60		*	*		*	*	nA
ANALOG INPUT CHARACTERISTICS											
Voltage Range	Linear Operation	±10	±12		*	*		*	*		V
Resistance			7×10^8			*			*		Ω
Capacitance			4			*			*		pF
INPUT NOISE											
Voltage Noise	f_B = 0.1Hz to 10Hz										
	G = 1		4.5			*			*		µVp-p
	G = 10		1.5			*			*		µVp-p
	G = 100		0.6			*			*		µVp-p
Voltage Noise Density	f_O = 1Hz, G = 1		490			*			*		nV/√Hz
	G = 10		178			*			*		nV/√Hz
	G = 100		83			*			*		nV/√Hz
	f_O = 10Hz, G = 1		155			*			*		nV/√Hz
	G = 10		56			*			*		nV/√Hz
	G = 100		20			*			*		nV/√Hz
	f_O = 100Hz, G = 1		93			*			*		nV/√Hz
	G = 100		31			*			*		nV/√Hz
	G = 100		18			*			*		nV/√Hz
	f_O = 1kHz, G = 1		79			*			*		nV/√Hz
	G = 10		31			*			*		nV/√Hz
	G = 100		18			*			*		nV/√Hz
Current Noise	f_B = 0.1Hz to 10Hz		76			*			*		pAp-p
Current Noise Density	f_O = 1Hz		8.8			*			*		pA/√Hz
	f_O = 10Hz		2.8			*			*		pA/√Hz
	f_O = 100Hz		0.99			*			*		pA/√Hz
	f_O = 1kHz		0.43			*			*		pA/√Hz
DYNAMIC RESPONSE											
±3dB Bandwidth	Small Signal, G = 1		1500			*			*		kHz
	G = 10		750			*			*		kHz
	G = 100		250			*			*		kHz
Full Power Bandwidth	V_{OUT} = ±10V, R_L = 2kΩ		160			*			*		kHz
Slew Rate	V_{OUT} = ±10V Step, R_L = 2kΩ	6	9		*	*		*	*		V/µs

SPECIFICATIONS (CONT)

ELECTRICAL

At +25°C, $\pm V_{CC}$ = 15VDC unless otherwise specified.

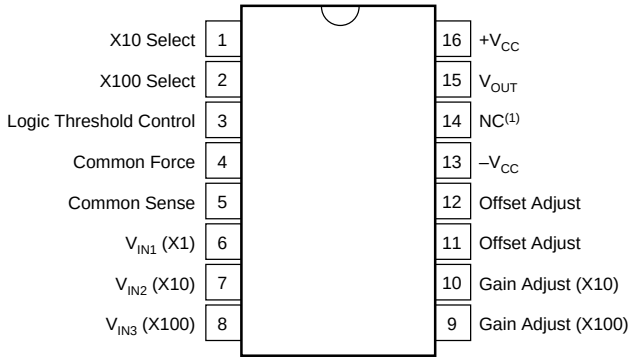
PARAMETER	CONDITIONS	PGA102AG			PGA102BG			PGA102KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DYNAMIC RESPONSE (CONT)											
Settling Time (0.1%)	V_{OUT} = 10V Step, G = 1		1.6			*			*		µs
	G = 10		2.2			*			*		µs
	G = 100		5.2			*			*		µs
Settling Time (0.01%)	V_{OUT} = 10V Step, G = 1		2.8			*			*		µs
	G = 10		2.8			*			*		µs
	G = 100		8.2			*			*		µs
Overload Recovery Time, 0.1%	50% Overdrive, G = 1 (see Performance Curve)		2.5			*			*		µs
CROSSTALK											
DC	±10V to Both Off Channels		–155			*			*		dB
60Hz	±10V to Both Off Channels		–144			*			*		dB
DIGITAL INPUT CHARACTERISTICS											
Input "Low" Threshold	V_{IL}[3] on Pin 1 or 2			VLTC+0.8			*			*	V
Input "Low" Current				1			*			*	µA
Input "High" Threshold	V_{IH}[3] on Pin 1 or 2	VLTC+2		1	*		*	*		*	V
Input "High" Current			0.1	1		*	*		*	*	µA
Logic Threshold Control	VLTC on Pin 3	$-V_{CC}$		V_{CC} – 4	*		*	*		*	V
Switching Time[4]	Between Channels		1			*			*		µs
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range		±5		±18	*		*	*		*	VDC
Quiescent Current	V_{OUT} = 0V		±2.4	±3.3		*	*		*	*	mA
	No External Load, V_{OUT} = ±10V			±5.3			*			*	mA
TEMPERATURE RANGE											
Specification, KP Grade	$T_{A\ MIN}$ to $T_{A\ MAX}$							0		+70	°C
AG and BG Grades		–25		+85	*		*				°C
SG Grade					–55		+125				°C
Operating		–55		+125	*		*	–25		+85	°C
Storage		–65		+150	*		*	–55		+125	°C
Thermal Resistance	θ_{JA}		100			*			*		°C/W

* Specification same as AG grade.

NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately ±0.3µV/°C for each 100µV of offset adjusted. (3) Voltage on the logic threshold control pin, VLTC, adjusts the threshold for "Low" and "High" logic levels. (4) Total time to settle equals switching time plus settling time of the newly selected gain.

PIN CONFIGURATION

Top View **DIP**



NOTE: (1) No Internal Connection.

ABSOLUTE MAXIMUM RATINGS

Power Supply ..... ±18V
Input Voltage Range: Analog ..... $\pm V_{CC}$
Digital ..... $(V_{PIN\ 3} - 5.6V)$ to $+V_{CC}$
Storage Temperature Range: G Package ..... –65°C to +150°C
P Package ..... –55°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C
Output Short Circuit Duration ..... Continuous to Common
Junction Temperature: G Package ..... +175°C
P Package ..... +110°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
PGA102AG	16-Pin Hermetic DIP	–25°C to +85°C
PGA102BG	16-Pin Hermetic DIP	–25°C to +85°C
PGA102SG	16-Pin Hermetic DIP	–55°C to +125°C
PGA102KP	16-Pin Plastic DIP	0°C to +70°C

PACKAGE INFORMATION

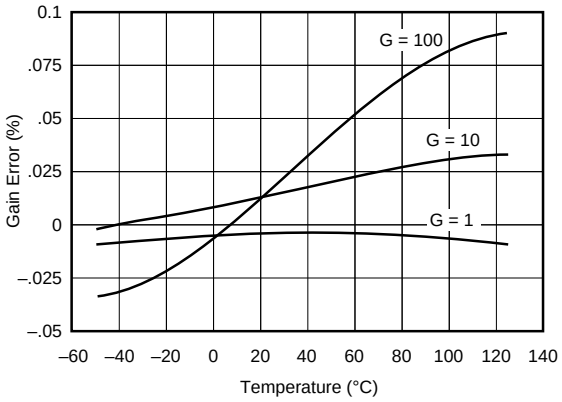
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PGA102AG	16-Pin Hermetic DIP	109
PGA102BG	16-Pin Hermetic DIP	109
PGA102SG	16-Pin Hermetic DIP	109
PGA102KP	16-Pin Plastic DIP	180

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

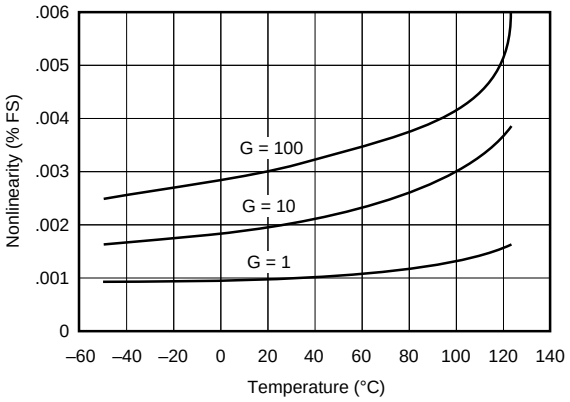
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted.

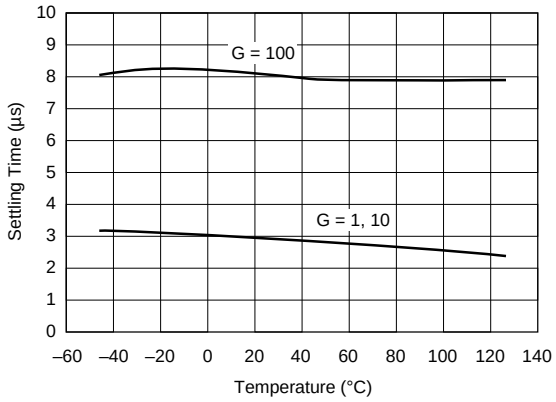
GAIN ERROR vs TEMPERATURE



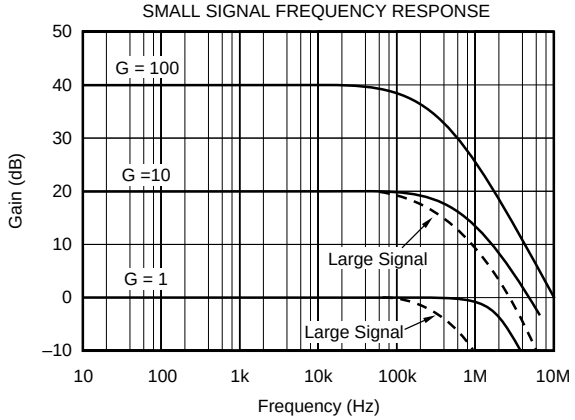
NONLINEARITY vs TEMPERATURE



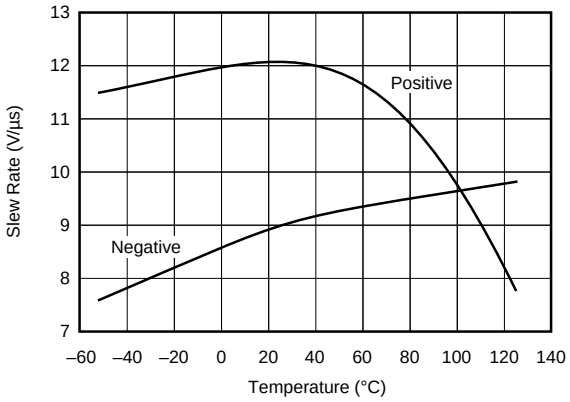
SETTLING TIME vs TEMPERATURE



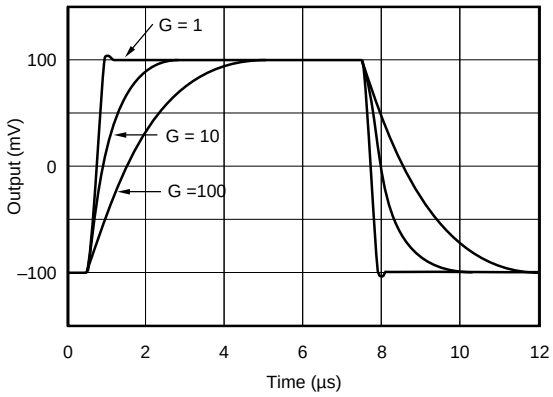
SMALL SIGNAL FREQUENCY RESPONSE



SLEW RATE vs TEMPERATURE



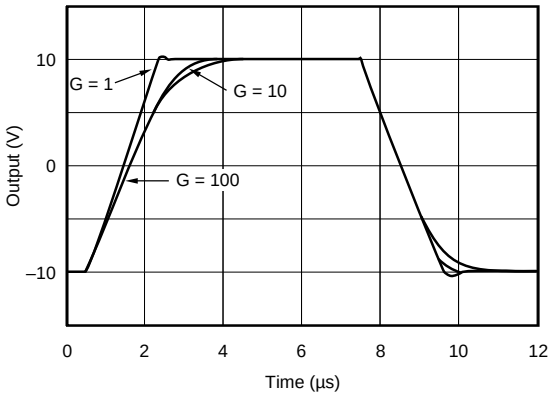
SMALL SIGNAL STEP RESPONSE



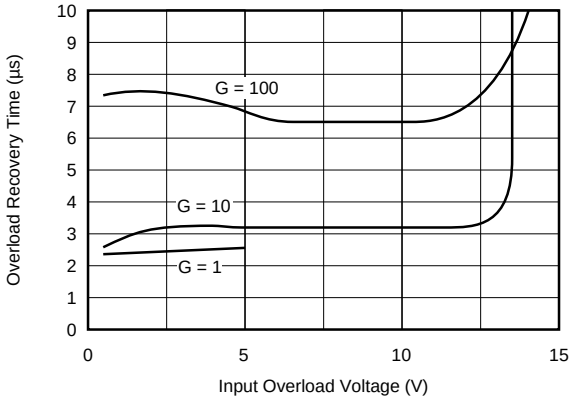
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted.

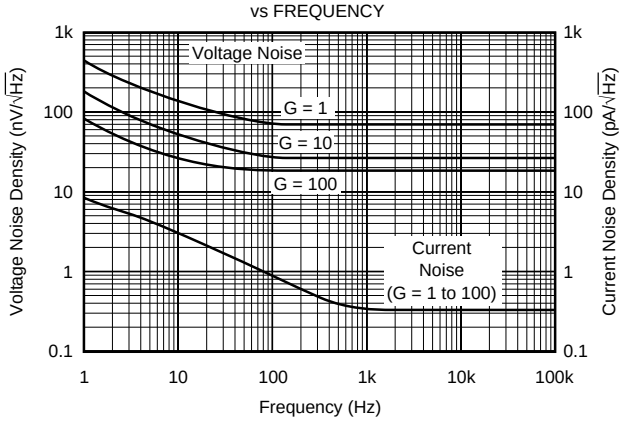
LARGE SIGNAL STEP RESPONSE



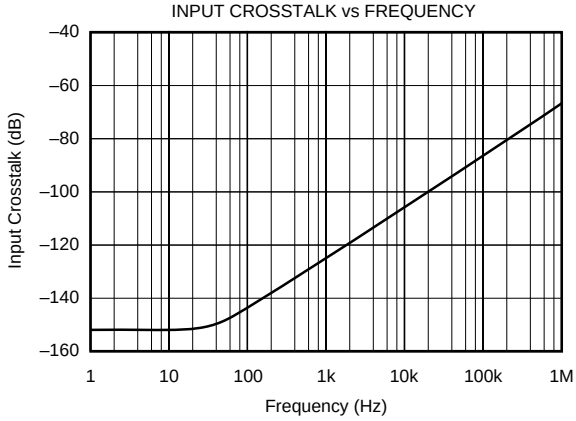
OVERLOAD RECOVERY vs INPUT OVERLOAD



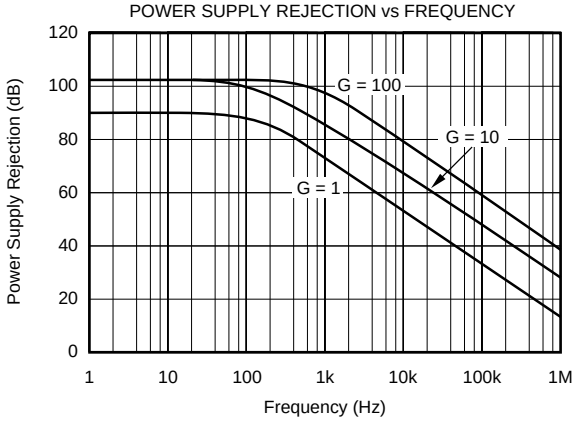
INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY



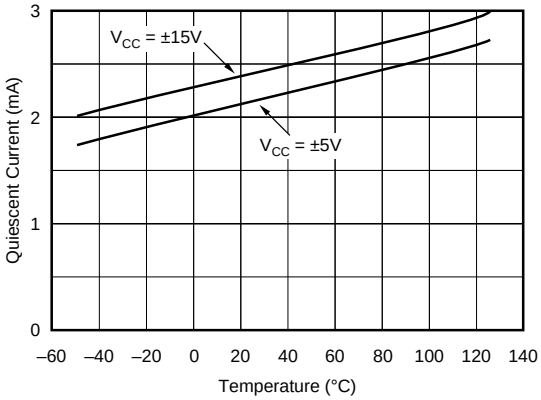
INPUT CROSSTALK vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



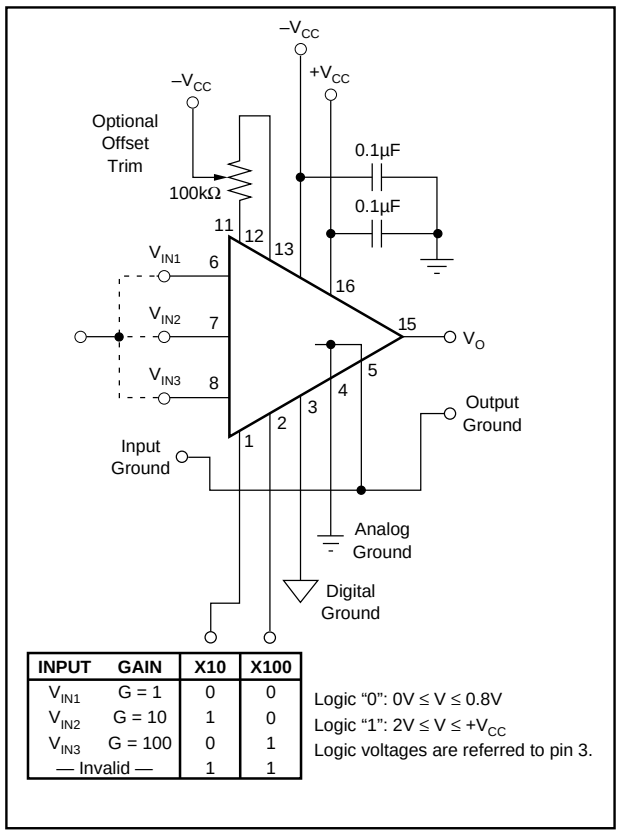
QUIESCENT CURRENT vs TEMPERATURE



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA102. Power supplies should be bypassed with 0.1µF capacitors located close to the device pins.

The inputs for each gain are independent and can be connected to three separate signal sources. Or, for many applications, the three inputs are connected in parallel to form a single input—see Figure 1. Only the input corresponding to the selected gain is active, operating as a non-inverting amplifier. The two inactive inputs behave as open circuits. The input bias current of the inactive inputs is negligible compared to that of the selected input.



INPUT	GAIN	X10	X100
V_{IN1}	G = 1	0	0
V_{IN2}	G = 10	1	0
V_{IN3}	G = 100	0	1
— Invalid —		1	1

Logic “0”: 0V ≤ V ≤ 0.8V
Logic “1”: 2V ≤ V ≤ +V_{CC}
Logic voltages are referred to pin 3.

FIGURE 1. Basic Circuit Connections.

DIGITAL INPUTS

Gain is selected by the digital input pins, "X10" and “X100”. The threshold of these logic inputs is approximately 1.3V above the voltage on pin 3. For CMOS or TTL logic signals, connect pin 3 to logic ground. The logic inputs are not latched. Any change logic inputs immediately selects a new gain. Switching time is approximately 1µs. This does not include the time required for the analog output to settle to a new output value (see settling time specifications).

Note that the two logic inputs allow four possible logic states—see Figure 1 for the logic table. A logic “1” on both inputs is an invalid code. This will not damage the device, but the analog output voltage will not be predictable while this code is applied.

OFFSET ADJUSTMENT

The offset voltage of each of the three input stages is laser-trimmed. Many applications require no further adjustment. The optional trim circuit shown in Figure 1 can be used to adjust the offset voltage. This adjustment affects the offset of all three gain channels. Since each gain setting may require a different adjustment of the potentiometer, this requires a compromise. Often, offset voltage of the G = 100 channel is the most important, so adjustment can be optimized for this channel only. Alternatively, Figure 2 shows a CMOS switch used to select independent offset adjustment potentiometers for each of the three channels.

Use these offset adjustment techniques only to null the offset voltage of the PGA102. Do not null offset produced by the signal source or other system offsets or this will increase the temperature drift of the PGA102.

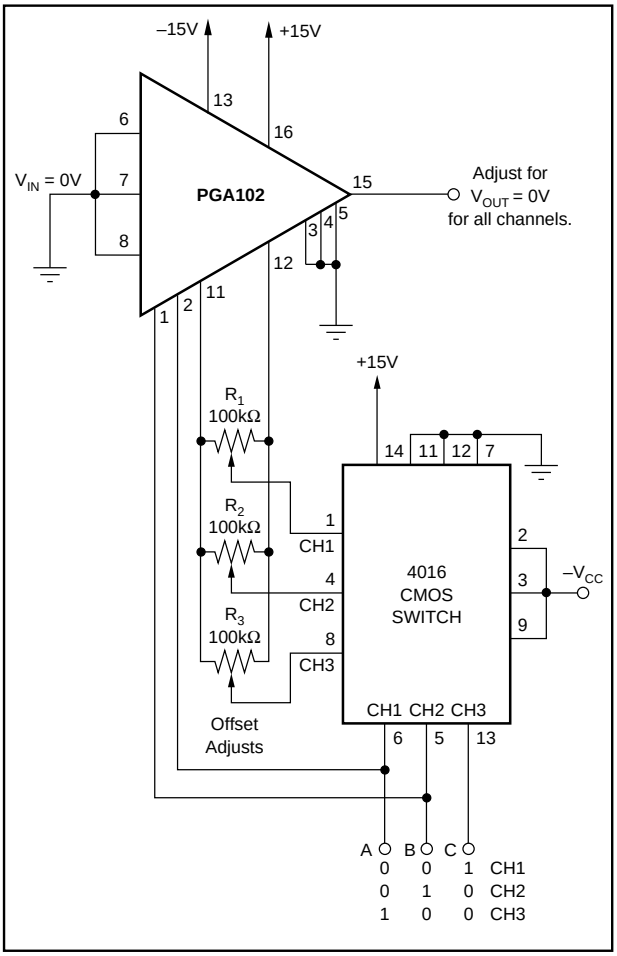


FIGURE 2. Independent Offset Adjustment of Channels 1, 2, and 3.

GAIN ADJUSTMENT

Gain of the PGA102 is accurately laser trimmed and usually requires no further adjustment. The optional circuit in Figure 3 allows independent gain adjustment of the G = 10 and G = 100 inputs.

The gain of the G = 10 and G = 100 inputs can be changed by adding external resistors to the internal feedback network as shown in Figures 4 and 5. The internal gain-set resistors are trimmed for precise ratios, not to exact values. The internal resistor values are within approximately ±30% of the nominal values shown on the front page diagram. This makes the external resistor values in Figures 4 and 5 subject to variation—especially for gains differing greatly from the initial value.

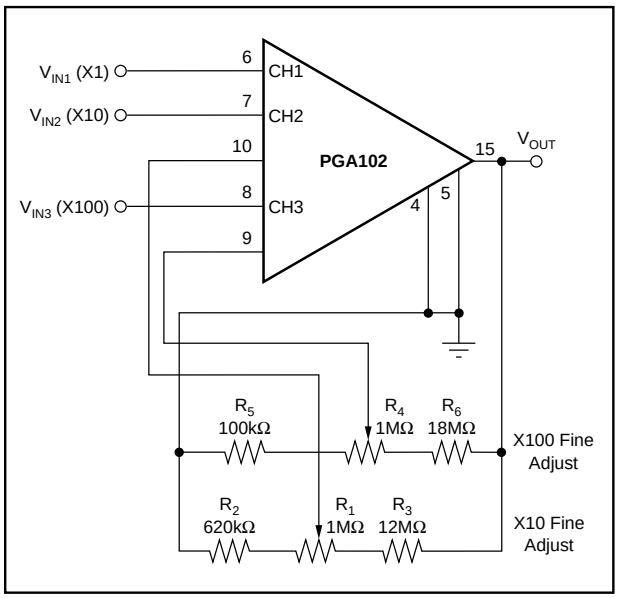


FIGURE 3. Optional Fine Gain Adjustment.

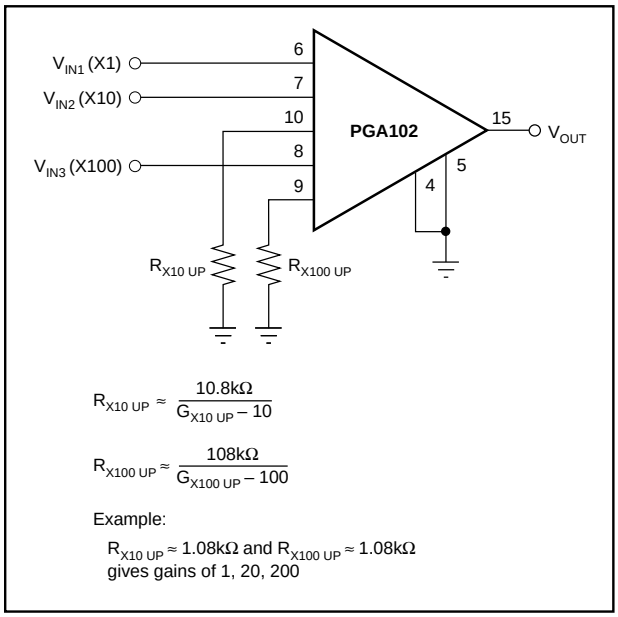


FIGURE 4. Connections for Higher Gains.

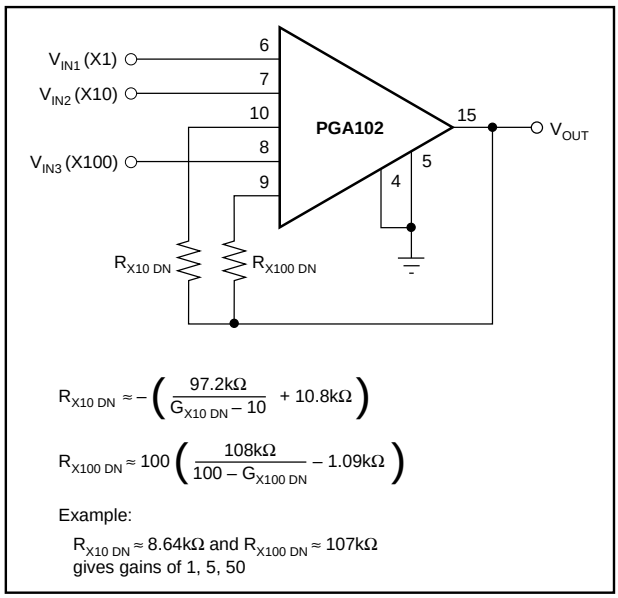


FIGURE 5. Connections for Lower Gains.

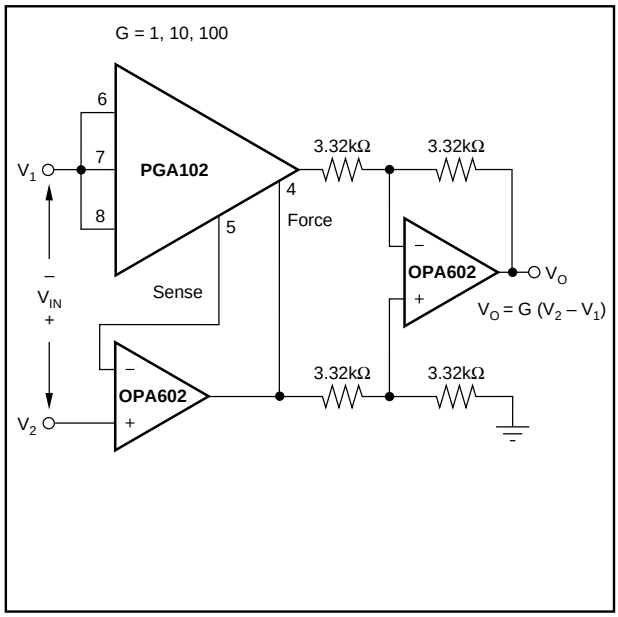


FIGURE 6. High-Speed Instrumentation Amplifier.

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