Product Brief
April 2001

PayloadPlus® Voice Packet Processor

Introduction

The Voice Packet Processor (VPP) is part of the Agere Systems PayloadPlus family of network processors. The VPP is designed to fit on the data path between the Fast Pattern Processor (FPP) and the Routing Switch Processor (RSP) to handle ATM Adaption Layer 2 (AAL2) traffic.

Key features of the VPP include:

- Parsing AAL2 cells to CPS packets. At OC-12, supports a total of 32,767 unique conversations
- Assembly of AAL2 cells from CPS packets. At OC-12, supports a total of 32,767 unique conversations
- Carrying up to 16,383 conversations on AAL2 VCs.
- Supporting up to 248 active voice channels per VC.
- CPS packet switching between VCs.
- Bypassing other traffic with remaining bandwidth available for IP/AAL5, up to OC-12.

Description

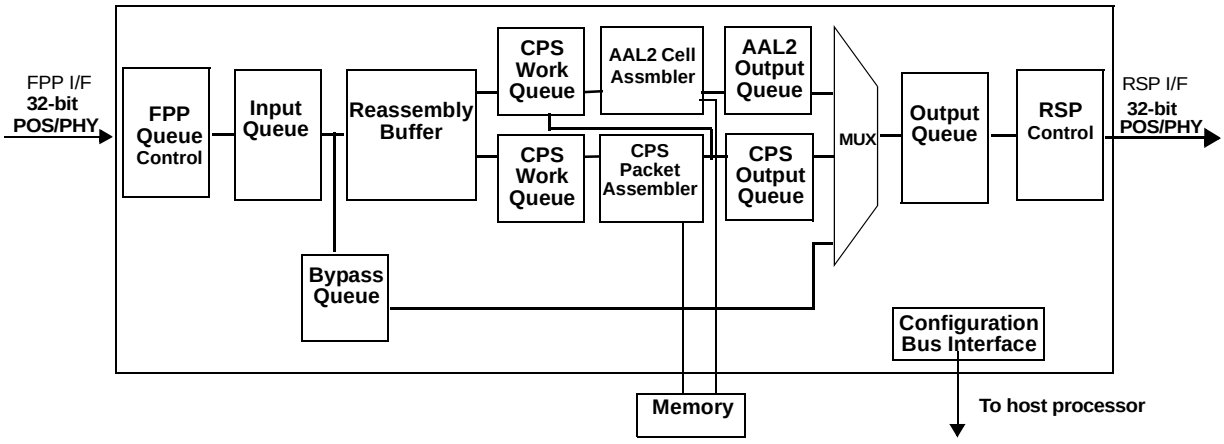
The VPP architecture is designed to generate and terminate AAL2 traffic.

The VPP accepts AAL2 cells, CPS packets, and other PDUs from the FPP. It processes the AAL2 cells and CPS packets, and passes the other PDUs to the RSP transparently.

The VPP parses AAL2 cells into CPS packets, and assembles CPS packets into AAL2 cells. It also keeps global, virtual connection, and channel statistics. See the block diagram below.

Applications

The VPP supports voice applications that use AAL2 cells, such as voice over ATM (VoATM).



VPP Block Diagram

The VPP can process VoATM concurrently with the FPP and RSP processing voice over IP (VoIP).

Feature Set

- Handles up to 32,767 active conversations in each direction on up to 16,383 different active VCs in each direction (with the exception of CPS packet switching)
- Handles total of OC-40 under the following restrictions:
  - —OC-12 of AAL2 cells
  - —OC-12 of CPS packets
  - —No more than OC-40 of bypassed traffic
- Parses AAL2 cells into constituent CPS packets
  - —Parses multiple CPS packets per AAL2 cell
  - —Parses CPS packets straddling two or three AAL2 cells
  - —Provides CPS packets with unique user-provisioned destination IDs to the RSP
  - —Performs error checking at the cell and packet level
  - —Keeps statistics at the VC and individual conversation level
  - —Performs timeout function on partially completed CPS packets
- Assembles CPS packets into AAL2 cells
  - —Assembles multiple CPS packets per AAL2 cell
  - — Assembles CPS packets straddling AAL2 cells
  - —Provides AAL2 cells with unique user-provisioned distination IDs to the RSP
  - —Performs error checking at the cell and packet level
  - —Keeps statistics at the VC and individual conversation level
  - —Performs timeout functions on partially assembled AAL2 cells
- Allows for non-AAL2/CPS data to be bypassed through the VPP
- Handles type 3 management packets in both directions
  - —In the AAL2-to-CPS direction, handles type 3 management packets in either active conversations or inactive conversations on active VCs
  - —In the CPS-to-AAL2 direction, handles type 3 management packets on active conversations
- Performs CPS packet switching (CPS packets from one AAL2 cell stream moved to different AAL2 cell streams)
  - —Supports CID modification along with modified CPS HEC
  - —Half-speed operation

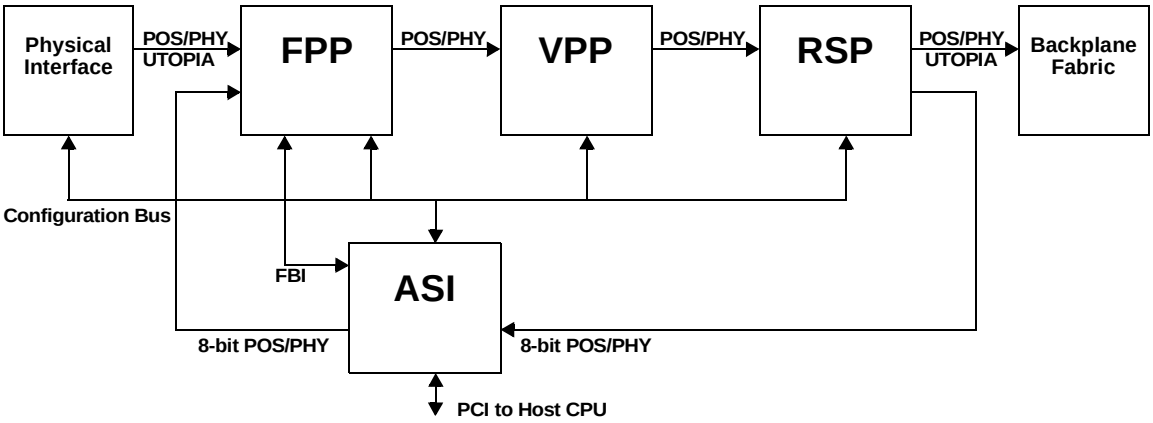
Up to 16,383 conversations can be switched on up to 8,191 VCs in each direction

Typical System Configuration

The VPP supports the following interfaces:

- 32-bit multiPHY POS-PHY Level 3 interface for input and output of the data path.
- 64-bit synchronous SRAM interface for maintaining state and statistics.
- 8-bit asynchronous bus for configuring the VPP from the host processor via the Agere System Interface (ASI) or other logic.

The VPP is connected to the FPP, RSP, and ASI as shown in the following diagram.



VPP System Configuration

Availability

- SDE — available now
- FPGA — 1Q 2001 (alpha engagements)
- ASIC — 2 Q 2001

Additional Information

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