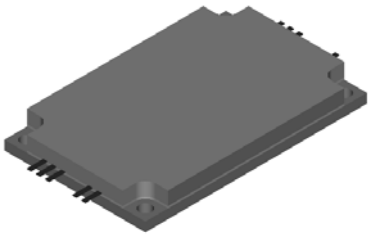


PFM21020WB SPECIFCATION
2080-2200 MHz, 20W, Two-Stage Power Module
Enhancement-Mode Lateral MOSFETs

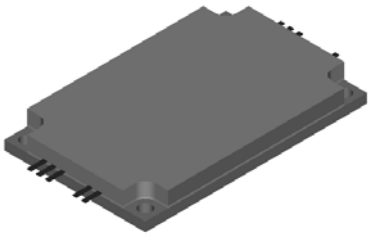
This UMTS module has been designed to serve as a driver amplifier in either the output or the error path of a multi-channel feedforward amplifier. The Si LDMOS transistors are biased for Class AB operation in order to optimize linearity and efficiency. Particular emphasis has been placed on wideband operation with excellent gain flatness and phase linearity over double the normal 2110 to 2170 MHz bandwidth. The PFM21020WB is a fully integrated power amplifier with temperature compensation circuitry and extensive internal power supply bypassing.

The module has a single drain supply lead and two high impedance gate voltage inputs. The two gate supply voltages are nominally +7.5 to +8.0 volts to set optimum quiescent bias current levels. The user may optimize the bias for a particular application by adjusting the gate supply voltages. The drain supply is normally +28 VDC, although the amplifier will operate with drain supply ranging from +25 to +30 VDC.

ELECTRICAL CHARACTERISTICS (Vdd=28Vdc, Tc=25deg C, 50 ohm system, unless otherwise specified)

Characteristic	Symbol	Min	Typ.	Max	Unit	Test Conditions	Comments
Frequency Range	BW	2080	2140	2200	MHz		All specifications apply over 2080-2200 MHz, unless otherwise noted.
Total Quiescent Current	Idq_{opt}		270	350	mA	No RF applied	$Idq_{opt} = Idq1_{opt} + Idq2_{opt}$
Optimum Quiescent Current a) Input Stage b) Output Stage	 $Idq1_{opt}$ $Idq2_{opt}$	 110 110	 130 130	 180 180	 mA mA	 No RF applied.	The optimum level provides best linearity. Optimum quiescent current levels are provided for each unit.
Small Signal Gain 2080 <F< 2200 MHz	Gss	24.0	25.5	28.0	dB	CW	Idq1= $Idq1_{opt}$ Idq2= $Idq2_{opt}$ Used for all measurements.
Gain Flatness versus Frequency	ΔG_f	-0.30	±0.15	+0.30	dB	CW	Gain variation versus frequency.
Gain Variation over –10 to +80 deg C	Gt		-0.031	-0.04	dB/ degC		
Phase Flatness	$\Delta\Phi$		±0.8	±1.0	Deg		Deviation from linear phase. Allows a constant time delay offset in the measurement.
Group Delay	t_D		3.45		nSec		Time delay used for phase linearity measurement. Does not include fixture delay of 0.16 nanosec.

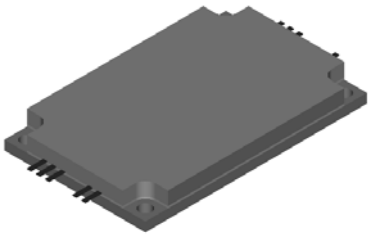
revision date: 02/11/02



PFM2120WB PRELIMINARY SPECIFCATION (Continued)
2.08-2.20 GHz, 20W, Broadband Two-Stage Power Module

Characteristic	Symbol	Min	Typ.	Max	Unit	Test Conditions	Comments
Third-order Inter-modulation Distortion (2-Tone Cont. Random Phase, 1.0 MHz separation)	IM3		-29 -40 -43 -45 -43	-27 -37 -41 -43 -43	dBc dBc dBc dBc dBc	P_{AVG} = 8.9 W (39.5 dBm) P_{AVG} = 4.5 W (36.5 dBm) P_{AVG} = 2.3 W (33.5 dBm) P_{AVG} = 1.1 W (30.5 dBm) P_{AVG} = 0.3 W (24.5 dBm)	$Idq1 = Idq1_{opt}$ $Idq2 = Idq2_{opt}$ 2110, 2140, 2170 MHz
Fifth-order Inter-modulation Distortion (2-Tone Cont. Random Phase, 1.0 MHz separation)	IM5		-33 -43 -48 -51 -51	-30 -40 -45 -48 -48	dBc dBc dBc dBc dBc	P_{AVG} = 8.9 W (39.5 dBm) P_{AVG} = 4.5 W (36.5 dBm) P_{AVG} = 2.3 W (33.5 dBm) P_{AVG} = 1.1 W (30.5 dBm) P_{AVG} = 0.3 W (24.5 dBm)	$Idq1 = Idq1_{opt}$ $Idq2 = Idq2_{opt}$ 2110, 2140, 2170 MHz
W-CDMA (PAR=9.4dB) ACPR (Pout=35 dBm) a) 2.515 MHz Offset b) 3.515 MHz Offset c) 4.0 MHz d) P.A.E.	 ACPR1 ACPR2 ACPR3 P.A.E.		 -62 -67 -52 13.5		 dBc dBc dBc %	 Int BW=30 KHz Int BW=30 KHz Int BW=1 MHz	ACPR is relative to the total in-channel power.
EDGE modulation Error Vector Magnitude	EVM		1.5		%	EDGE signal, Pave= 7 Watts	
EDGE Adjacent Channel Rejection (RMS) a) 400 KHz Offset b) 600 KHz Offset	ACPR		 -62 -72		 dBc dBc	EDGE signal, Pave= 7 Watts	
EDGE Power Added Efficiency			22		%	@ EVM=2.5%	
Power Output @ 1dB compression	P1dB	17.8	20		W	CW	
Efficiency (with one CW signal operated at 1 dB gain compression).		29	33		%	CW	

UltraRF™

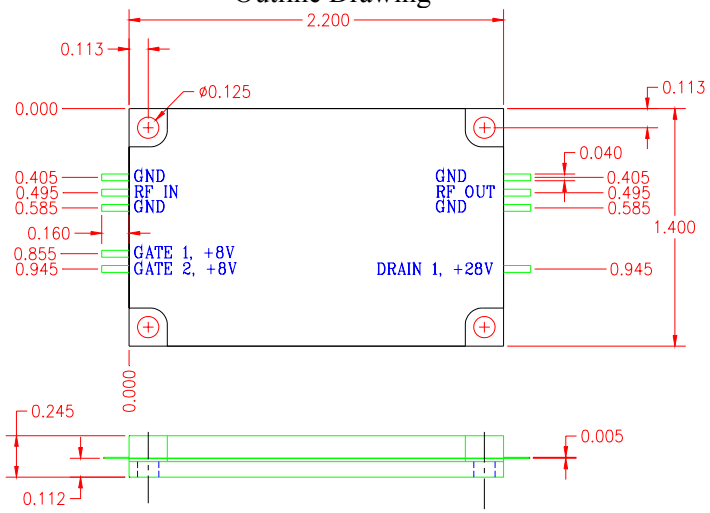


Characteristic	Symbol	Min	Typ.	Max	Unit	Test Conditions	Comments
Input Overdrive Level				+25	dBm	Peak	
Input Return Loss	IRL		-20	-18	dB		Pin ≤ +13 dBm
Output Return Loss	ORL		-20	-18	dB		
Gate Supply Terminal Impedance			20		KOhms		Typical gate supply voltage is +7.5 volts.
Input & output series blocks		The input and output are isolated by a series 24 pF capacitor. Inputs and Outputs are DC isolated from ground.					
Load Mismatch Stress Load VSWR=9:1, all phase angles		Unconditionally stable. Reliably operates with 10 Watts CW forward power, at case temperatures to +70 degrees C.					

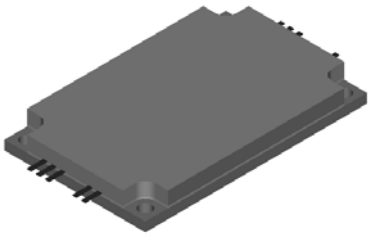
MAXIMUM RATINGS (@25degC, unless otherwise specified)

Rating	Symbol	Value	Unit
DC Drain Supply Voltage	Vs	32	Vdc
DC Gate Supply Voltage	V_{SG}	15	Vdc
RF Input Power	Pin	+25	dBm
Storage Temperature Range	Tstg	-40 to +150	Deg C
Operating Case Temperature Range	Tc	-30 to +90	Deg C
Maximum Operating Channel Temperature	Tch	+200	Deg C
RF Output Power	Pout	35	W
Thermal Resistance (Max channel temp rise divided by module dissipation for Pout=20W, at Tbase=+85 C)	Θjc	1.8	Deg C/W
ESD Protection a) Human Body Model b) Machine Model		Class 2 Class M3	

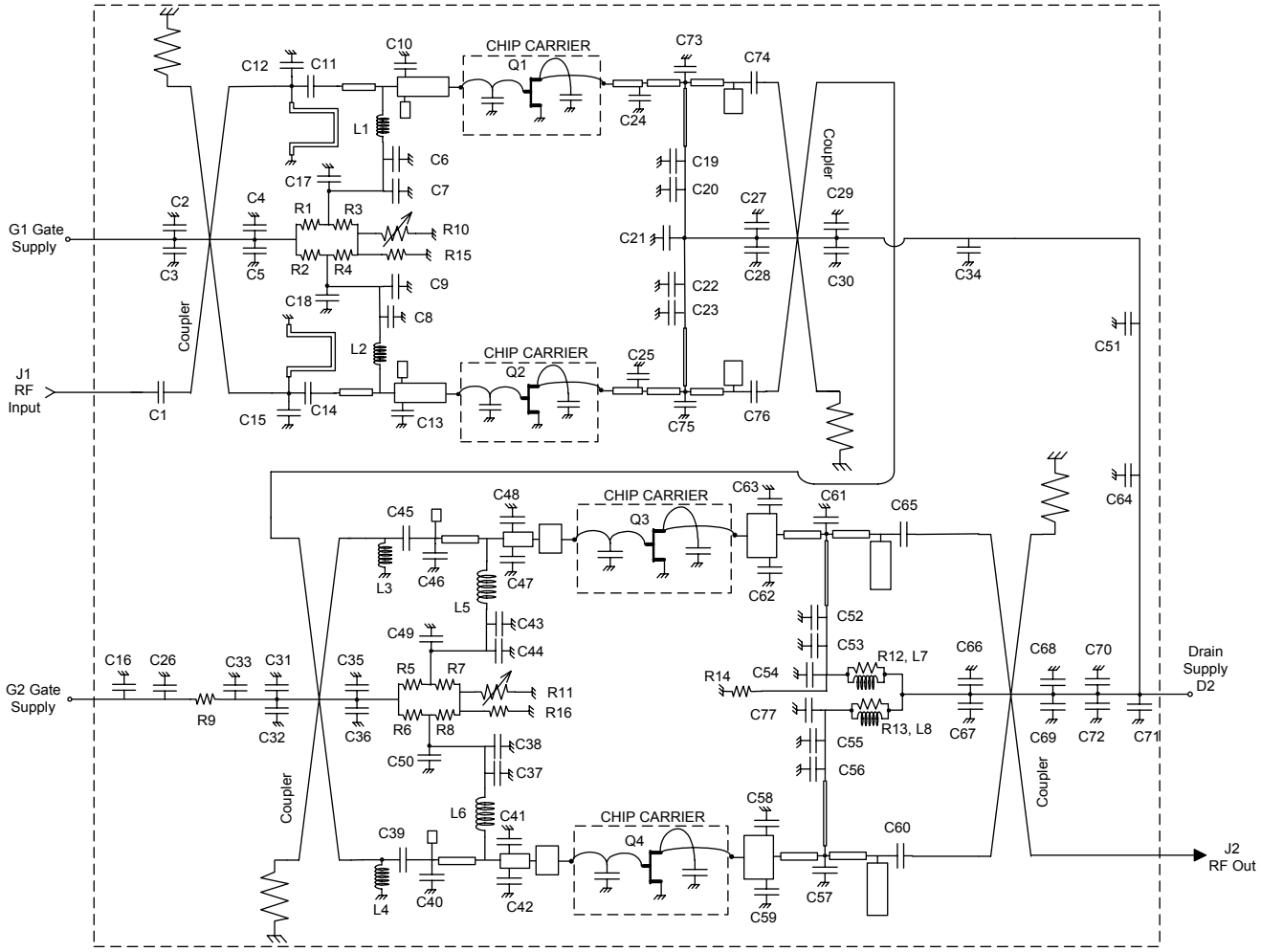
Outline Drawing



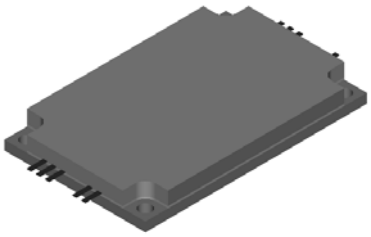
revision date: 02/11/02



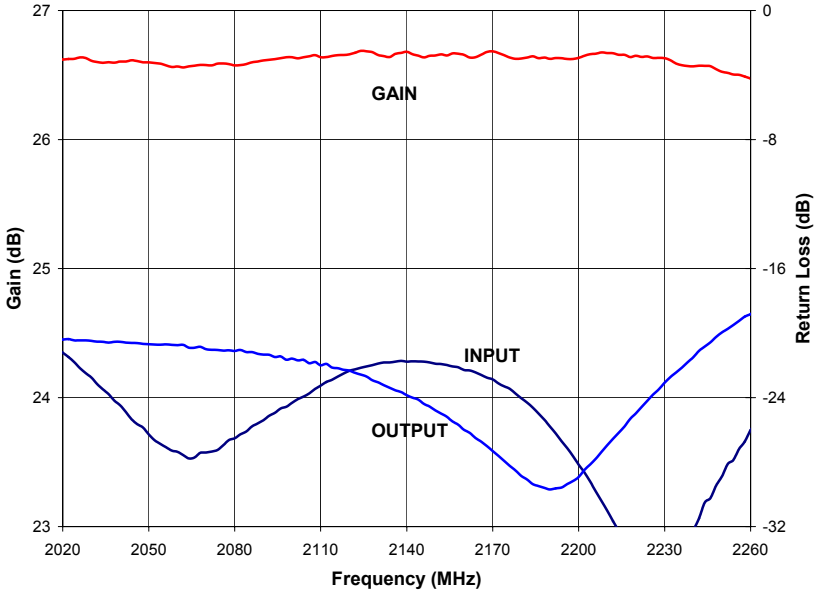
PFM2120WB PRELIMINARY SPECIFCATION (Continued)
2.08-2.20 GHz, 20W, Broadband Two-Stage Power Module



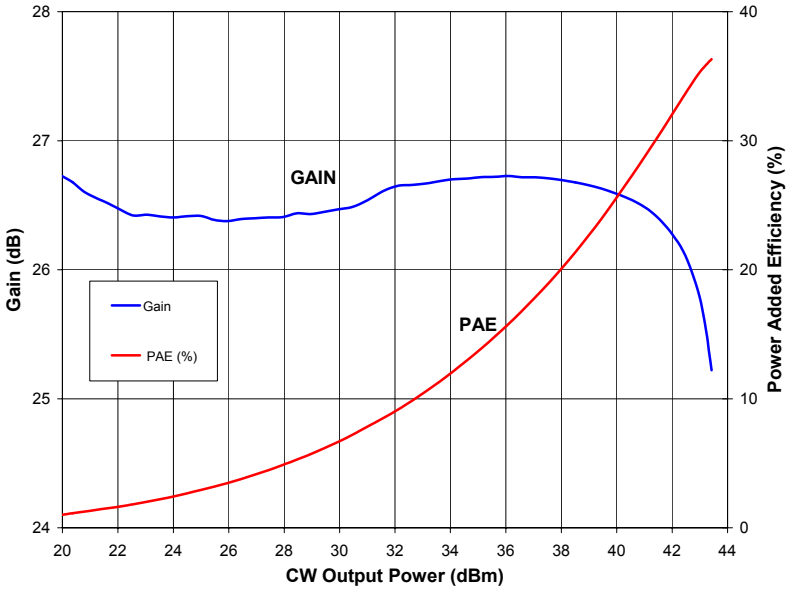
PFM21020WB Schematic



PFM2120WB TYPICAL PERFORMANCE

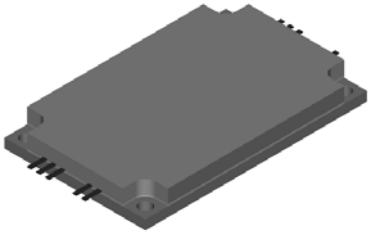


PFM21020WB Gain and Return Loss versus Frequency

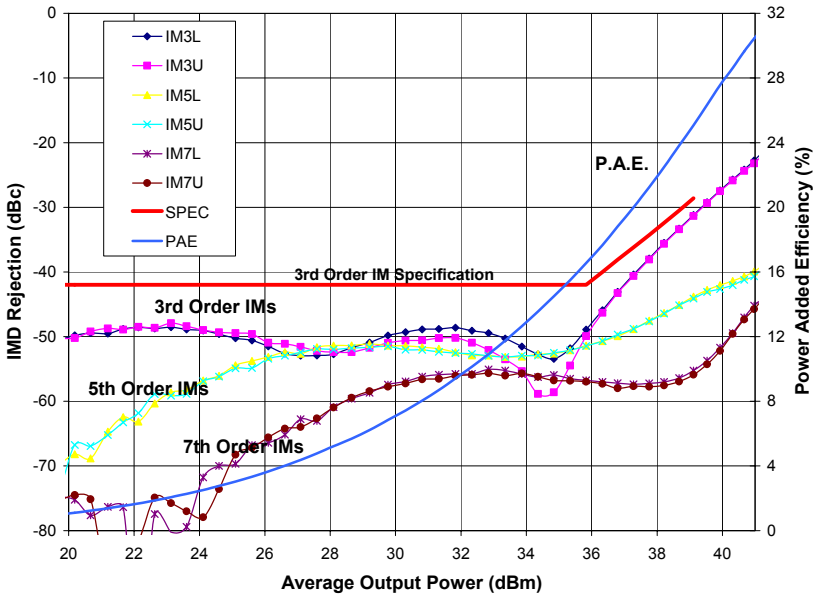


PFM21020WB Gain and Power Added Efficiency versus Output Power

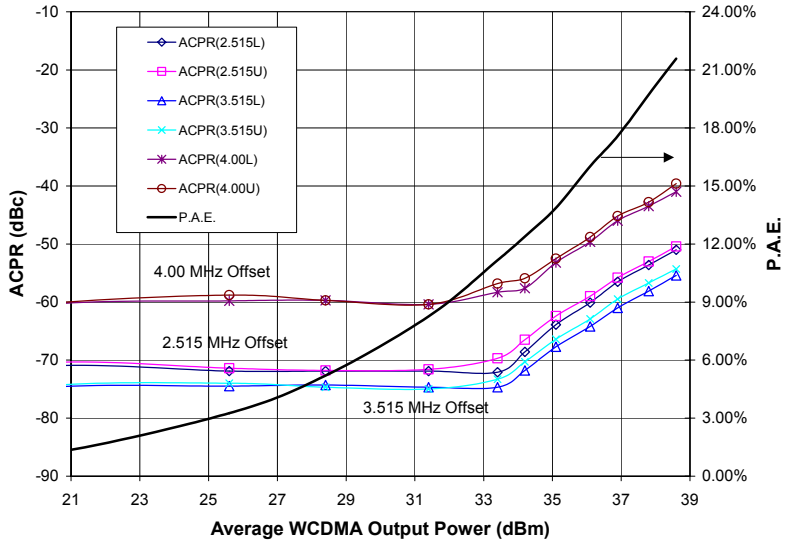
revision date: 02/11/02



PFM2120WB TYPICAL PERFORMANCE



PFM21020WB Two-Tone Intermodulation Products and Power Added Efficiency versus Average Output Power



PFM21020WB WCDMA ACPR & P.A.E. versus Average Output Power

(Source P/A=8.0 dB 1st 2nd ACPR Int. BW=30 KHz; 3rd ACPR Int. BW = 1.0 MHz)

revision date: 02/11/02